A 3-D Track-Finding Processor for the CMS Level-1 Muon Trigger

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We report on the design and test results of a prototype processor for the CMS Level-1 trigger that performs 3-D track reconstruction and measurement from data recorded by the cathode strip chambers of the endcap muon system. The tracking algorithms are written in C++ using a class library we developed that facilitates automatic conversion to Verilog. The code is synthesized into firmware for field-programmable gate-arrays from the Xilinx Virtex-II series. A second-generation prototype has been developed and is currently under test. It performs regional track-finding in a 60 degree azimuthal sector and accepts 3 GB/s of input data synchronously with the 40 MHz beam crossing frequency. The latency of the track-finding algorithms is expected to be 250 ns, including geometrical alignment correction of incoming track segments and a final momentum assignment based on the muon trajectory in the non-uniform magnetic field in the CMS endcaps.

1. INTRODUCTION

The endcap regions of the Compact Muon Solenoid (CMS) experiment will consist of four stations of Cathode Strip Chambers (CSC). These chambers will provide CMS complete azimuth coverage (in I), as well as 0.9 to 2.4 in pseudo-rapidity (K. Six cathode strip chambers compose a single station in the endcap system. The chambers are trapezoidal in shape, extending 10^o or 20^o in I, and are composed of cathode strips aligned radially from the beam axis, and anode wires aligned in the orthogonal direction.

In the endcap system, muon track-finding is electronically partitioned into six 60^o sectors. A single Sector Processor (SP) receives trigger primitives from front-end electronics which sit on or near the CSCs. The front-end electronics form Local Charged Tracks (LCTs) from the six detector layers of a station. A Muon Port Card (MPC) collects the LCTs for a given station and sector, sorts them, and sends the best three to an SP via optical fibers. A single SP collects LCTs sent via fifteen 1.6 Gbit/s optical links, and is responsible for linking LCTs in I and K in order to form full tracks, and to report the transverse momentum (p_t), I, and K for each track. The entire Track-Finding processor is composed of twelve such SPs housed in a single 9U VME crate. The challenge for the Track-Finding Processor is to report muon candidates with the lowest possible Pt threshold, and yet maintain a single muon trigger rate below 1 kHz/K at full Large Hadron Collider (LHC) luminosity.

This paper is organized as follows: Section 2 will describe the Track-Finder (TF) algorithm, Section 3 will discuss the first prototype, Section 4 will discuss the second prototype including preliminary test results, Section 5 will discuss software used for the SP, and a summary can be found in Section 6.

2. TRACK-FINDER LOGIC

The principle of the TF logic [1] is illustrated in Figure 1. The Track-Finding process is partitioned into several steps. A given station within a sector may have as many as three LCTs reported to the SP. These LCTs are then converted into track-segments, which are described in terms of their I, and K coordinates. Each track-segment in each station should be checked against the other segments in neighboring stations for consistency to share a single track. Thus, each track-segment is extrapolated through to other stations, and compared against existing segments. If an extrapolation is successful, these segments are "linked" to form a single track. Each possible pairwise combination is tested in parallel. After extrapolation, doublets are then linked to assemble full tracks. Redundant tracks are cancelled, the best three tracks are selected, and the track parameters are then measured.

The SP has the ability to handle LCTs received out of step from the actual bunch crossing time in which they originated. This is accomplished by the Bunch Crossing Analyzer, which allows the Sector Processor to form tracks from LCTs received up to one bunch crossing later than the earliest LCT.

The first step in the track-finding process is to extrapolate pairwise combinations of track-segments. This is accomplished by requiring the two segments to be consistent with a muon originating from the collision vertex and with an appropriate curvature induced by the non-uniform magnetic field. A successful extrapolation is assigned when two stubs lie within allowed windows of I and K - neither LCT should parallel to the beam axis, and both should appear to originate from the interaction region

The Track Assembler Units (TAUs) examine successfully extrapolated track-segment pairs to see if a larger track can be formed. If so, those segments are

combined and a code is assigned to denote which muon stations are involved.

A list of nine possible tracks is sent to the Final Selection Unit (FSU). Since different data streams may contain data from the same muons, the FSU must cancel redundant tracks, and select the best three distinct candidates.

The final stage of processing in the TF is the measurement of the track parameters, which includes the M and K coordinates of the muon, the magnitude of the transverse momentum P_T, the sign of the muon, and an overall quality which we interpret as the uncertainty of the momentum measurement. The most important quantity to calculate accurately is the muon P_T , as this quantity has a direct impact on the trigger rate and on the efficiency. Simulations have shown that the resolution of the momentum measurement in the endcap using the displacement in M measured between two stations is about 30% at low momenta, when the first station is included. (It is worse than 70% without the first station.) We would like to improve this so as to have better control on the overall muon trigger rate, and the most promising technique is to use the M information from three stations when it is available. This improves the resolution to approximately 22% at low momenta, which is sufficient. In order to achieve a three-station P_T measurement, we have developed a scheme that uses the minimum number of bits necessary in the calculation.

Figure1: Sector Processor logic principle

The first step is to do some pre-processing in FPGA logic: the difference in M is calculated between the first two track segments of the muon, and between the second and third track segments when they exist. Only the essential bits are kept from the subtraction. For example, we do not need the same accuracy on the second subtraction because we are only trying to untangle the multiple scattering effects at low momenta. The subtraction results are combined with the K coordinate of the track and the track type, and then sent into a 4 MB memory for assignment of the signed P_T. Tracks composed of only two track segments are allowed also in certain cases.

3. FIRST PROTOTYPE SYSTEM ARCHITECTURE

4. SECOND (PRE-PRODUCTION) PROTOTYPE SYSTEM ARCHITECTURE

Although the first prototype was proven a success, improvements were needed in the overall Level-1 Trigger design in order to meet the latency allowance of 3.2 Ps. Recent significant improvements in logic density [5] allow implementing all Sector Processor logic onto one Xilinx Virtex-II FPGA (XC2V4000). Also, the optical link components have become smaller and faster; thus allowing the merger of three Sector Receivers and one Sector Processor of the first prototype onto one sixteen-layer board (Figure 3).

This board accepts fifteen optical links from the Muon Port Cards, where each link carries information corresponding to one muon track segment, which is described by a 32-bit word (two 16-bit frames). Each link transmits a 32-bit word every 25 ns. Finisar's FTRJ-8519-1-2.5 transceiver is used by the MPC for transmission, and by the SP for reception of LCT data. Additionally, the board receives up to 8 muon track segments, sent using LVDS synchronous with the 40

In the second prototype Track-Finder system, we no longer use Channel Links for the backplane transmission because of their long serialization/deserialization latency of 100 ns; rather, GTLP backplane technology is now used. This allows transmitting the data point-to-point (from Sector Processor to Muon Sorter) at 80 MHz, with no time penalty for serialization since the most time-critical portions of data are sent. The SP will also send data to a DAQ readout board over the SP's sixteenth optical link. This board receives the LCT data received by the SP from the MPC, and final results completed by the SP. The entire second prototype Track-Finder system fits into one 9U VME crate (Figure 5).

The second prototype has been designed and built, and is now undergoing tests. So far, the FPGAs have been successfully programmed, and the VME interface and the onboard databus have been validated. Successful tests have also been completed to verify operation of the TLK2501 chips on the SP. These chips have the ability to generate pseudo random bit streams to facilitate testing of a single chip (internal loop-back test), or pairs of chips. In transmitting these bit streams over optical fibres, one TLK2501 is used to send data, and another is used to receive data. Because the SP is equipped with optical transceivers, one can transmit and receive these bit streams on the same SP by utilizing multiple links. Such tests were also completed between a Muon Port Card and a Sector Processor. The MPC sat in the same VME crate as the SP using a special test slot designed in the custom backplane. Test routines were written which load test LCT patterns into the MPC input buffer, and transmit a subset of these patterns over the optical links into the SP. The output LCTs from the MPC were checked against the SP input LCTs, and were found to be in agreement.

The original design for the optical links called for a common clock for the operation of transceivers and for trigger logic; however, it is enough to have a low-jitter clock (e.g. from a crystal) operating at the transmitter frequency, which act as a reference for the transceivers, and a second clock driving the SP logic; such a design would allow the links to operate more robustly with respect to clock jitter in the distributed LHC clock. More tests will be conducted between the MPC and SP to determine the most optimal clock configuration.

Future tests also include: operation of Sector Receiver memories and verification of Track-Finding logic. There will also be opportunities to examine the functionality of the Sector Processor during a possible future beam test, and with the use of cosmic rays.

All software used for testing of the second prototype was written using the Hardware Access Library (HAL), which is part of the XDAQ software package from CMS

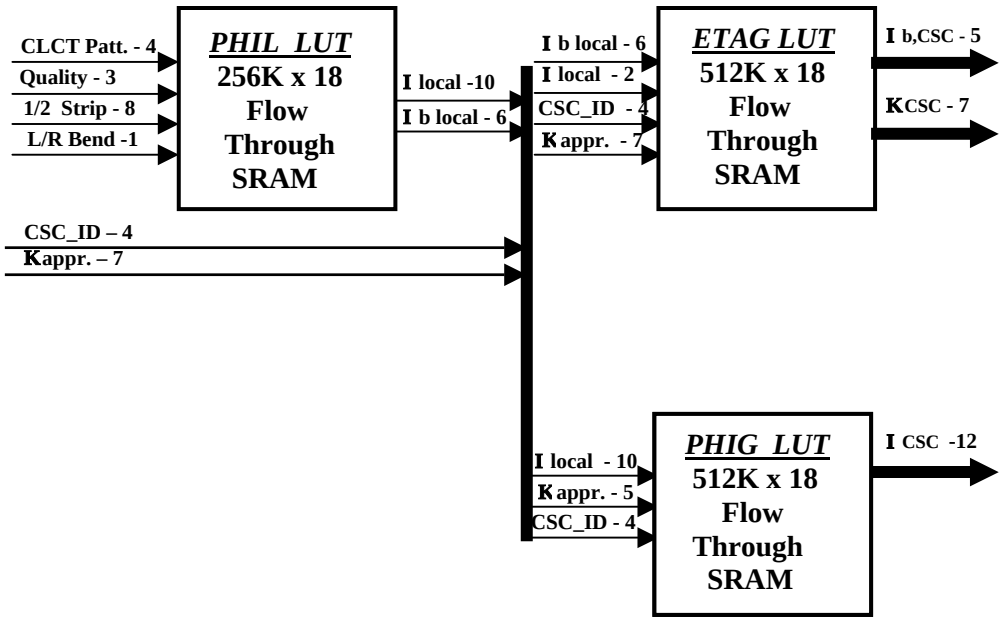

Figure 4: Sector Receiver look-up memory scheme. Here "CLCT Patt", "Quality", "½ Strip", "L/R Bend", "CSC_ID", and "Kappr." are variables that describe a LCT received by the Sector Receiver. From this data, I with respect to the given chamber ("I local"), and the bend angle ("Ib local") are found. These are then sent to more memories from which I ("I CSC-12") and K("KCSC-7") are reported.

bit-for-bit compatible simulation. This Verilog code can then be synthesized by our FPGA vendor tools and is used as our SP Firmware. This allows us to verify the SP logic through C++ debugging tools such as MS Visual C++. We can also run this code as a part of the CMS simulation and reconstruction framework - thus allowing us to use usual analysis tools for verification (e.g. ROOT); therefore, a line-by-line correspondence is maintained between simulation logic and Firmware logic.

6. SUMMARY

The design of a Track-Finder for the Level-1 trigger of the CMS endcap muon system is mature and has been successfully prototyped. The design is implemented as 12 identical processors, which cover the pseudo-rapidity interval $0.9 < K < 2.4$. The track-finding algorithms are three-dimensional, which improves the background suppression. The P_T measurement uses data from 3 endcap stations, when available, to improve the resolution to 22%. The input to the Track-Finder can be held for more than one bunch crossing to accommodate timing errors. The latency is expected to be 7 bunch crossings (not including the optical link and timing errors accommodation). The design is implemented using Xilinx Virtex FPGAs and SRAM look-up tables and is fully programmable. The first prototype was successfully built and tested; the pre-production prototype has been built and is currently undergoing tests.

7. REFERENCES

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