A Prototype Track-Finding Processor for the Level-1 Trigger of the CMS Cathode Strip Muon System

S.M.Wang, D.Acosta, A.Madorsky, B.Scurlock
University of Florida

A.Atamanchouk, V.Golovstov, B.Razmyslovich
PNPI

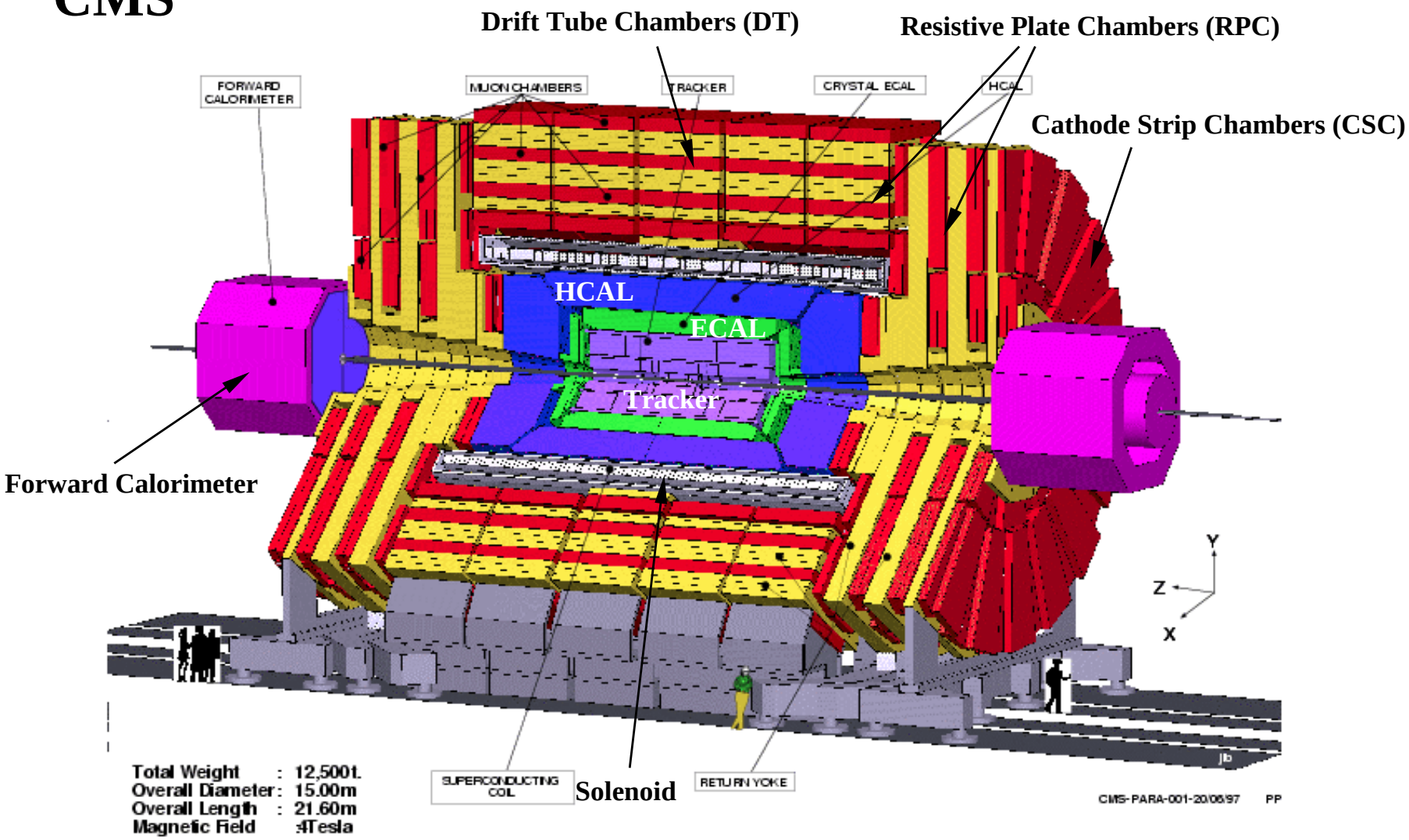
DPF 2000
August 9-12, 2000

Track-Finding Processor Prototype

- We have designed and built a prototype Track-Finding processor for the Level-1 Trigger of the CMS Endcap Muon System
- It is fast and efficient in linking tracks segments into complete 3-D tracks
- Measures the P_t, ϕ, η of these tracks

- In this talk :
  - Design of the prototype
  - Test results of the prototype

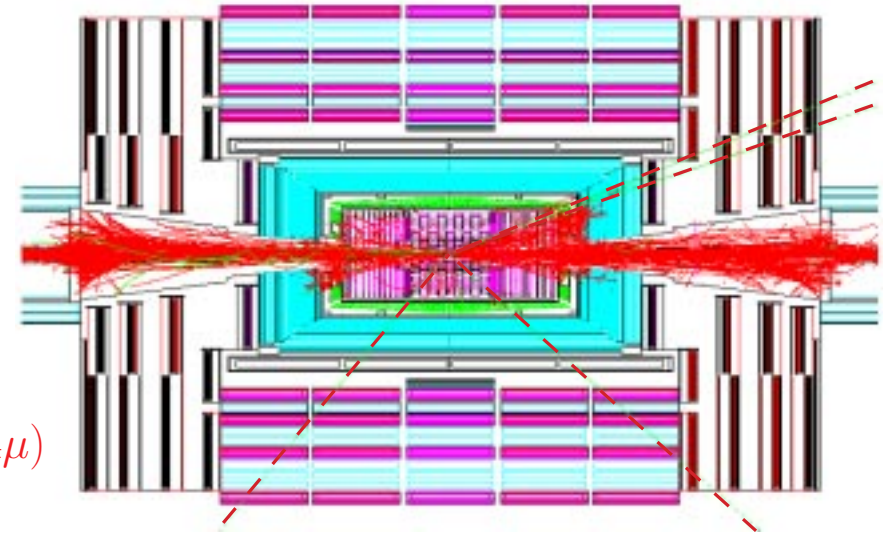
CMS


Drift Tube Chambers (DT)
Resistive Plate Chambers (RPC)
Cathode Strip Chambers (CSC)
FORWARD CALORIMETER
MUON CHAMBERS
TRACKER
CRYSTAL ECAL
HCAL
HCAL
ECAL
Tracker
Forward Calorimeter
Solenoid
SUPERCONDUCTING COIL
RETURN YOKE
Total Weight : 12,500t.
Overall Diameter: 15.00m
Overall Length : 21.60m
Magnetic Field :4Tesla
Y
Z
X
CMS-PARA-001-20/06/97 PP

Purpose for a Fast and Efficient Muon Trigger

At LHC :

- Expect muons to provide clear signature for a wide range of interesting physics processes
  - Higgs production, B Physics, New Physics ...



$(H \rightarrow ZZ^* \rightarrow 4\mu)$

- These interesting physics events have low production cross sections
- Need high luminosity ($\Rightarrow$ high bunch crossing rate (40 MHz)) to observe these rare processes
- Require a fast and efficient muon trigger to:
  - efficiently tag muons from rare physical processes, and reject most muons from large background processes
  - perform trigger operation in a short period of time (3.2 μs for Level-1)

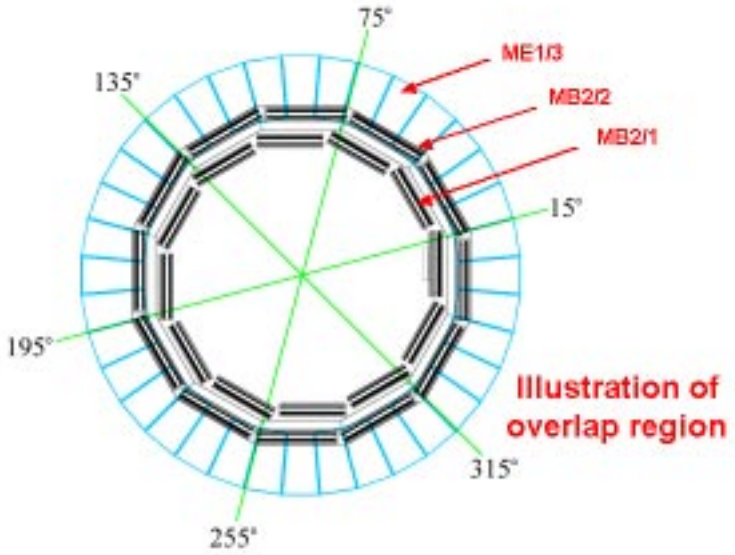
Requirements for CSC Track-Finder

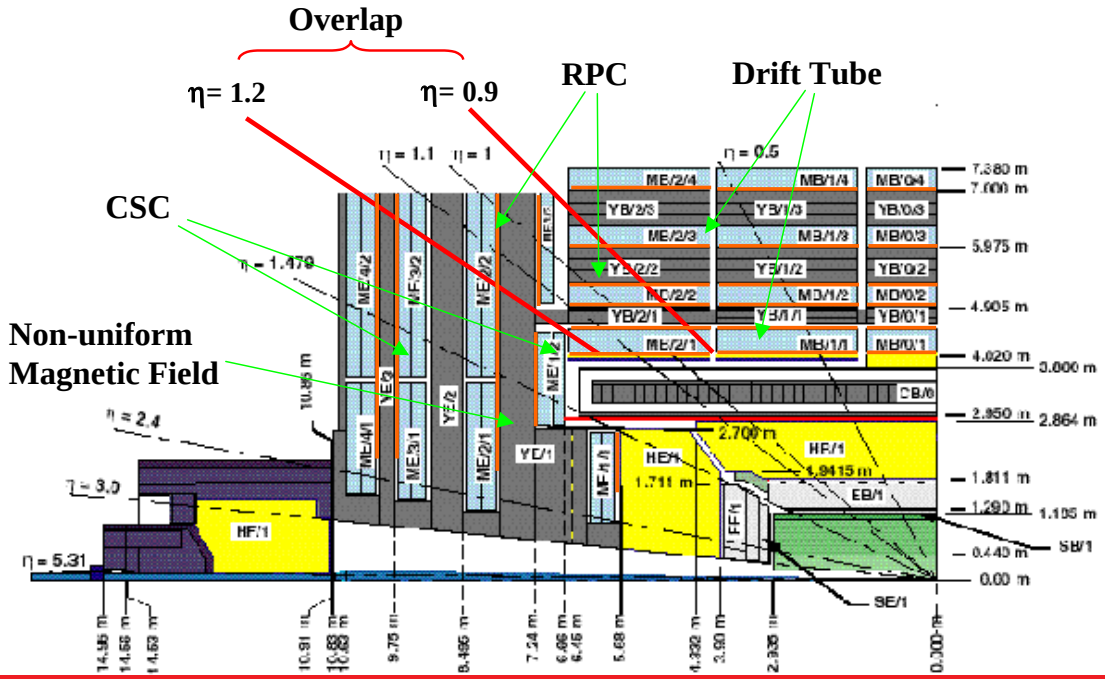
- High efficiency with low P_t threshold ($\sim$ 20 GeV/c)
- Single muon trigger rate $<$ few kHz at $L = 10^{34}\text{cm}^{-2}\text{s}^{-1}$
- P_t resolution $\approx 20\%$
  - Require 3-D tracking and information from 3 CSC stations
- Multi-muon capability
- Pipelined at 40 MHz bunch crossing frequency
  - deadtime-less
- Small latency, = 16 bunch crossing (400 ns)
- Programmable $\Rightarrow$ FPGA and RAM implementation
  - Allows experiment to adapt to different background conditions and collision rates

CSC Level-1 Trigger

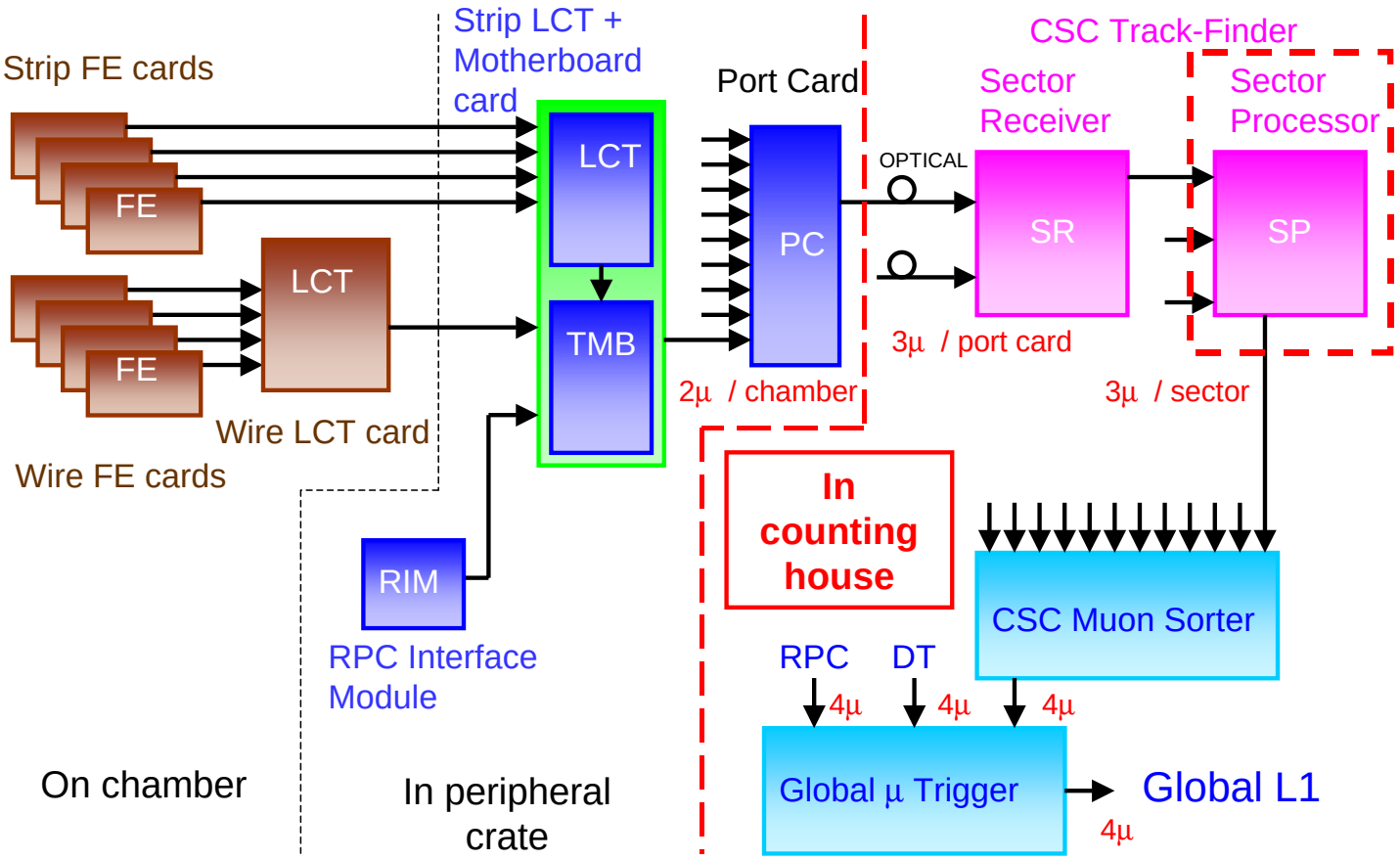
Trigger Regions :

- Divided into 60° sectors in azimuth for both endcaps
- η region covered by each sector includes Overlap region ($1.0 \lesssim |\eta| \lesssim 1.2$), and Endcap region ($1.2 \lesssim |\eta| \lesssim 2.4$)

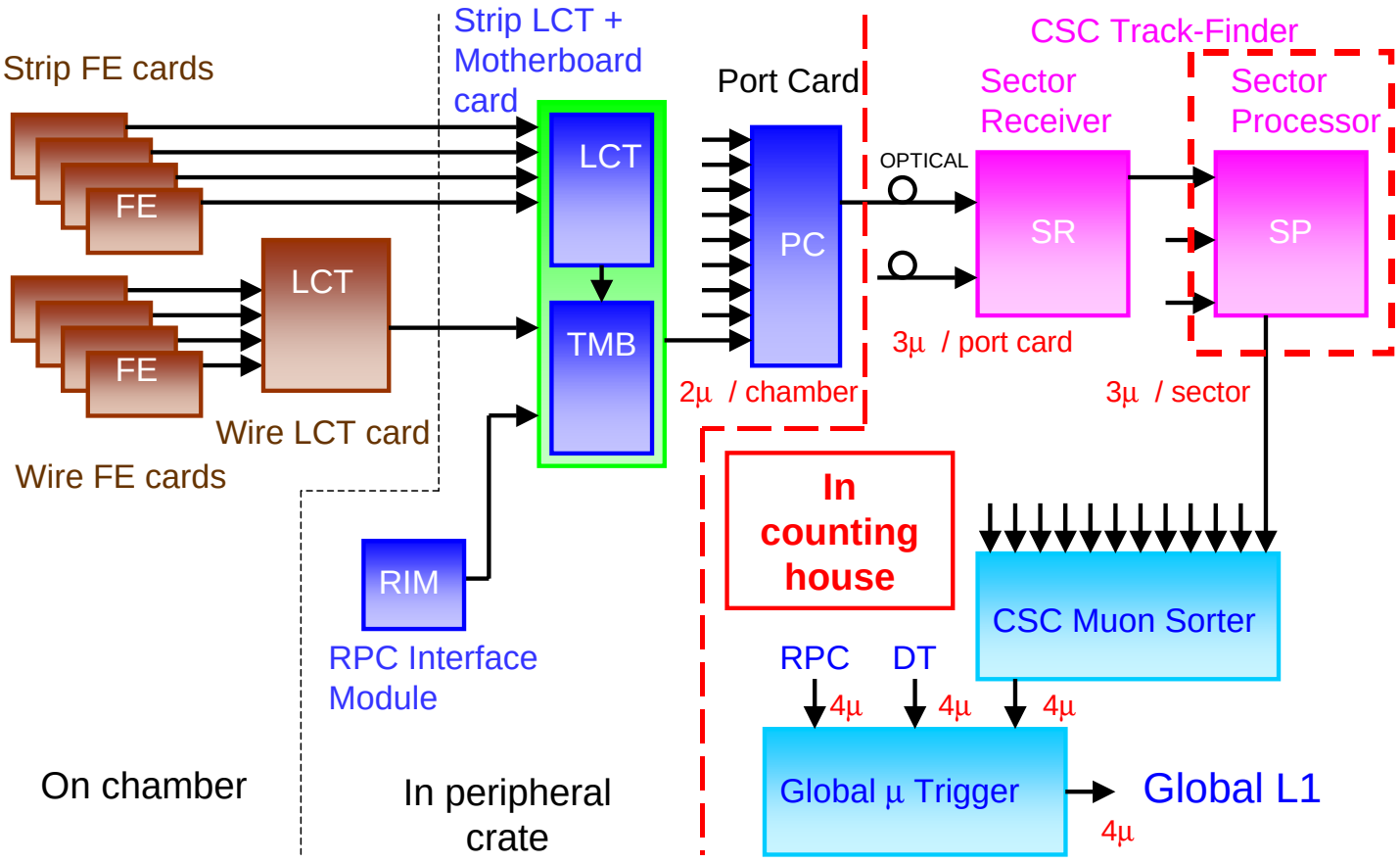




CSC Level-1 Trigger Scheme



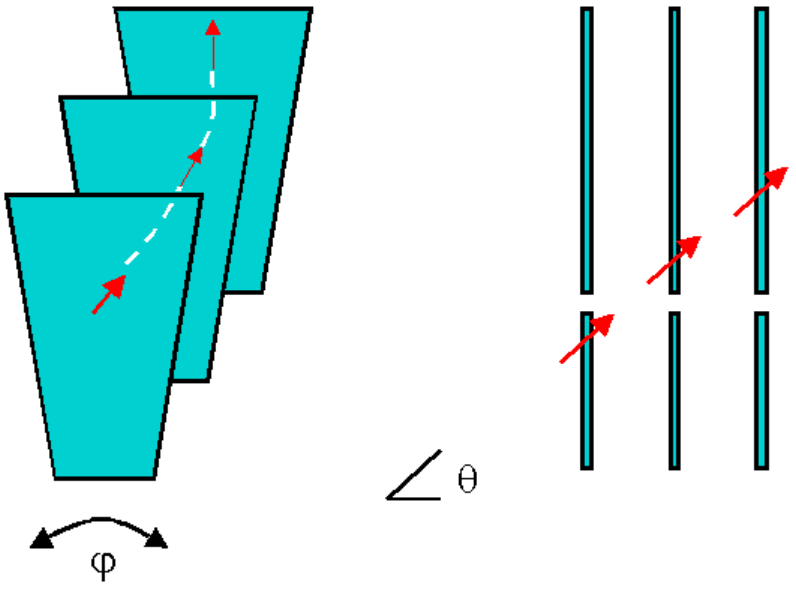
CSC Level-1 Trigger Scheme



- Track segments from chambers in 60° sector are sent to Sector Receiver for pre-processing before sending to Sector Processor
- Track-finding is performed in the Sector Processor.
- Sector Processor also receives track segments from Drift Tube chambers for track-finding in the overlap region

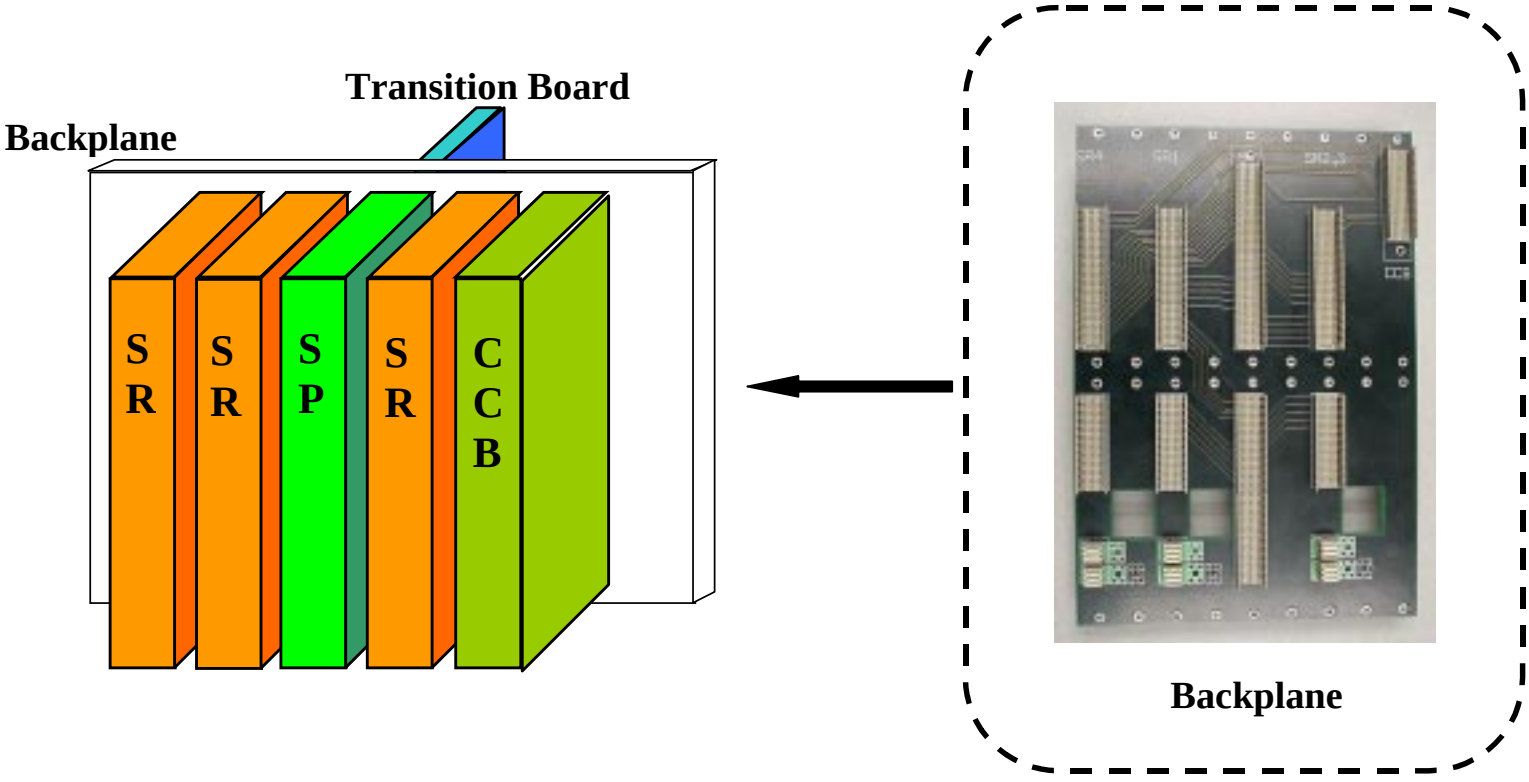
CSC Track-Finder Architecture

- Track-Finder implemented as 12 Sector Processors (6 for each endcap)
- Each Sector Processor :
  - Handles track segments in 60° azimuthal sector
  - Perform 3-D track-finding from track segments (match segments in ϕ and η)
  - Measure P_t, ϕ, and η.
  - Send up to 3 best track candidates to the Muon Sorter

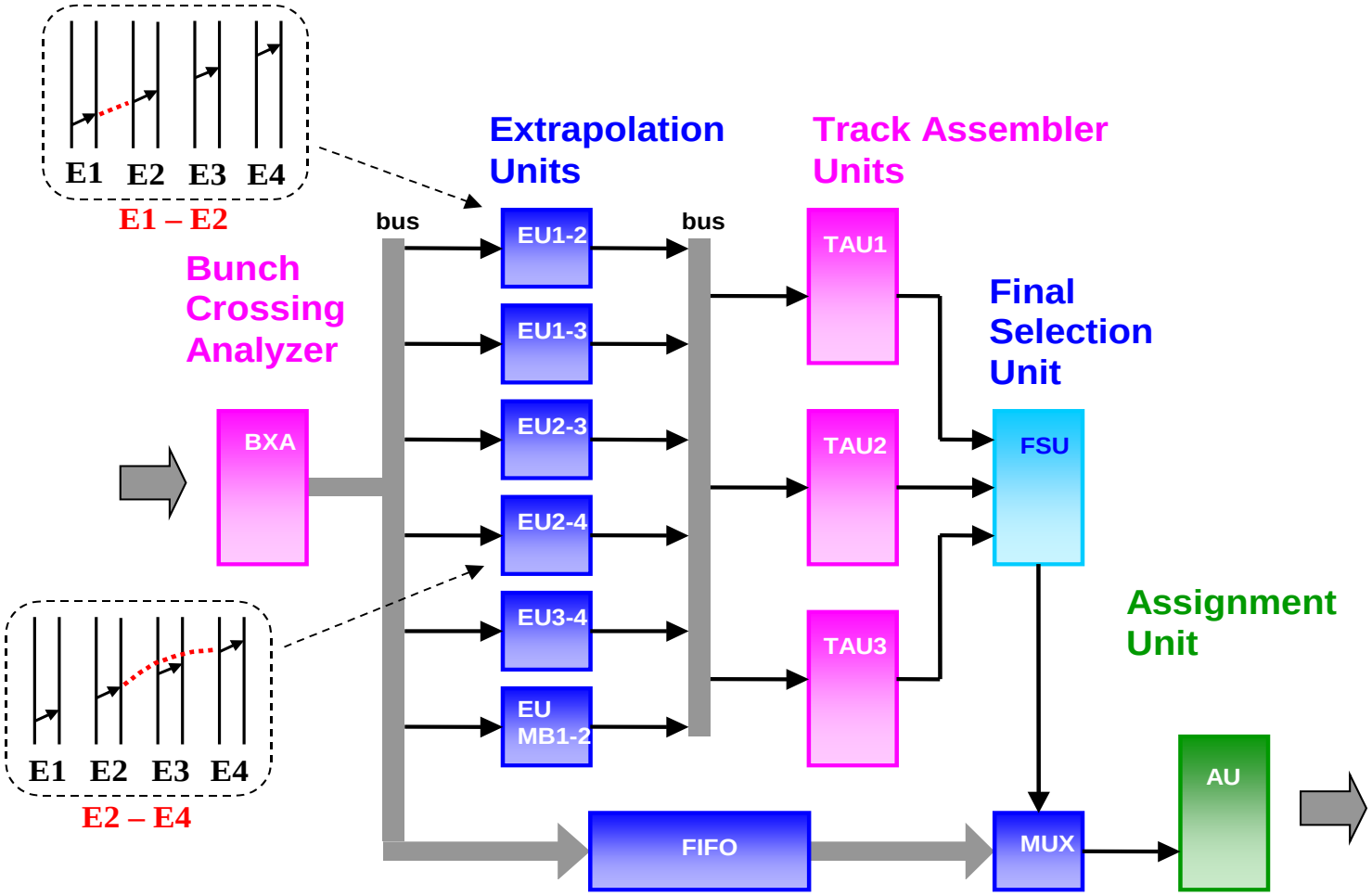


CSC Track-Finder Architecture

- Each Sector Processor implemented on a 9U VME card
- CSC track segments are sent from 3 Sector Receivers (SR) via custom point-to-point backplane. DT track segments arrive via a transition board at the back of crate
- Custom point-to-point backplane
  - Delivers $\sim$ 600 bits every 25 ns (3 GBytes/s)
  - Operates at 280 MHz to reduce connections
    - National Channel Link 28:4 serialization

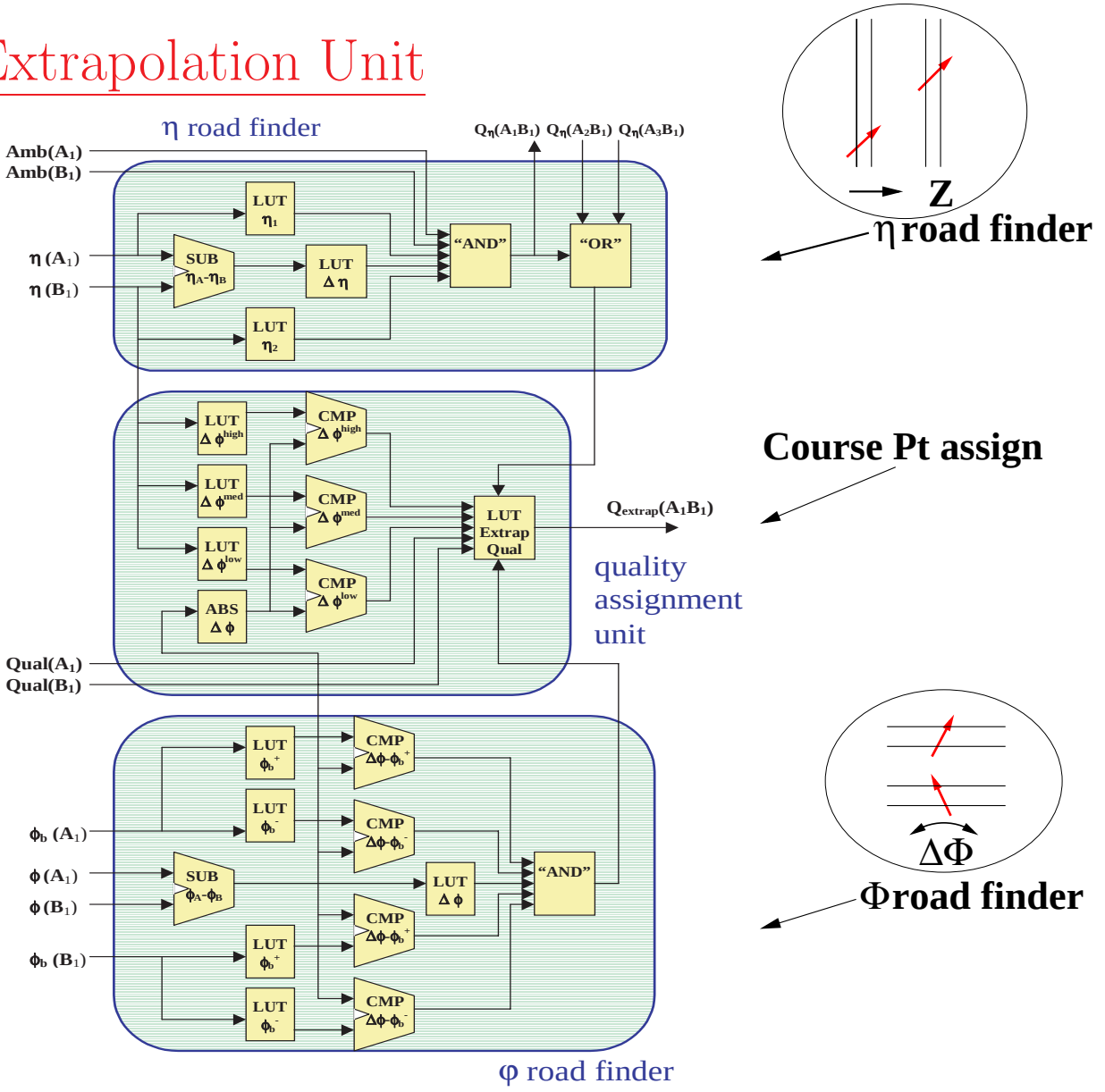


Sector Processor Block Diagram



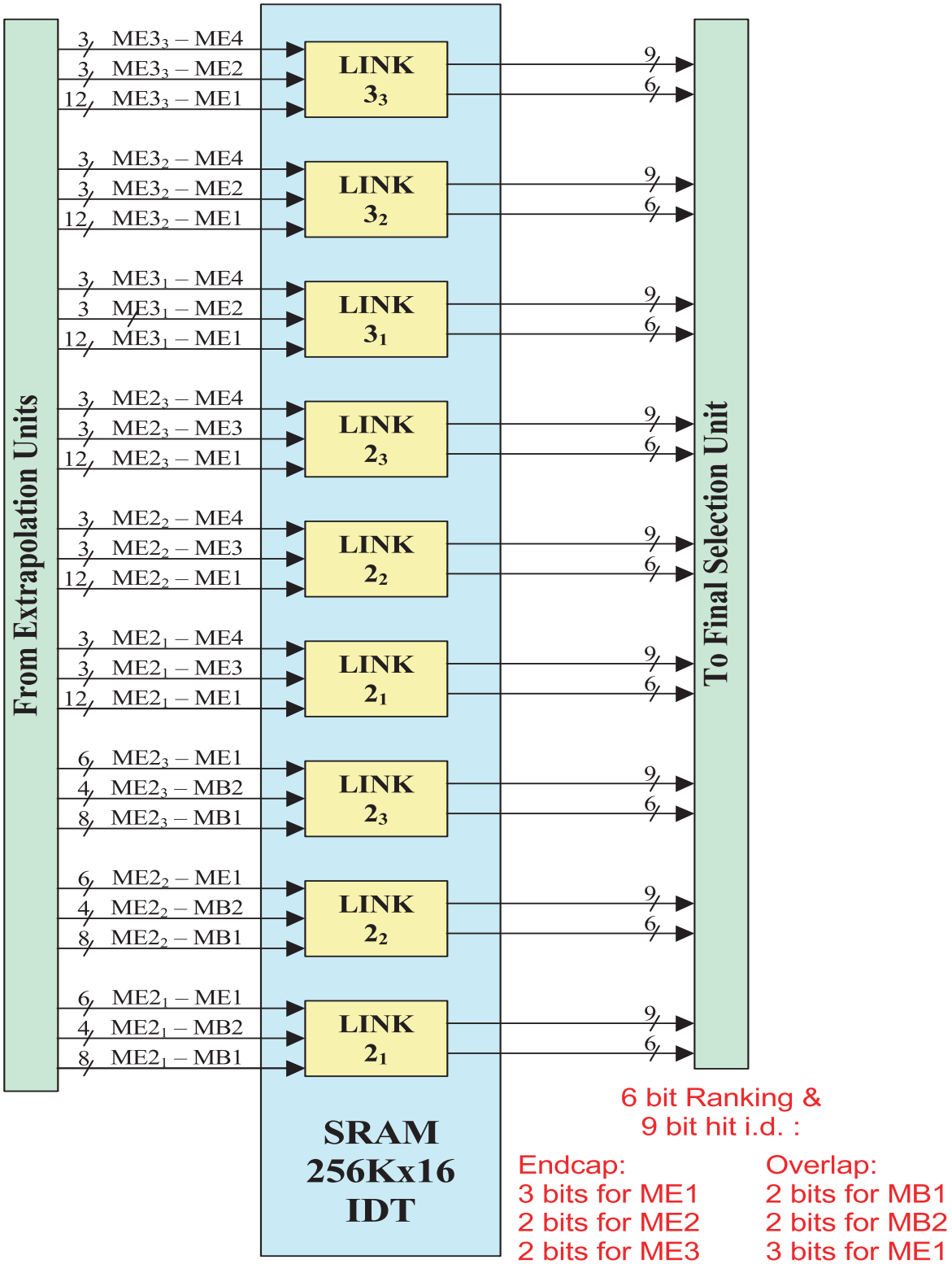
- Main components :
  - Bunch Crossing Analyser (BXA) : accumulate track segments for a couple of B.X., to accommodate error in B.X. assigned to track segments
  - Extrapolation Units (EU)
  - Track Assembler Unit (TAU)
  - Final Selection Unit (FSU)
  - Assignment Unit (AU)
- Expected overall latency is 16 B.X.

Extrapolation Unit



- Link track segments from two muon stations in 3-D :
  - Test if segments are matched in η
  - Check if $\Delta\Phi$ is consistent with the bend angles in each station
  - Assign coarse Pt
  - Output Quality: no match, low, medium, or high P_t
- 87 individual extrapolations are performed in parallel, a total of $\sim 10^{11}$ operations per second

Track Assembler Unit (TAU)

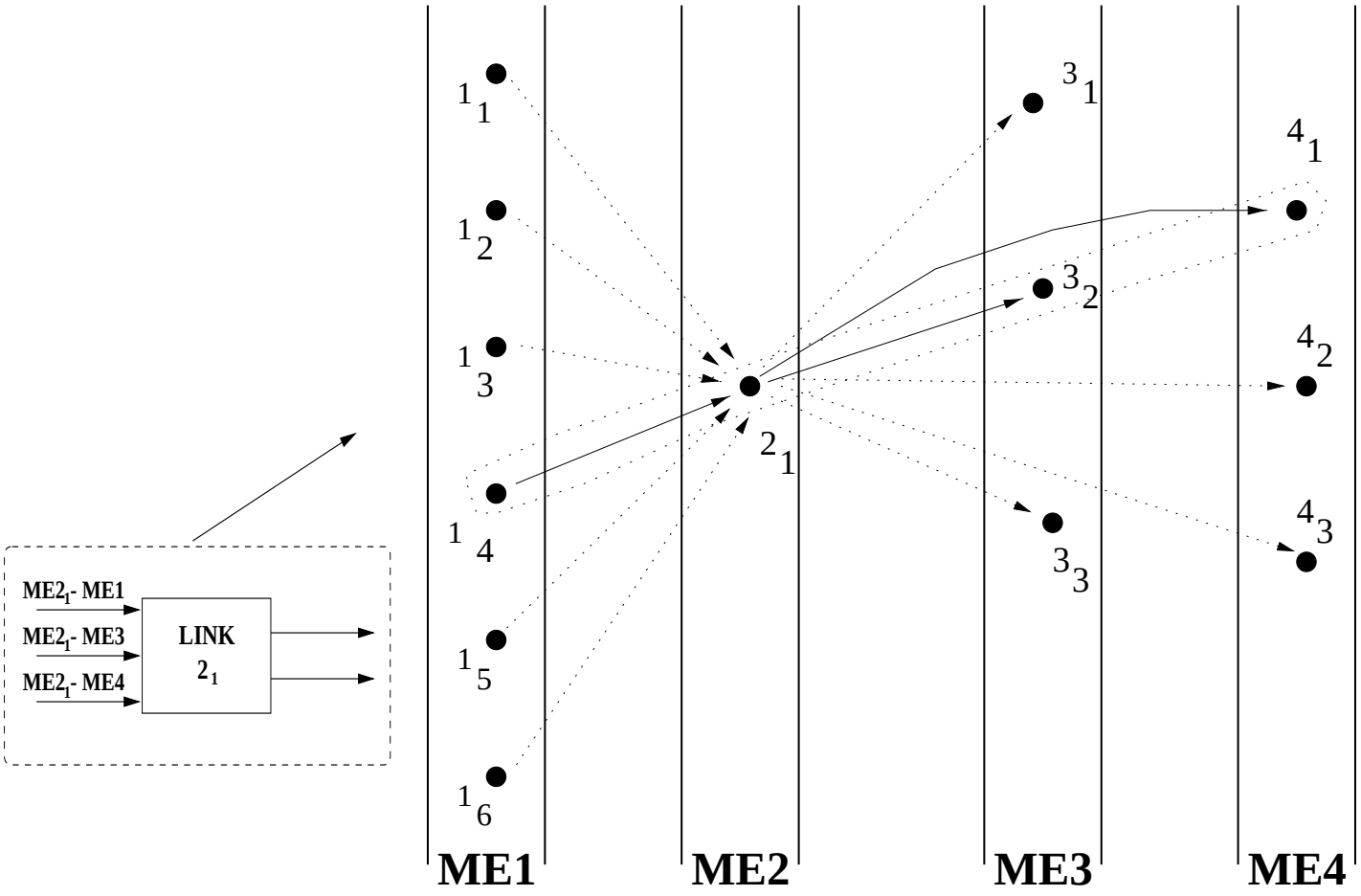


6 bit Ranking &
9 bit hit i.d. :

Endcap:
3 bits for ME1
2 bits for ME2
2 bits for ME3
2 bits for ME4

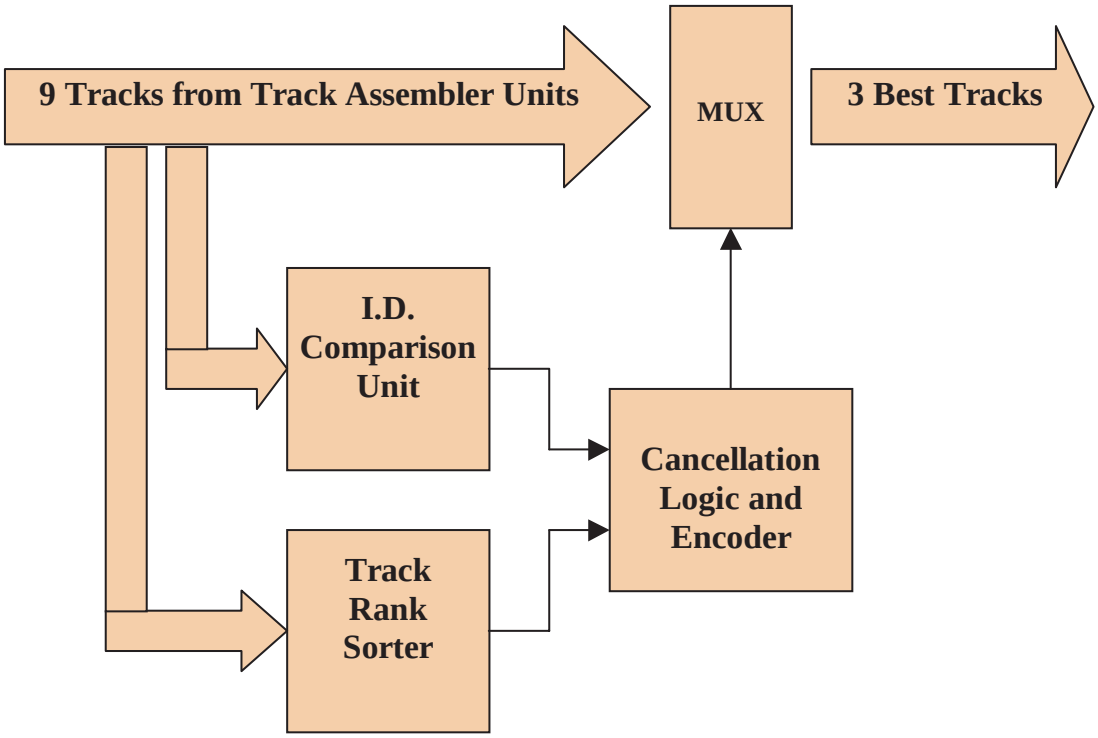
Overlap:
2 bits for MB1
2 bits for MB2
3 bits for ME1
2 bits for ME2

- TAU implemented as 9 static RAM memories for Endcap and Overlap
- Each Link unit handles all extrapolations to a single track segment in station 2 or 3. Successful extrapolations are used to form the best track pattern.



- Id of the track segments and the quality of the assembled track are sent to the Final Selection Unit (FSU)

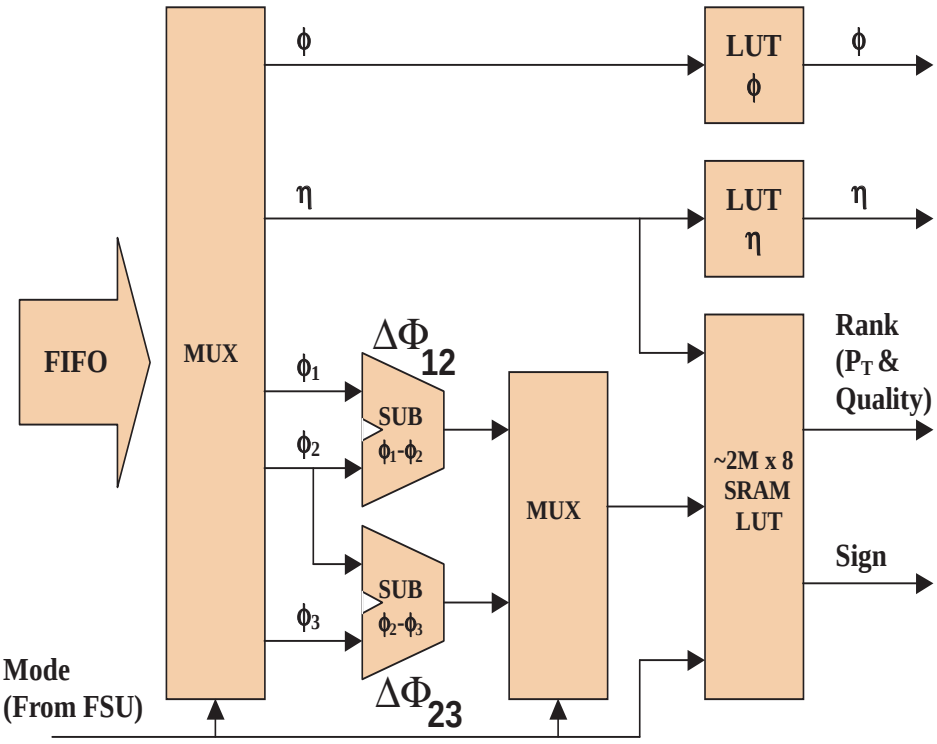
Final Selection Unit (FSU)

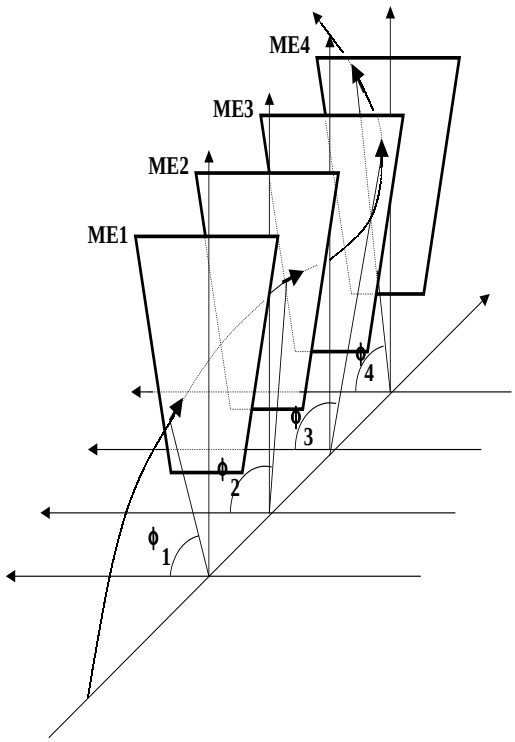


- Compare the qualities of the tracks and the ID of the track segments that form the tracks to
  - cancel redundant tracks
  - select 3 best distinct tracks
    (best $\Rightarrow$ highest P_t)

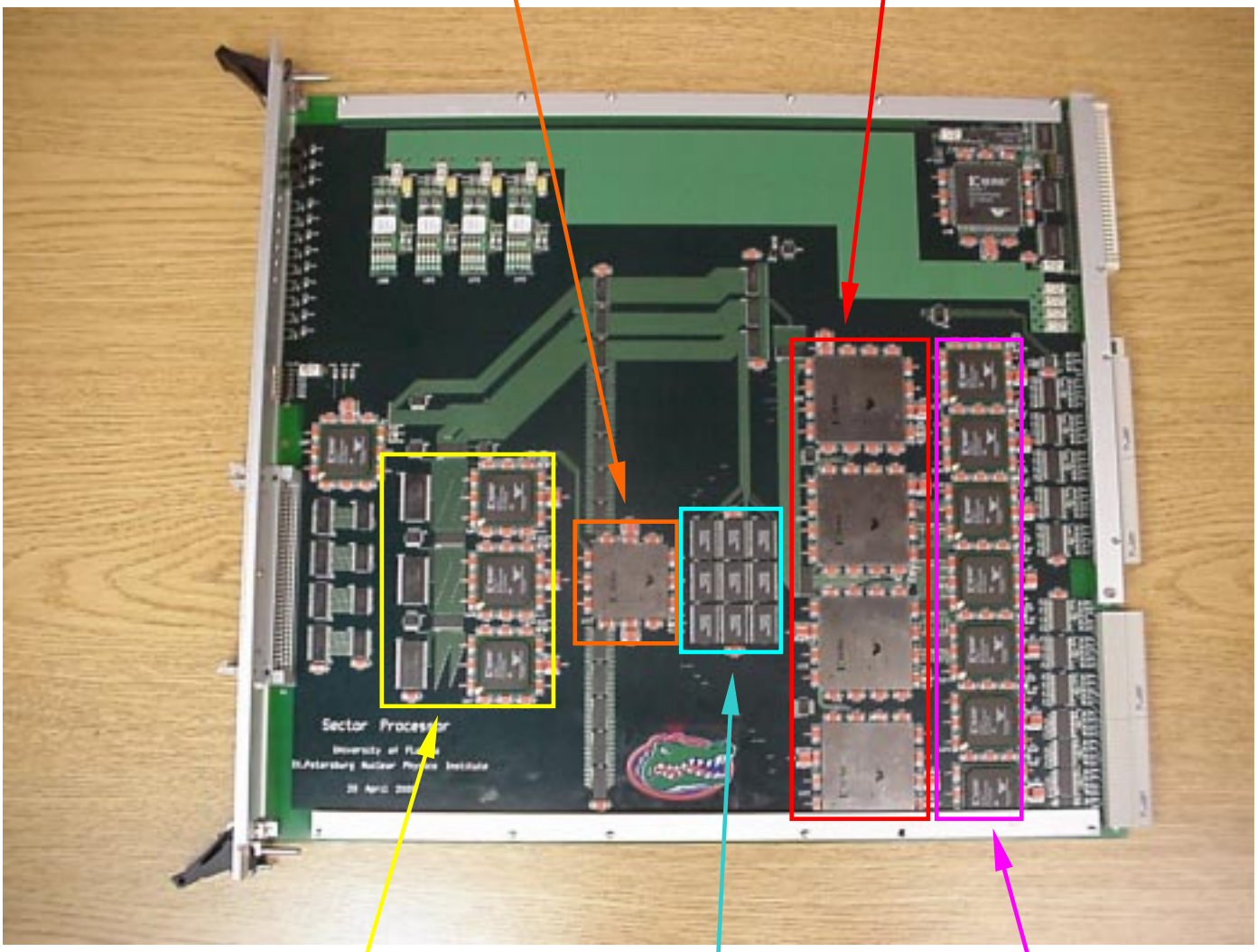
Assignment Unit

- Determines ϕ, η, P_t of the 3 best muon candidates selected by the Final Selection Unit
- P_t determined from the sagitta measured between 2 or 3 muon stations in the endcap fringe field
  - $\sigma_{Pt}/Pt \sim 30\%$ with only 2 stations
  - $\sigma_{Pt}/Pt \sim 20\%$ with 3 stations
    $\Rightarrow$ improve rate reduction at Level 1
- Implemented with FPGA preprocessing followed by large SRAM look-up table





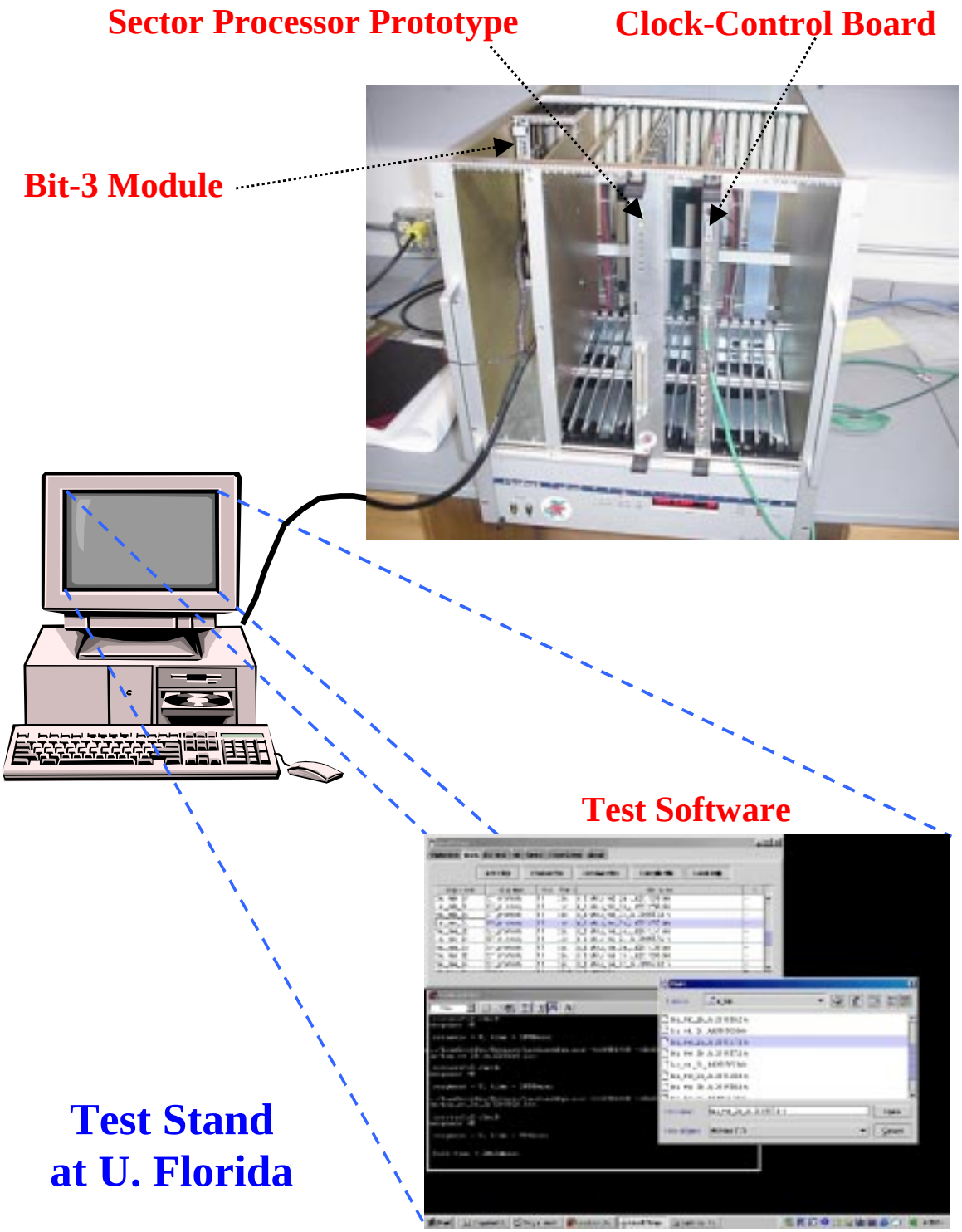
CSC Sector Processor Prototype



XCV => Xilinx Virtex FPGA

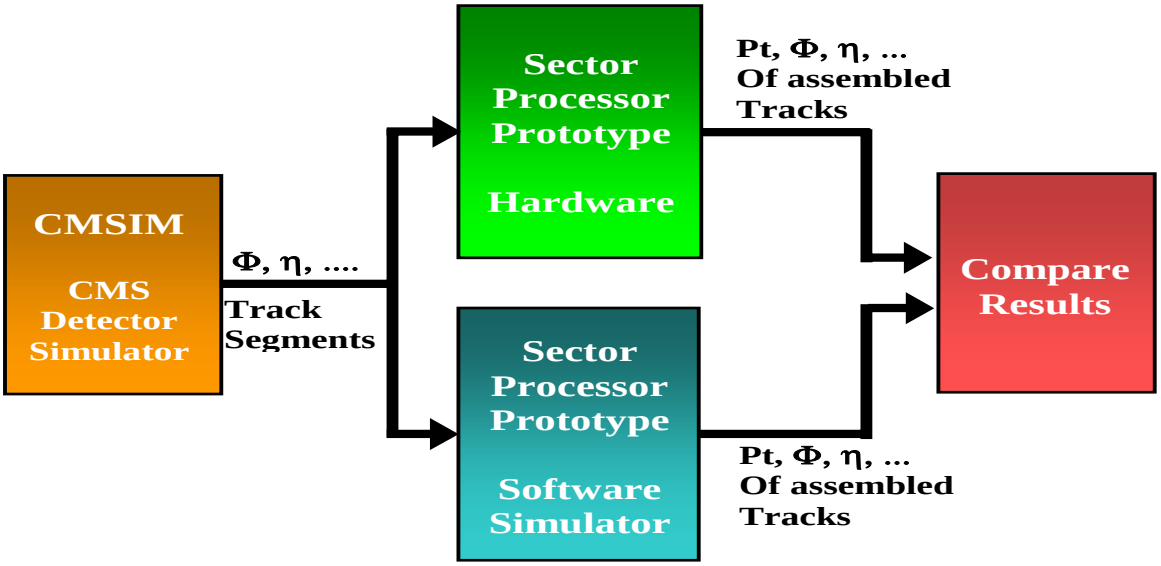
Test of the CSC Sector Processor ProtoType

- Currently SP prototype is undergoing series of tests at U. Florida



Tests:

- Down load programs and LUTs into FPGAs and SRAMs (PASS)
- Logic tests :
  - Each subprocessor is tested individually
  - Known "patterns" are loaded into buffer, send through subprocessor, compare the output from subprocessor with the results from simulation



  - Send track segments from $\sim$ 100k single muon and triple muon events through both hardware and software simulation. Get similar results in both.
  - Test each subprocessor at 40 MHz rate

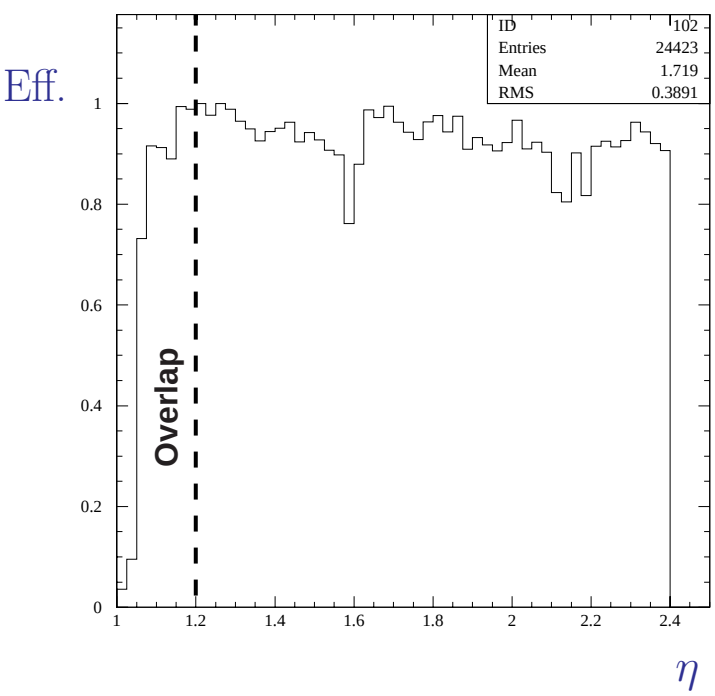
Summary of Tests

Subprocessor	Logic Test	Logic Test at 40 MHz
EU	PASS	PASS
TAU	PASS	PASS
FSU		
AU		

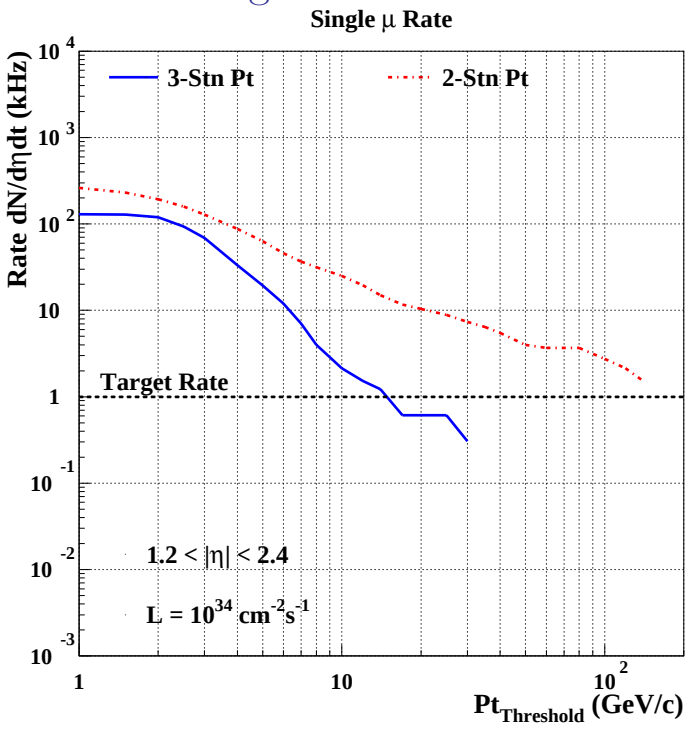
Table 1:

Simulation Results on the Prototype:

Efficiency of finding single track



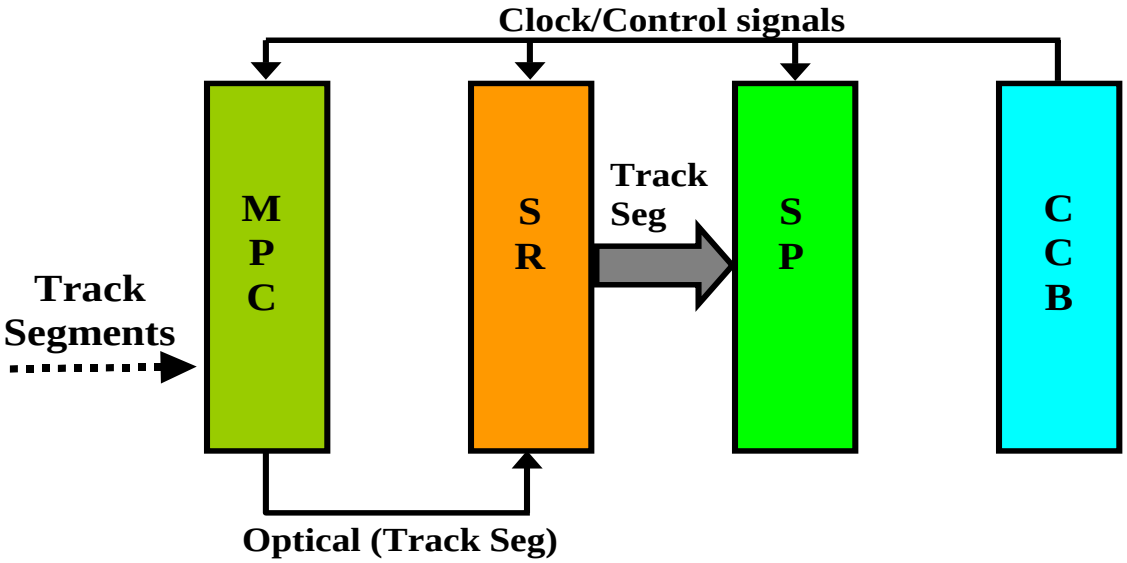
Single Muon Rate



- High single track finding efficiency
- Can achieve the target single muon trigger rate with 3 station P_t measurement

Future Tests:

- Test with other CSC electronic trigger prototypes
  - These tests will be conducted at Florida in August



Summary

- A Track-Finder Processor prototype for CMS has been built and tested
- Uses 3-D algorithm to find tracks
- Processor is driven at 40 MHz, overall latency is 400 ns
- Each Sector Processor handles trigger region $1.04 < \eta < 2.4$, $\Delta\phi = 60°$
- Measure momenta of the best track candidates from the sagitta measured between 2 or 3 muon chambers in the endcap fringe field
- Track finding algorithm is fully re-programmable, since the logics is mainly implemented in FPGAs and SRAMs
- Initial tests indicate that the prototype is performing according to design