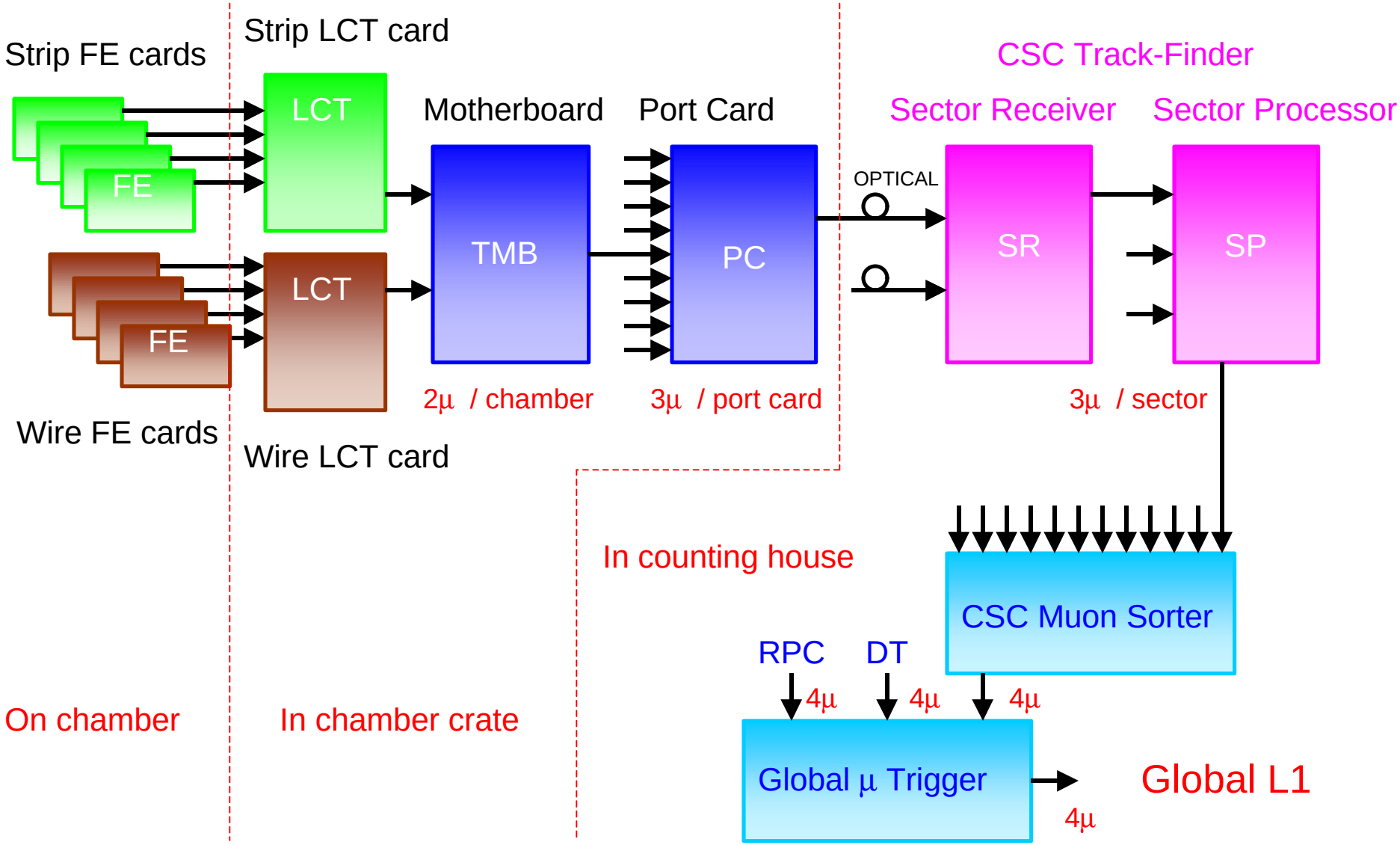
The CSC Track-Finding Processor

D.Acosta

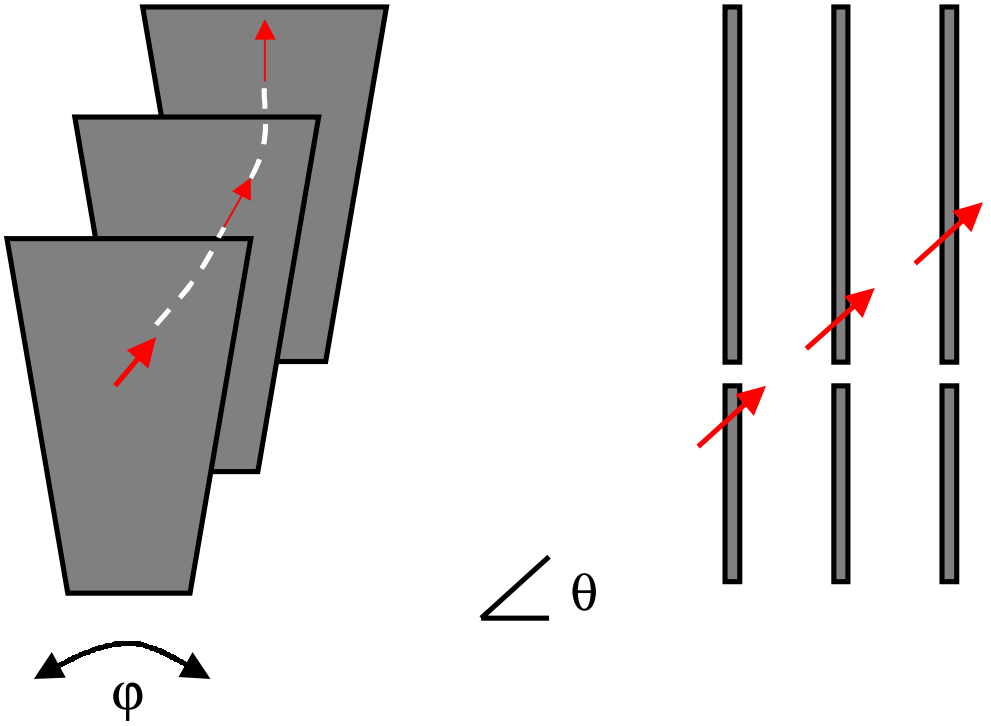
University of Florida

CSC Muon Trigger Scheme



Muon Track-Finding

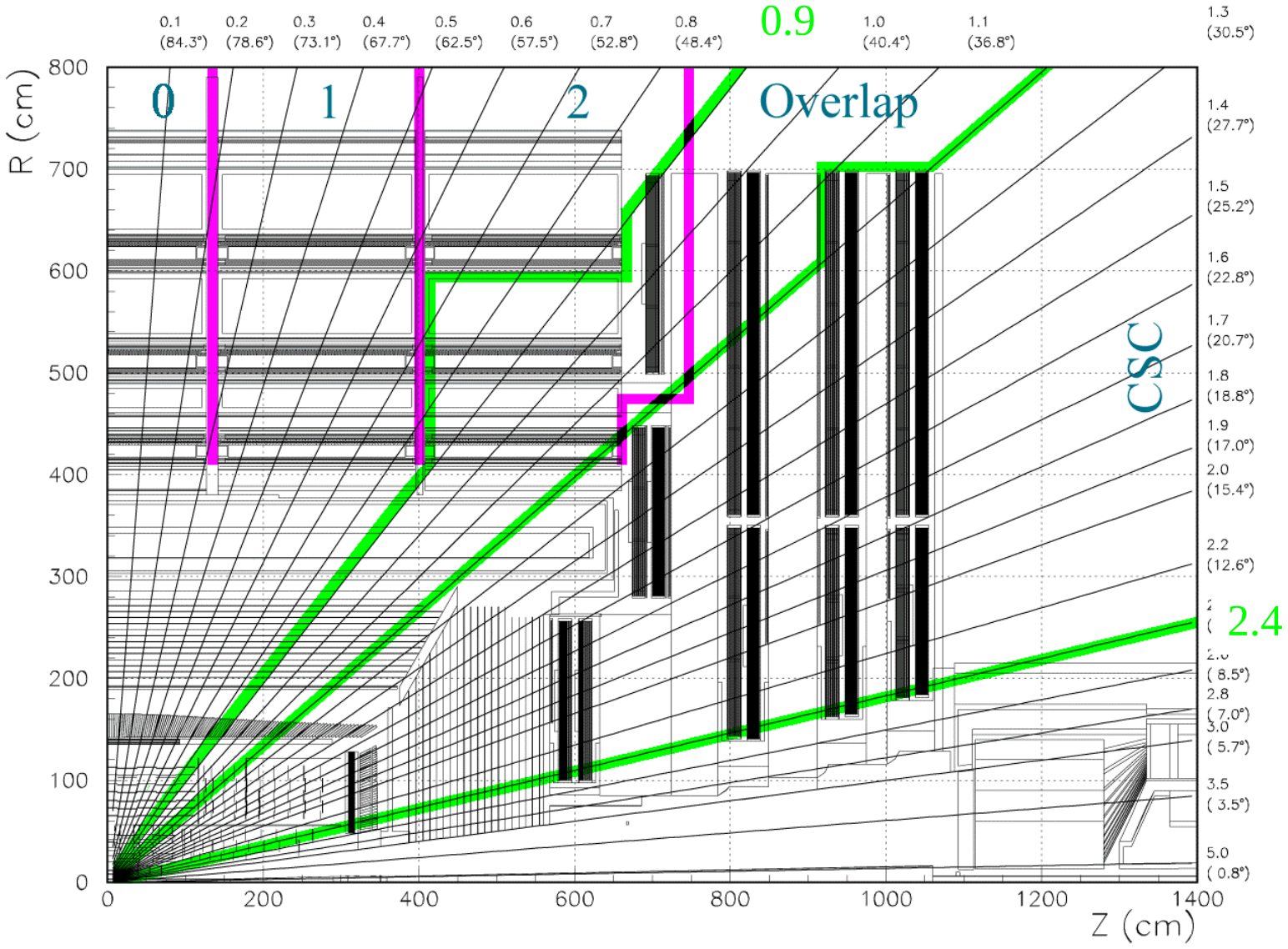
- Link trigger primitives into tracks
- Assign P_T, φ, and η
- Send highest P_T candidates to Global L1 trigger



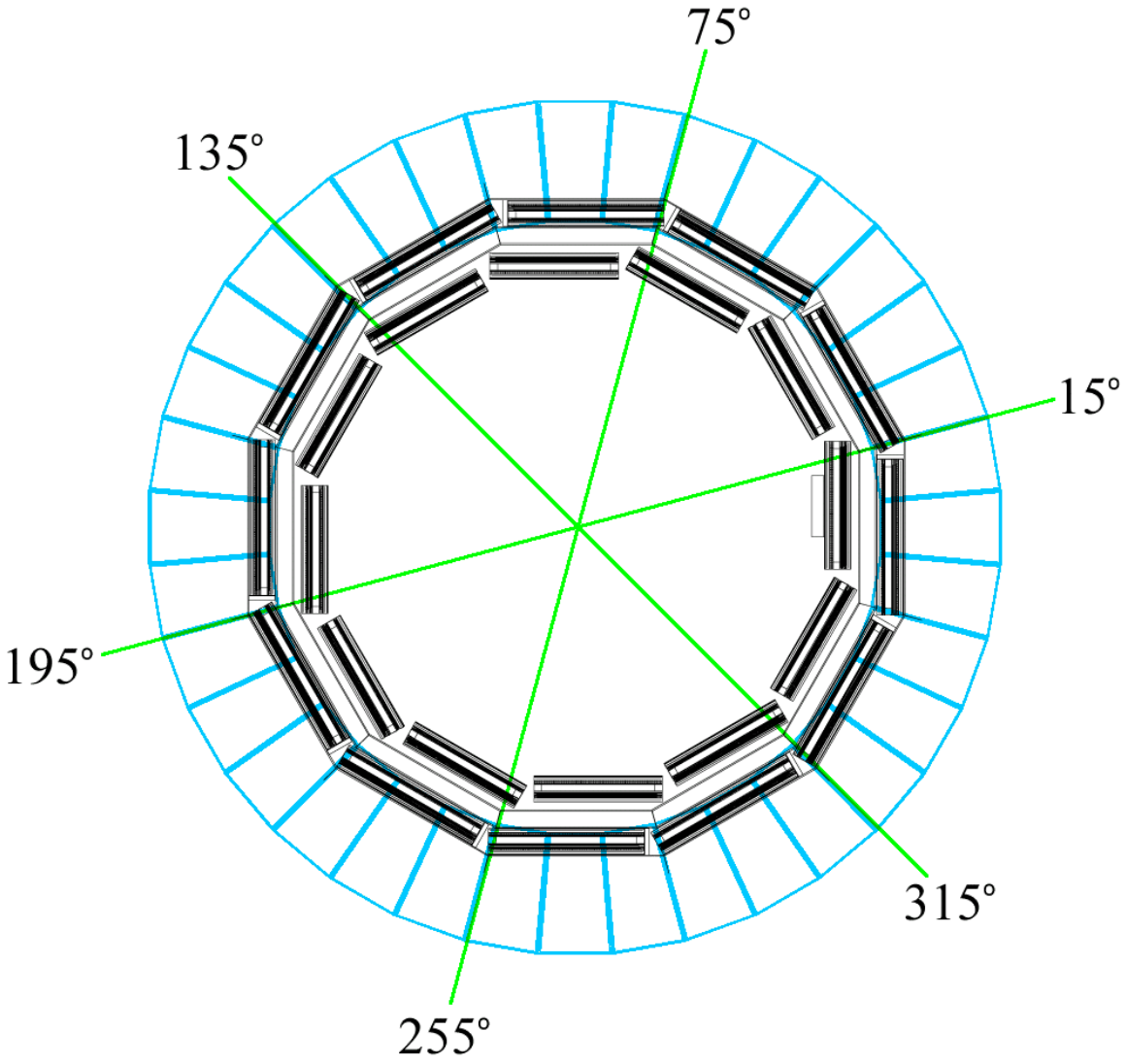
CSC Track-Finder Requirements

- Trigger Rate: Single muon rate < few kHz at $L = 10^{34}cm^{-2}\ s^{-1}$
- Resolution: $\sigma_{Pt} / P_t \leq 30\%$ (*Requires* η *information*)
- Threshold: $P_t > 3$ GeV
- Selection: ≤ 3 muons per 60° sector
- Redundancy: Require 2 stations out of 3 or 4
- Latency: ≤ 16 b.x. for Sector Processor
- Pipelined
- High Efficiency
- Programmable
- Test features

Trigger Regions in η



Trigger Regions in φ



Track Segments per Sector

Region	Station	Chamber	Segments per sector	No. of φ sectors	No. of segments	Extrap-olations
CSC	1	ME1	3	2	6	81
	2	ME2	3	1	3	
	3	ME3	3	1	3	
	4	ME4	3	1	3	
OVL	1	MB1	2	2	4	106
	2	MB2	2	2	4	
	3	ME1	3	2	6	
	4	ME2	3	1	3	

- Neighbors in φ are not considered:
  - CSC chambers project in φ
  - $\Delta\varphi_{12} < 3°$ for $P_T > 10$ GeV
- Neighbors in η do not exist

Differences between CSC and DT Track-Finders

- No neighbor input for CSC T-F implies
  - Fewer extrapolations
  - Less data input
  - Fewer signals to fan out
  - Less opportunity for two tracks to arise from one muon

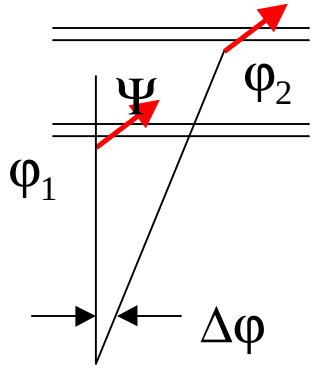
- Inclusion of η in CSC T-F allows
  - Precise P_T assignment in endcap
  - Track-Finding in 3 dimensions
  - Rate reduction

- *Therefore, CSC T-F is fundamentally different than DT T-F*

- Coverage of overlap region in CSC T-F complements approach taken by DT T-F

Required Precision of Data

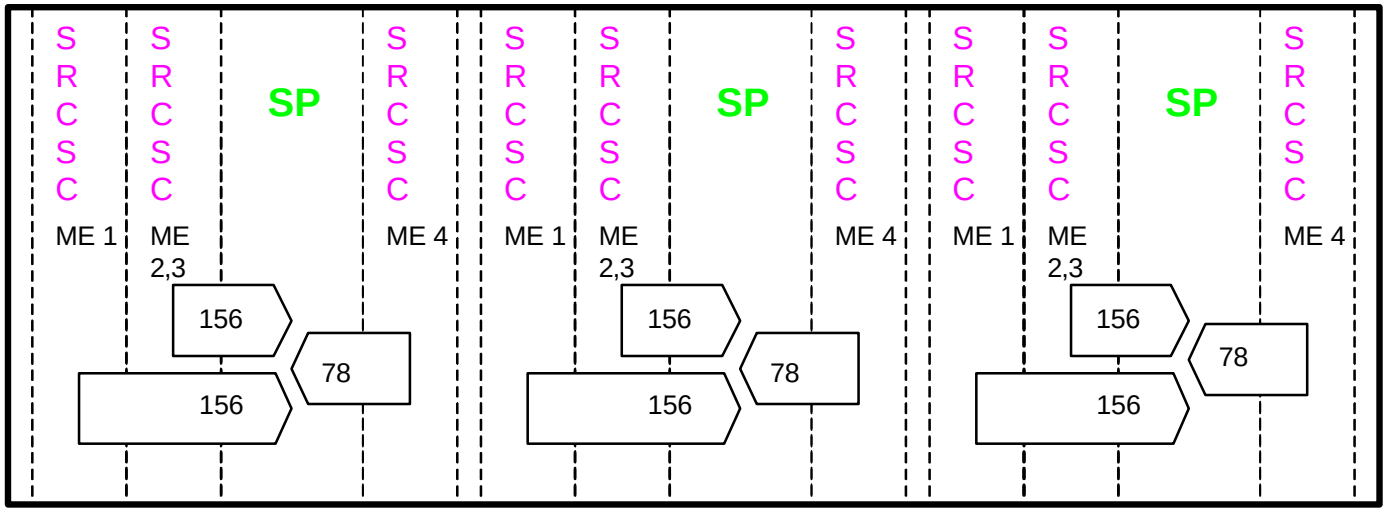
- Azimuthal angle φ:
  - 12 bits / 60° ⇒ 1 bit / 0.26 mrad (0.1 strip)
- Bend angle Ψ:
  - 6 bits / ±45° ⇒ 1 bit / 60 mrad
- Polar angle η:
  - B-field variation < ±3% for 0.05 unit bins
  - 5 bits / 1.5 units ⇒ 1 bit / 0.05
- Quality:
  - 3 bits
- Full precision needed for P_T assignment only, not extrapolation
  - e.g. φ : 7 bits Δφ : 6 bits



Inputs to CSC Sector Processor

- 1 CSC stub = 12 φ bits + 6 Ψ bits + 5 η bits + 3 Q bits = 26 bits
- 1 Port Card sends 3 stubs
- 1 Sector Receiver accepts 2 Port Cards = 6 stubs
- 1 Sector Processor accepts 6 + 3 + 3 + 3 = 15 stubs (divided between 2.5 Sector Receivers)
- 15 stubs × 26 bits = 390 bits

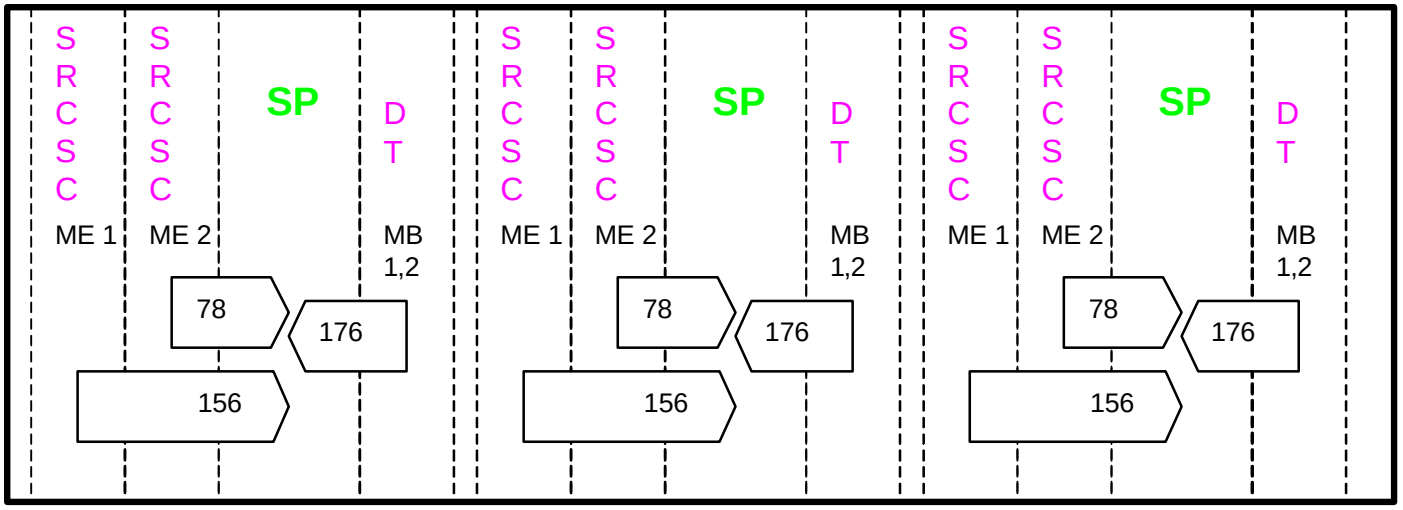
CSC crate: 9U VME with custom point-to-point backplane for last 3U



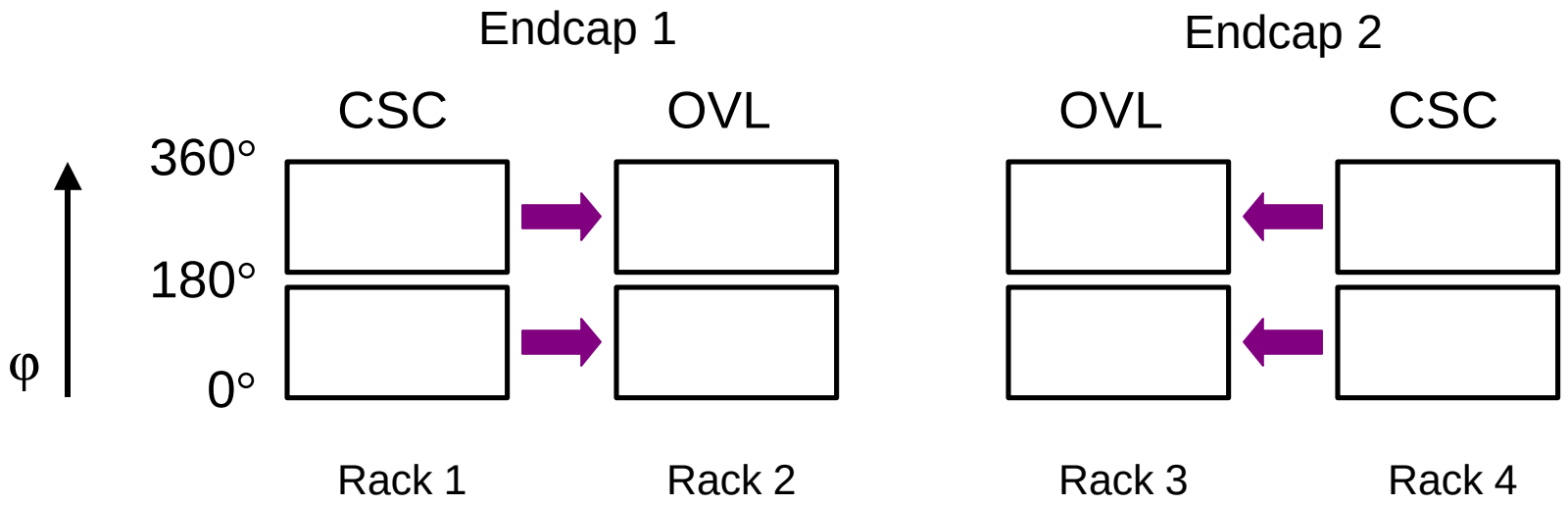
Inputs to OVL Sector Processor

- 1 CSC stub = 26 bits
- 1 DT stub = 11 φ bits + 8 Ψ bits + 3 Q bits = 22 bits
- 1 Sector Processor accepts 4+4 DT stubs and 6+3 CSC stubs
- (8 DT stubs × 22 bits) + (9 CSC stubs × 26 bits) = 410 bits
- DT stubs sent from DT trigger fan-out unit

OVL crate: 9U VME with custom point-to-point backplane for last 3U



CSC Track-Finder Crate Organization



CSC Counting House electronics:

Racks: 4

Crates: 8 (including power supply, controller, CCC)

Sector Processors: 24

Sector Receivers: 48

Muon Sorter: 1

Sector Receiver Functionality

- Receives 6 stubs via optical links from 2 Port Cards
- Synchronizes the data
- Reformats the data
  - LCT bit pattern $\rightarrow \eta, \varphi, \Psi$
- Communicates to Sector Processor via custom point-to-point backplane
- Fans out signals to CSC overlap processors and sends ME1/3 signals to DT Sector Processor

Sector Processor Functionality

- Sector Processor must identify muons from ~400 bits every 25ns (2 GB/s)

1. Perform all possible station-to-station extrapolations in parallel
   Simultaneously search for roads in φ and η
2. Assemble 3- and 4-station tracks from 2-station extrapolations
3. Cancel redundant short tracks if track is 3 or 4 stations in length
4. Select the three best candidates
5. Calculate P_T, φ, η and send to CSC muon sorter:

Quantity	Precision
η	6 bits
φ	8 bits
Muon sign	1 bit
P_T	5 bits (nonlinear)
Quality	2 bits

Sector Processor Block Diagram

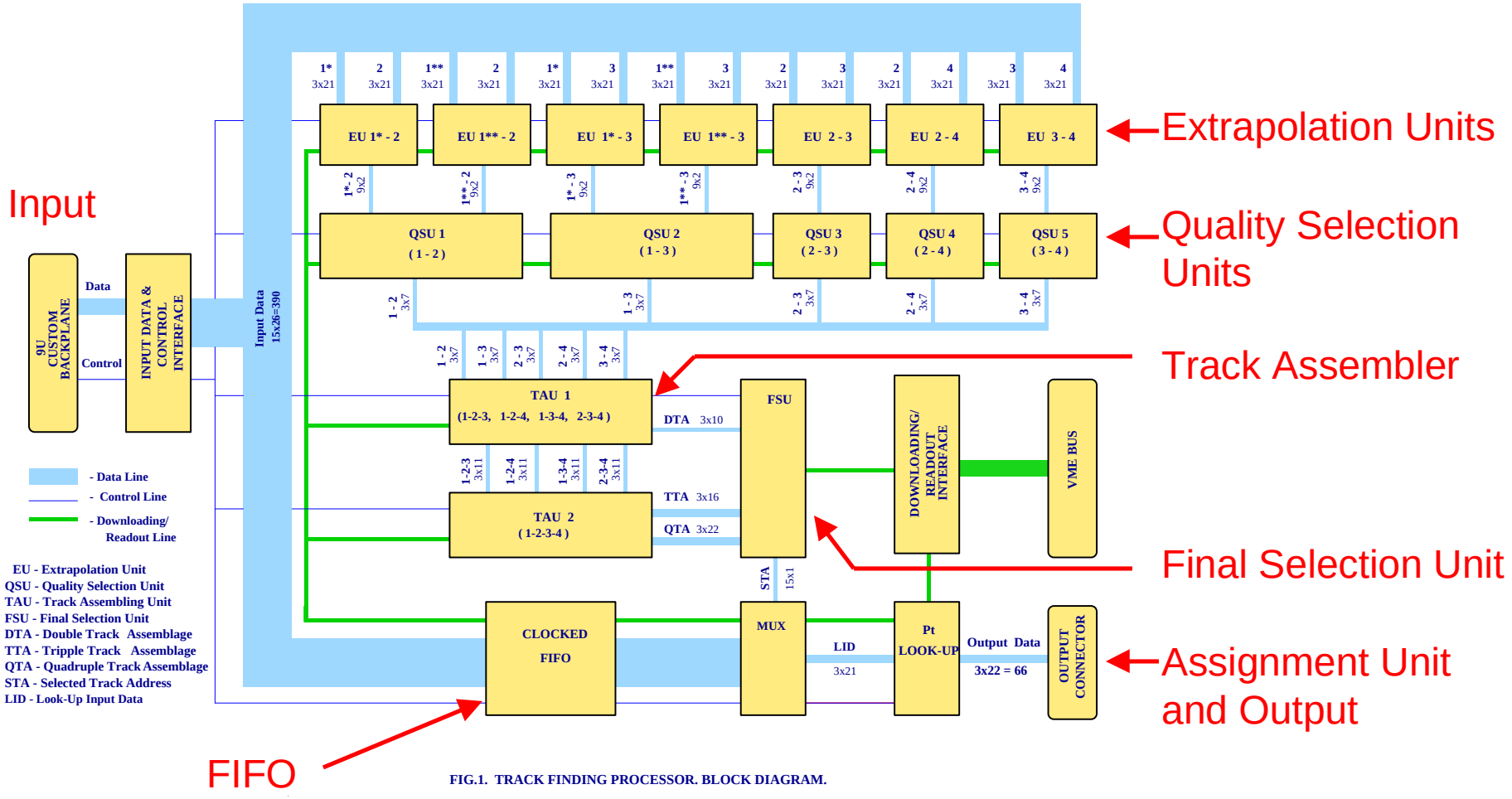
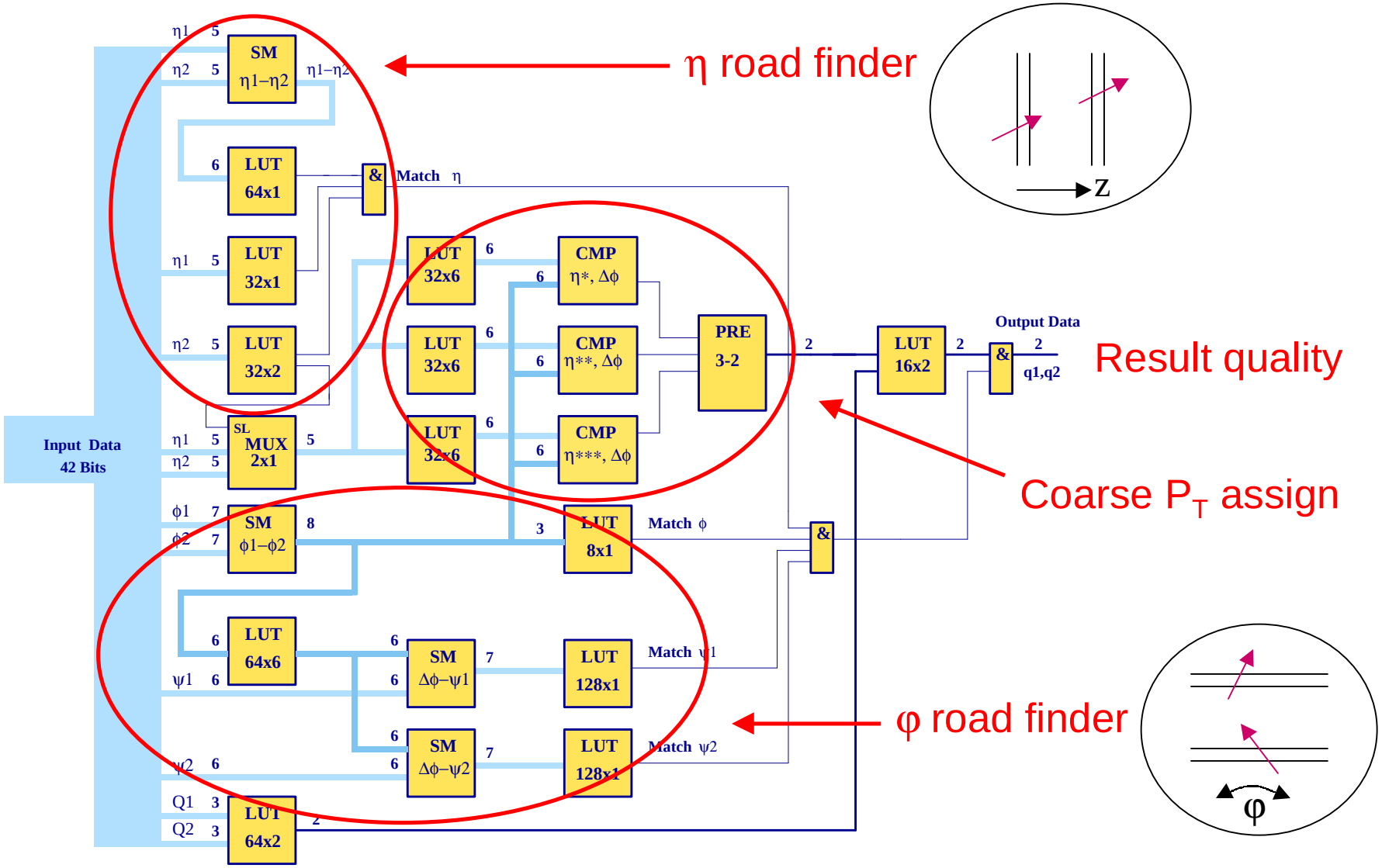


FIG.1. TRACK FINDING PROCESSOR. BLOCK DIAGRAM.

NOVEMBER, 2nd.

Extrapolation Unit Detail



Implementation Technology

- Sector Processor logic to be implemented in FPGAs and RAM
- Attempt to run some logic at 80 MHz
- Study of Xilinx FPGA implementation of Extrapolation Unit only:
  - Small number of chips needed for extrapolation (3)
  - Number of I/O pins needed per chip under control (~250)
  - Logic size under control (~60K gates)
  - No external RAM needed
  - Routing resources inside chip limits minimum chip size
- Complication of η dependence for P_T assignment under control $\Rightarrow$

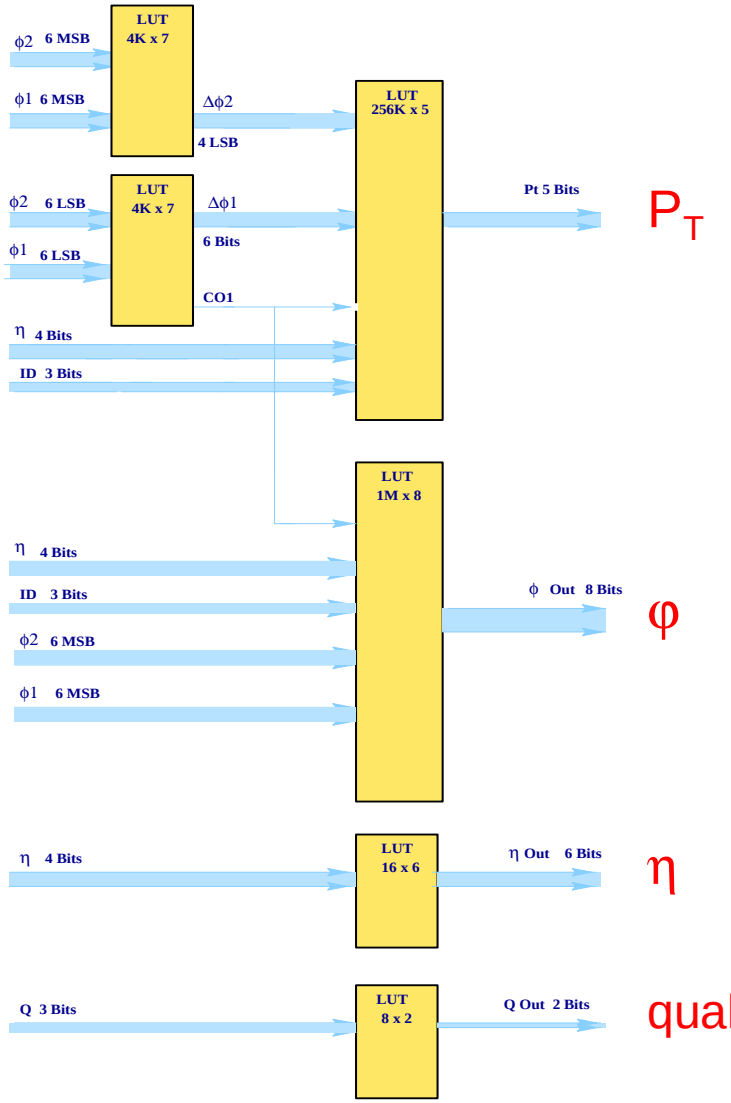
Assignment Unit

φ_1

φ_2

η

Station I.d.



P_T

φ

η

quality

Clock RAMs at 80 MHz
$\Rightarrow$ 1 b.x. delay only

CSC Muon Sorter

- The three highest rank muons from each Sector Processor are sent to the *CSC muon sorter,* which then selects the four highest rank overall

- Total muon count:
  - 3 muons $\times$ 6 sectors $\times$ 2 endcaps = 36 muons for CSC only
  - $\times$ 2 = 72 muons for CSC and OVL regions
- For comparison, the DT muon sorter accepts 24 muons

- Sort is based on 7 bits (5 bits for P_T and 2 bits for quality)

- One sorter card is necessary for entire CSC+OVL

Milestones / Schedule

- √ D387 – 1999 Mar, Sector Receiver Initial System Design
- √ D331 – 1999 Mar, Sector Processor Initial System Design
- D390 – 1999 Sep, Sector Receiver Prototype Design
- D332 – 1999 Sep, Sector Processor Prototype Design
- D391 – 2000 Jan, Sector Receiver Prototype
- D334 – 2000 Jan, Sector Processor Prototype
- D335 – 2000 Apr, Sector Receiver / Processor Crate Test
- Dnnn – 2001 Sep, Sector Receiver Final Design
- Dnnn – 2002 Apr, Sector Processor Final Design
- Dnnn – 2003 May, Sector Receiver Produced
- Dnnn – 2003 Aug, Sector Processor Produced
- Dnnn – 2003 Oct, Sector Receiver Installed
- Dnnn – 2004 Jan, Sector Processor Installed
- Dnnn – 2004 Sep, Trigger System Tested

Documentation

- Can be found at:
  - http://www.phys.ufl.edu/~acosta/cms/trigger.html
- Includes more detailed design descriptions and some simulation results