CSC Track-Finder
HW/SW Update

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New Track-Finder Crate Design

- Single Track-Finder Crate Design with 1.6 Gbit/s optical links

- Reduces SR/SP processing time from 21 bx (old design) to 7 bx
- Crate Power Consumption ~ 1000 W
- 16 Optical connections per SR/SP card
- Custom Backplane for SR/SP ⇔ CCB and MS connection
CSC Track Finder Backplane

Standard VME 64x J1/P1 backplane

Standard VME J2/P2 backplane

Custom GTLP 6U backplane

GTLP backplane avoids latency penalty of previous Channel-Link backplane (~3BX)

These SRSP feedthru connectors are for DT information exchange via transition board

Design Approved
Technology
same as EMU peripheral crates

Rice

Florida
DT-CSC Interface Specified

- DT/CSC transition board pinout specified
- Connector pinout to DT/CSC transition board defined
- Would like to specify DT/CSC cable pinout
- CMS IN 2002/040 released

<table>
<thead>
<tr>
<th>Signal</th>
<th>Bits/stub</th>
<th>Bits/3 stubs</th>
<th>Bits/6 stubs</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\phi$</td>
<td>12</td>
<td>36</td>
<td>72</td>
<td>Azimuth coordinate</td>
</tr>
<tr>
<td>$\eta$</td>
<td>1</td>
<td>3</td>
<td>6</td>
<td>DT/CSC region flag</td>
</tr>
<tr>
<td>Quality</td>
<td>3</td>
<td>9</td>
<td>18</td>
<td>stub quality</td>
</tr>
<tr>
<td>BXN</td>
<td>-</td>
<td>2</td>
<td>4</td>
<td>2 LSB of BXN</td>
</tr>
<tr>
<td>BC0</td>
<td>-</td>
<td>1</td>
<td>2</td>
<td>bunch crossing 0</td>
</tr>
<tr>
<td>Clock</td>
<td>-</td>
<td>1</td>
<td>2</td>
<td>clock for data</td>
</tr>
<tr>
<td>Total:</td>
<td>16</td>
<td>52</td>
<td>104</td>
<td></td>
</tr>
</tbody>
</table>

DT TF $\rightarrow$ CSC TF

CSC TF $\rightarrow$ DT TF
New Mezzanine Card has 6 Connectors - Allows > 800 I/O signals to the main FPGA

- EEPROM
- Indicators
- TLK2501 Transceiver
- Front FPGA
- DDU FPGA
- Optical Transceiver
- Phi Global LUT
- Eta Global LUT
- Phi Local LUT
- DC-DC Converter
- EEPROM
- VME/CCB FPGA
- PT LUT
- From CCB
- To Muon Sorter
- To/From Barrel
- Main FPGA
- Mezzanine Card
SR LUT Triad

FRONT FPGA

A18
A11
C3
C3
C4
CLK40P1
CLK40P2
D16
C2
C4
CLK40

PHIL LUT
256K x 18
Flow
Through
SRAM

CSC ID - 4
WG ID = 7

16 Bit
Transceiver

ETAG LUT
512K x 18
Flow
Through
SRAM

CSC_ID - 4
WG_ID - 3

16 Bit
Transceiver

PHIG LUT
512K x 36
Flow
Through
SRAM

CSC_ID - 4
WG_ID - 3

16 Bit
Transceiver

MAIN FPGA

Identical for all tracks.

Contents depend on Sector or Station

All are synchronous GSI memories. Plan to use same technology for Pt LUTs.

To DT

CLK40

Legend:  A – Address Lines
D  - Data  Lines
C – Control Lines
CLK – Clock

•SR now has 3 memories rather than 6 per stub [total of 45 per board]. Need to define their contents. LUTs are created in ORCA, but have yet to be tested.

•>64 MB per board ⇒ Need high VME bandwidth, broadcast capability to identical chips, and crate broadcast capability to SPs

CMS Week: Trigger Meeting, June 2002. B. Scurlock, University of Florida
SR/SP 2002 Design Status

- Schematics Complete:
  - Sector Receiver Front FPGAs (5 total)
    - Choice: XC2V1000-FF896C with 432 user I/Os
  - Sector Processor Main FPGA
    - Choice: XC2V4000-FF1152C with 824 user I/Os
    - Placed on mezzanine card (design started)
    - Firmware written in “Verilog++”, validated by simulation
  - VME & control interface FPGA
    - Choice: XC2V250-FG456C with 200 user I/Os
  - DAQ Interface FPGA
    - Choice: XC2V250-FG256C with 172 user I/Os
  - SRAM:
    - 51 SRAM chips (>64MB) for Look-up functionality
    - May require BGA packages to allow more space for routing
- Layout to commence soon
  - Board will be dense! (Merger of 4 boards, but I/O ~same)
Software Update

- Verilog++ SP model implemented and LUTs generated in ORCA.
- Also need to add Bunch Crossing Analyzer and Ghost Busting [background reduction] to Verilog++ model.
- Phi and Eta SR LUT Contents Have Been Specified in ORCA. [Thank You Slava Valouev!]
- Work underway to attach track-stub data to tracks in Verilog++ model and in DAQ (this will be useful for L2 Trigger).
Software Update

• Currently examining alternative bend patterns in CLCT Processor to improve $\phi$ resolution and Pt assignment.

• First attempt will be using patterns from CMSIM100 $\Rightarrow$ Bend value based only on the number of strips extended. For example:

![Diagram showing bend patterns]

- 5 half strip widths $\Psi = 5$
- 4 half strip widths $\Psi = 4$
- 3 half strip widths $\Psi = 3$
- 2 half strip width $\Psi = 2$
- 1 half strip widths $\Psi = 1$
We have started working on integrating software written for the 2000 TF crate tests into the XDAQ environment.

Screen shot of the Hardware configuration GUI.

JAVA GUI and configuration database

Command-line programs to load FPGAs and LUTs
Schedule

- **November 2002**: expect to finish the SP prototype. Will conduct single board tests

- **MPC → SR/SP** tests will continue through to 4/30/03.

- **5/1/03 to 9/30/03**: Plan chain tests with CSC chambers and front-end electronics using cosmic rays and test beam.

- Also plan to do DT↔CSC tests sometime after May 1 2003.
Conclusions

- CSC TF Backplane Specified
- DT-CSC Interface Specified
- SR/SP Schematics Complete
- SR/SP Layout Started
- SR LUT Generation Completed in ORCA
- More Additions Scheduled for Verilog++ SP Model
- Work on $\phi_b$ Definition in Progress