Topics:

- Board Layout
- Bit counts and data serialization
- Memory architecture  (PNPI)
- SP to Verilog Translation   (Madorsky)
- DDU plans
Possible Single Crate Solution

Track-Finder crate (1.6 Gbits/s optical links)

- Total latency: ~ 20Bx (from input of SR/SP card to output of CCB/MS card)
- Power consumption: ~ 500W per crate
- 15 optical connections per SR/SP card
- Custom backplane for SR/SPs < > CCB/MS connection
Merged SR/SP

15 trigger links, 1 DAQ

From trigger primitives

To CSC DAQ

Input: 528 bits/sector/b.x.

Output: 60 bits/sector/b.x.

45 SRAM

From MPC (chamber 4)
From MPC (chamber 3)
From MPC (chamber 2)
From MPC (chamber 1C)
From MPC (chamber 1B)
From MPC (chamber 1A)

Small Form Factor Transceivers

Deserializer Chips

Front FPGAs

Memory Look-up Tables

Sector Processor FPGA chip

Pt-assignment LUTs

To Muon Sorter

To/From Barrel

From Clock and Control Board

VME Interface

~45 SRAM chips
80 MHz speed

From Clock
and Control Board

To Muon Sorter

To/From Barrel

Sector Processor 2
University of California, Los Angeles
University of Florida

1 April 2001

15 trigger links, 1 DAQ

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Sector Processor 2
University of California, Los Angeles
University of Florida

1 April 2001
Salient Features

Bi-Directional Optical Links

- Since we have both transmitters and receivers in the optical connection, this allows the option to send data as well as receive.
- Makes testing much easier
  - One board sends data to other, or even itself through links.

SR memory set for each muon stub

- No muon multiplexing means shortest latency.

SP chip on a mezzanine board

- Decouples board development from FPGA technology.
- Makes upgrades easier.

DT fan-out on transition board

- Deliver all possibly needed signals to backplane connector.
- Settle transmission technology, connector type, connector count on transition board at a later date.
SR/SP Inputs

Muon Port Cards deliver 15 track stubs each BX via optical

<table>
<thead>
<tr>
<th>Signal</th>
<th>Bits / stub</th>
<th>Bits / 3 stubs (1 MPC)</th>
<th>Bits / 15 stubs (ME1-ME4)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>½ Strip *</td>
<td>8</td>
<td>24</td>
<td>120</td>
<td>½ strip label</td>
</tr>
<tr>
<td>CLCT pattern *</td>
<td>4</td>
<td>12</td>
<td>75</td>
<td>Pattern number without 4/6, 5/6, 6/6</td>
</tr>
<tr>
<td>L/R bend *</td>
<td>1</td>
<td>3</td>
<td>15</td>
<td>Sign bit for pattern</td>
</tr>
<tr>
<td>Quality *</td>
<td>3</td>
<td>9</td>
<td>45</td>
<td>Computed by TMB</td>
</tr>
<tr>
<td>Wire group</td>
<td>7</td>
<td>21</td>
<td>105</td>
<td>Wire group label</td>
</tr>
<tr>
<td>Accelerator μ</td>
<td>1</td>
<td>3</td>
<td>15</td>
<td>Straight wire pattern</td>
</tr>
<tr>
<td>CSC i.d.</td>
<td>4</td>
<td>12</td>
<td>60</td>
<td>Chamber label in subsector</td>
</tr>
<tr>
<td>BXN</td>
<td>2</td>
<td>6</td>
<td>30</td>
<td>2 LSB of BXN</td>
</tr>
<tr>
<td>Valid pattern</td>
<td>1</td>
<td>3</td>
<td>15</td>
<td>Must be set for above to apply</td>
</tr>
<tr>
<td>Spare</td>
<td>1</td>
<td>3</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>Total:</td>
<td>32</td>
<td>96</td>
<td>480</td>
<td>(240 bits at 80 MHz)</td>
</tr>
</tbody>
</table>

Sent on first frame

Reduced from 5

Needed for frame info

DT Track-Finder delivers 2 track stubs each BX via LVDS

<table>
<thead>
<tr>
<th>Signal</th>
<th>Bits / stub</th>
<th>Bits / 2 stubs (MB1: 60°)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>φ</td>
<td>12</td>
<td>24</td>
<td>Azimuth coordinate</td>
</tr>
<tr>
<td>φb</td>
<td>5</td>
<td>10</td>
<td>φ bend angle</td>
</tr>
<tr>
<td>Quality</td>
<td>3</td>
<td>6</td>
<td>Computed by TMB</td>
</tr>
<tr>
<td>BXN</td>
<td>2</td>
<td>4</td>
<td>2 LSB of BXN</td>
</tr>
<tr>
<td>Synch/Calib</td>
<td>1</td>
<td>2</td>
<td>DT Special Mode</td>
</tr>
<tr>
<td>Muon Flag</td>
<td>1</td>
<td>2</td>
<td>2nd muon of previous BX</td>
</tr>
<tr>
<td>Total:</td>
<td>24</td>
<td>48</td>
<td></td>
</tr>
</tbody>
</table>
# SR/SP Outputs

- 6 track stubs are delivered to DT Track-Finder each BX (delivered at 40 MHz to transition board)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Bits / stub</th>
<th>Bits / 2 stubs (ME1: 20°)</th>
<th>Bits / 6 stubs (ME1: 60°)</th>
<th>Bits / 6 stubs @ 80 MHz</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\phi$</td>
<td>12</td>
<td>24</td>
<td>72</td>
<td>36</td>
<td>Azimuth coordinate</td>
</tr>
<tr>
<td>$\eta$</td>
<td>1</td>
<td>2</td>
<td>6</td>
<td>3</td>
<td>DT/CSC region flag</td>
</tr>
<tr>
<td>Quality</td>
<td>3</td>
<td>6</td>
<td>18</td>
<td>9</td>
<td>Computed by TMB</td>
</tr>
<tr>
<td>BXN</td>
<td>–</td>
<td>2</td>
<td>6</td>
<td>3</td>
<td>2 LSB of BXN</td>
</tr>
</tbody>
</table>

16 34 102 51 Total

- 3 muons per SP are delivered to Muon Sorter via GTLP backplane

<table>
<thead>
<tr>
<th>Signal</th>
<th>Bits / $\mu$</th>
<th>Bits / 3 $\mu$ (1 SP)</th>
<th>Bits / 36 $\mu$ (12 SP)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\phi$</td>
<td>5</td>
<td>15</td>
<td>180</td>
<td>Azimuth coordinate</td>
</tr>
<tr>
<td>$\eta$</td>
<td>5</td>
<td>15</td>
<td>180</td>
<td>Pseudorapidity</td>
</tr>
<tr>
<td>Rank *</td>
<td>7</td>
<td>21</td>
<td>252</td>
<td>5 bits $p_T$ + 2 bits quality</td>
</tr>
<tr>
<td>Sign *</td>
<td>1</td>
<td>3</td>
<td>36</td>
<td></td>
</tr>
<tr>
<td>BXN *</td>
<td>–</td>
<td>2</td>
<td>24</td>
<td>2 LSB of BXN</td>
</tr>
<tr>
<td>Error *</td>
<td>–</td>
<td>1</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Spare *</td>
<td>1</td>
<td>3</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Total:</td>
<td>19</td>
<td>60</td>
<td>720</td>
<td>(360 bits at 80 MHz)</td>
</tr>
</tbody>
</table>

Sent on first frame
## SR/SP Internal Dataflow

Data delivered from SR to SP

<table>
<thead>
<tr>
<th>Signal</th>
<th>Bits / stub</th>
<th>Bits / 6 stubs (ME1)</th>
<th>Bits / 15 stubs (ME1–ME4)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\phi)</td>
<td>12</td>
<td>72</td>
<td>180</td>
<td>Azimuth coordinate</td>
</tr>
<tr>
<td>(\phi_b)</td>
<td>5</td>
<td>30</td>
<td>75</td>
<td>(\phi) bend angle</td>
</tr>
<tr>
<td>(\eta)</td>
<td>6</td>
<td>36</td>
<td>90</td>
<td>Pseudorapidity</td>
</tr>
<tr>
<td>Accelerator (\mu)</td>
<td>1</td>
<td>6</td>
<td>15</td>
<td>(\eta) bend angle</td>
</tr>
<tr>
<td>Front/Rear *</td>
<td>1</td>
<td>6</td>
<td>6</td>
<td>ME1 chamber stagger</td>
</tr>
<tr>
<td>CSC ghost *</td>
<td>–</td>
<td>4</td>
<td>4</td>
<td>2 stubs in same ME1 CSC</td>
</tr>
<tr>
<td>Quality</td>
<td>3</td>
<td>18</td>
<td>45</td>
<td>Computed by TMB</td>
</tr>
<tr>
<td>Total:</td>
<td>28</td>
<td>172</td>
<td><strong>415</strong></td>
<td>(sent at 80 MHz)</td>
</tr>
</tbody>
</table>
Old SR Memory Scheme

SR Look-Up Tables
Six 256K x 16 RAMs

Now in TMB
New SR Memory Scheme

Don’t need “muon #” if not multiplexing muons

Same memory with 24 output bits
Discussion of SR Memory (1)

Data Frames:

- Data arrives off links @ 80 MHz
- The proposed framing scheme implies no latency loss
  - First LUT operates on first frame only
    (but must reduce CLCT pattern label by 1 bit)
- This frame definition must be applied in the TMB where the data is generated and first serialized (i.e. before MPC) to avoid latency penalty

Memories:

- LUT for DT only applies to ME1
- Chip count is 3 per stub, down from 6 originally
- Increased memory size to 0.5M (okay for synch. SRAM)
- "Muon #" only applies if more than one stub in a BX is sent through same memory
Discussion of SR Memory (2)

One memory set per stub:
- \(15 \times 3 = 45\) chips
- 1 BX latency
- 415 signals to SP

First SR had 36 chips and 1 BX latency

Memory choices:
- synch SRAM clocked at 160 MHz (tested to this frequency)
- Flow Through SRAM clocked at 80 MHz (see PNPI)
Must serialize to fit data on backplane
- No latency penalty for serialization if Rank sent first to Muon Sorter
- SP FPGA contains tri-state buffers and generates enable for memories

\[ \Delta \phi_{23} \] could be replaced by \( \phi_b \)

Added F/R bit to improve \( P_T \) resolution
SP to Verilog translation

What we said last time:

Will overhaul some of the SP software/firmware to facilitate changes to both

- Have SW algorithms match Verilog/Schematics better
- Have SW read same HW LUTs (it already generates them)

Plan to test next SP design even before construction!

- Add utilities to write ORCA data into Xilinx simulator format and to compare simulator output to ORCA
- Gives us a head start on validating logic design
- Will allow us to focus on HW debugging rather than SW debugging when testing the next prototype

This is now done! Latency: 12 $\rightarrow$ 5 BX (See Madorsky)
CSC TF DAQ Plans

Send input of SR and output of SP to DAQ stream for diagnostics

Track-Finder DAQ acts as additional DDU for EMU system

- Plan to use existing DDU design by OSU
  - OSU has decided to use T.I. Chip for serialization
  - 12 SP fiber connections fits well into 15 planned for DDU
  - (Don’t even need separate links as ours are bi-directional)

Next step is to have Lev work with OSU (Jason Gilmore) to learn their design

- Check bandwidth and buffer limitations
- Understand how to format our data
- Design buffers and readout on SR/SP
OSU now plans 20° slices to equalize bandwidth.

Sector Processors send L1 data.

DDU designed by Ohio State Univ.

CSC DDU

Linux CPU

Gigabit Ethernet fiber

10 Mbit Ethernet Cat 5

15 optical fibers

Peripheral Crates

Peripheral Crates

9 DAQMB’s

9 G-Link fibers

CCB, LV1, ...

ERRORs

SLINK

36

SLINK

+ 1 (2?)