Status of the CSC Track-Finder

Darin Acosta

University of Florida

May 2000

Outline

Overview of the CSC trigger system

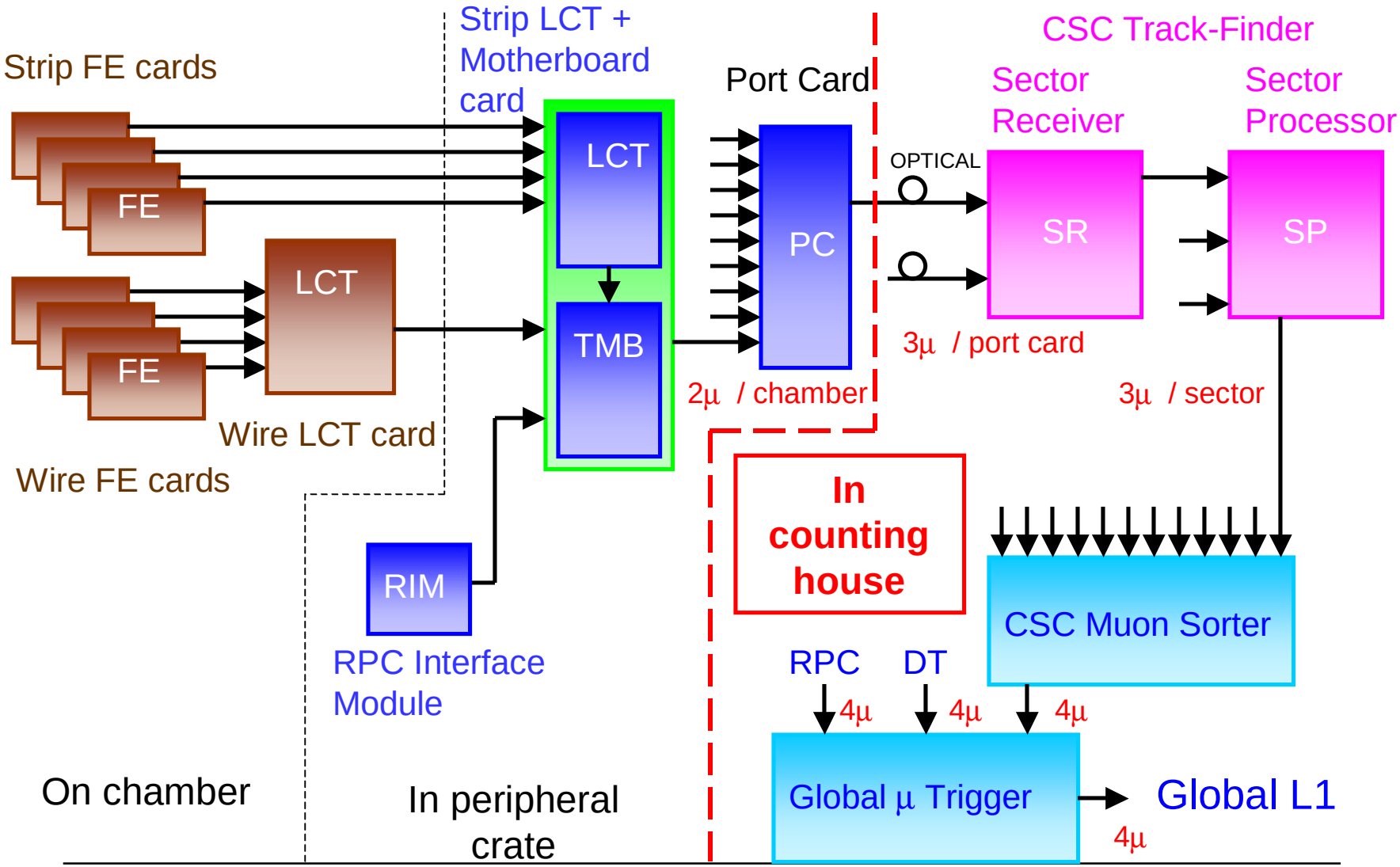
Sector Receiver

Sector Processor

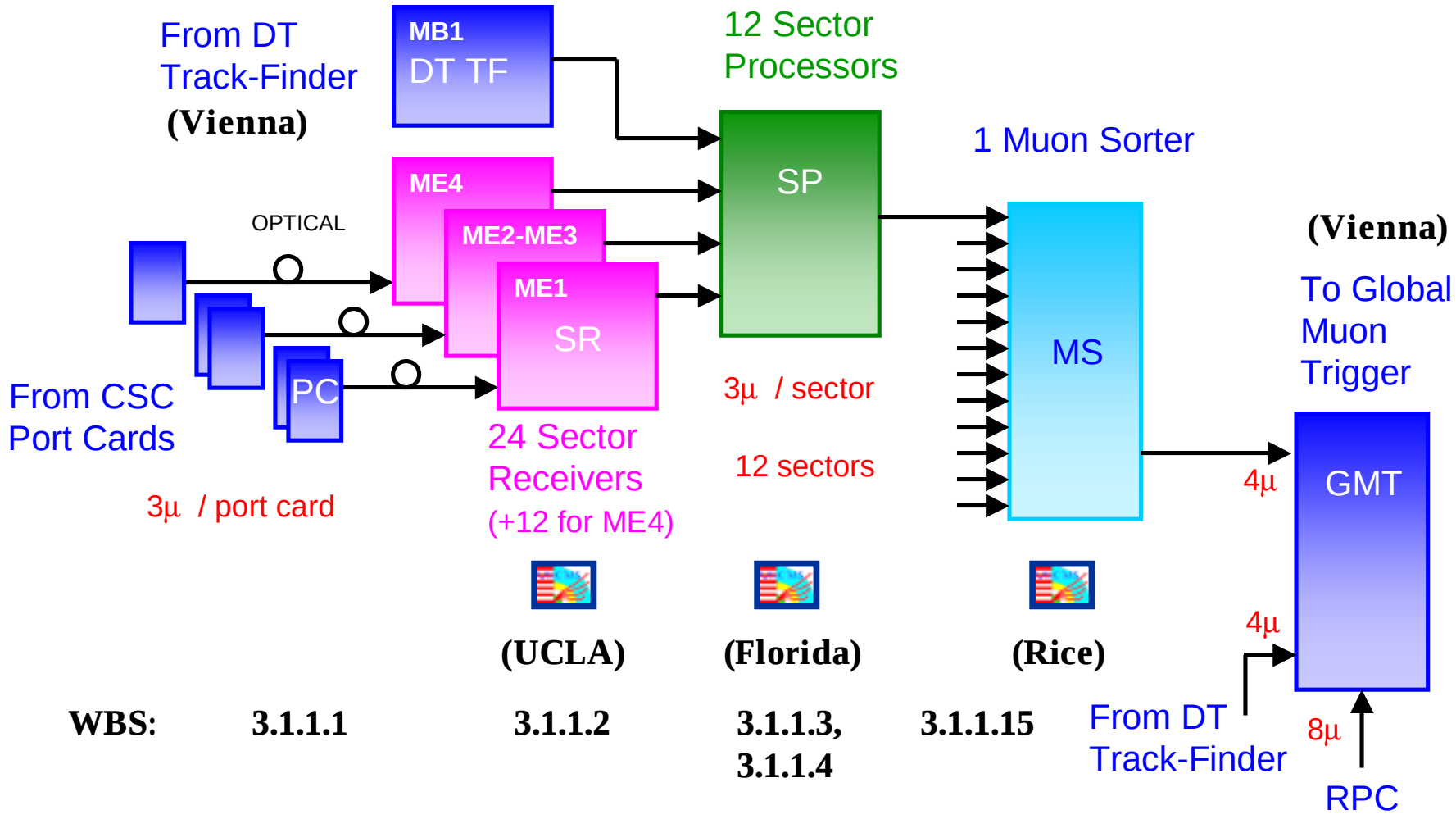
Muon Sorter

CSC/DT Interface

CSC Muon Trigger Scheme



The CSC Track-Finder



Sector Receiver Functionality

UCLA

3.1.1.2

1. **Receive 6 μ segments via 12 optical links from 2 Muon Port Cards**
   - Require 3 Sector Receivers for one 60° sector
2. **Synchronize the data**
3. **Reformat the data into track segment variables**
   - LCT bit pattern $\rightarrow \eta, \varphi, \varphi_b$, ...

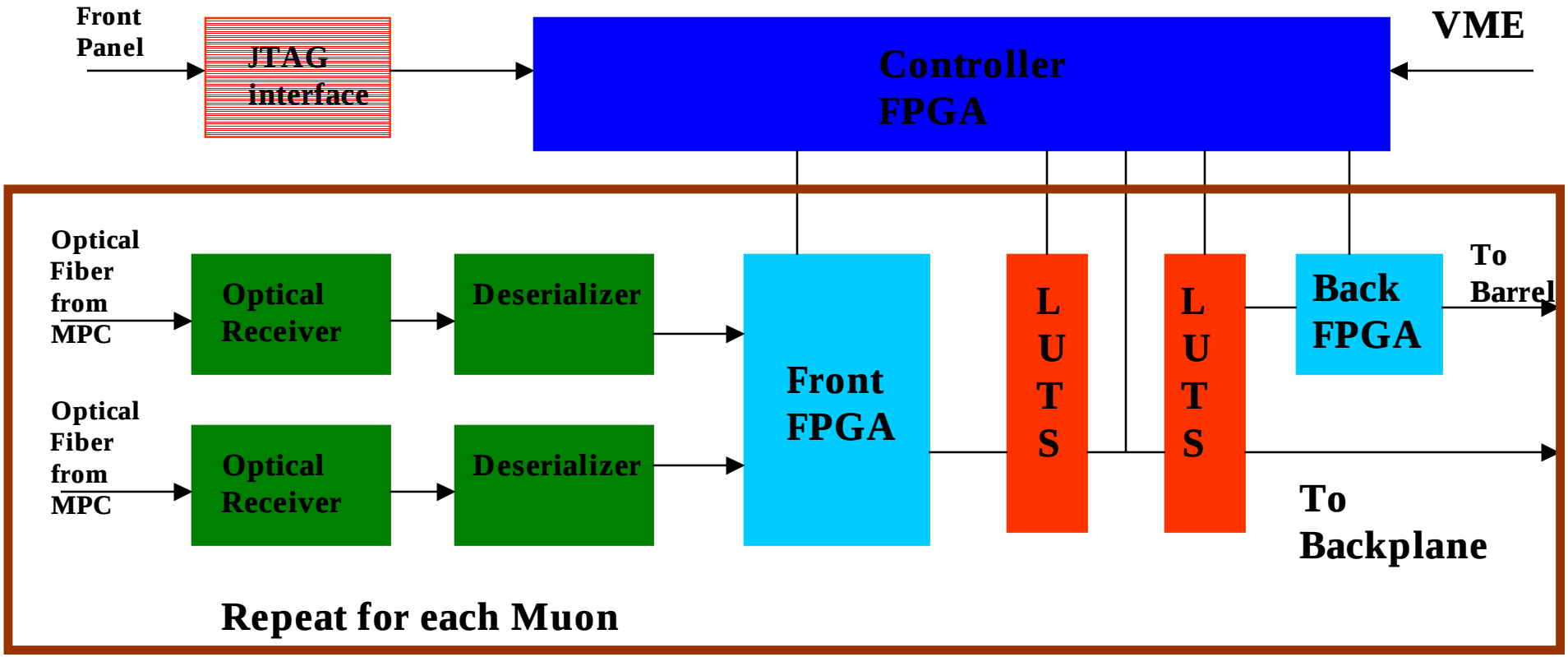
} **via LUTs**

4. **Apply corrections for alignment**
5. **Communicate to Sector Processor via custom backplane (Channel Link)**
6. **Fan out ME1/3 μ segments to DT Track-Finder**

Sector Receiver Logic

UCLA

3.1.1.2

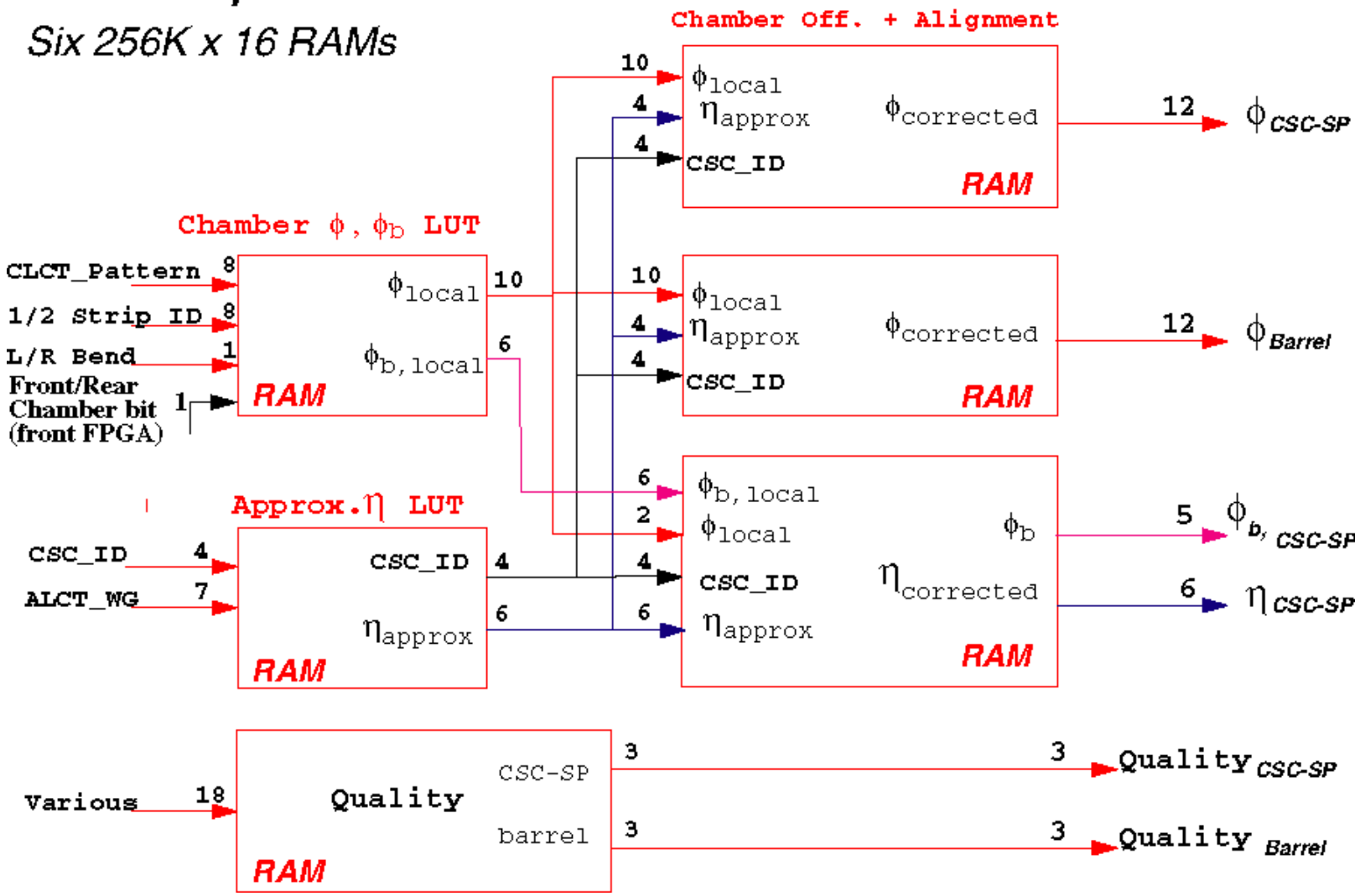


Sector Receiver LUT Scheme

UCLA

SR Look-Up Tables

Six 256K x 16 RAMs



Sector Receiver

UCLA

3.1.1.2

- **Fell behind schedule after postdoc departure.**
- **Personnel added in December/January:**
  - **Robert Cousins, physicist, 50% time**
  - **Vladislav Sedov, electronics engineer, 90% time**
    (10% residual work on ALCT board)
  - **Also using paid consultant for some FPGA work**
    (UCLA CS Ph.D. candidate)
- **Schematics now well underway.**
- **Long-lead-time parts ordered.**
- **Layout planned by beginning of May.**
- **Plan to be ready for summer Track Finder test.**

Sector Processor Functionality

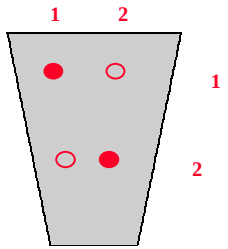
Florida

3.1.1.3, 3.1.1.4

1. **Accumulate** track segments for possibly more than one B.X.
2. **Extrapolate** in 3D from one station to another for all possible track segment combinations
3. **Assemble** tracks from extrapolation results
4. **Select** best 3 tracks and cancel ghosts
5. **Assign** track parameters: p_T, φ, η, quality

New since last Review:

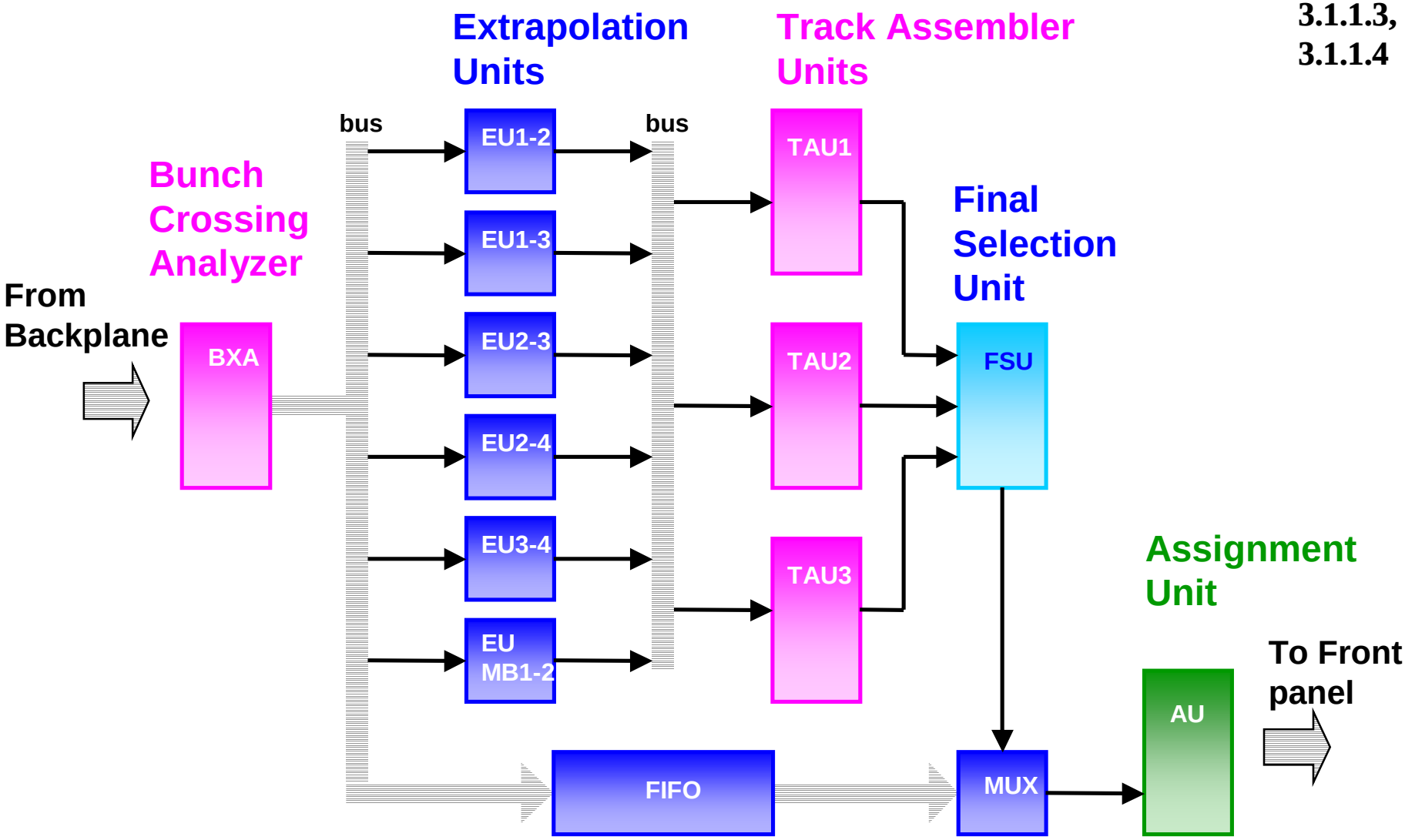
- **Combined DT/CSC overlap region onto same board as CSC-only region (add MB1–ME2 extrap.)**
- **Improved P_T assignment technique**
- **Ghost-busting when 2 muons enter 1 CSC chamber (try all combinations)**



Sector Processor Logic

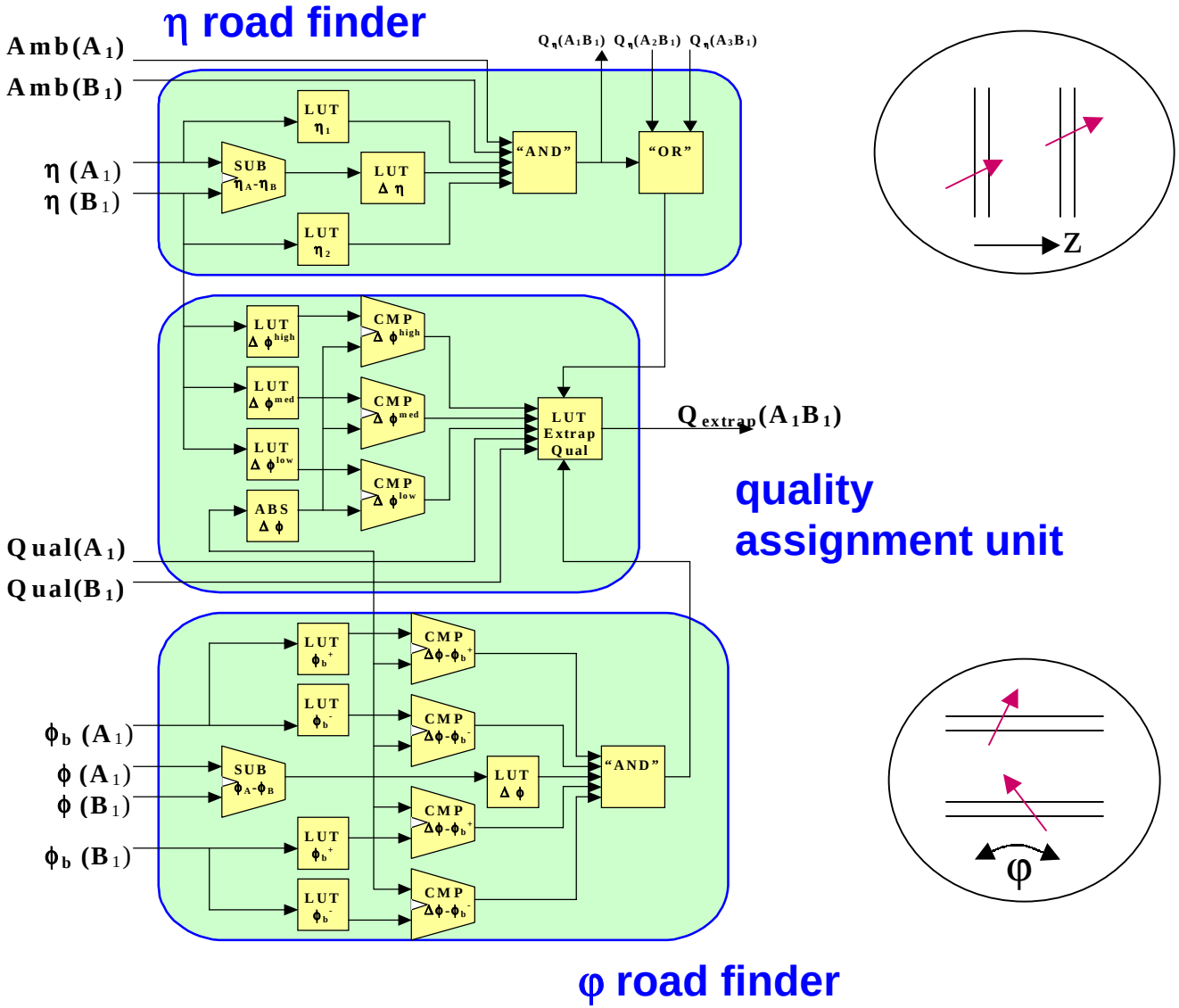
Florida

3.1.1.3,
3.1.1.4



Extrapolation Logic

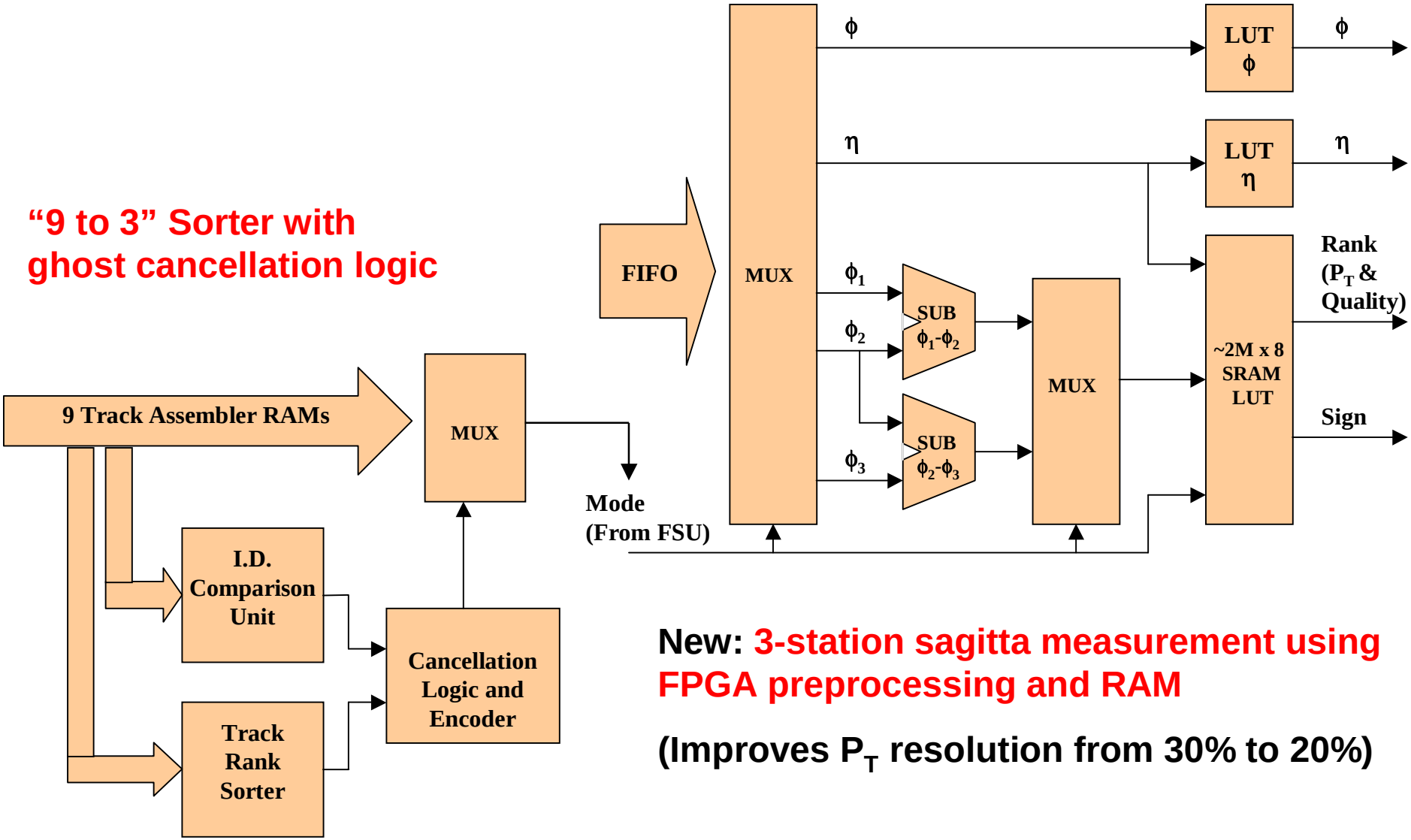
Florida



Track Selection and P_T Assignment

Florida

"9 to 3" Sorter with ghost cancellation logic



New: 3-station sagitta measurement using FPGA preprocessing and RAM

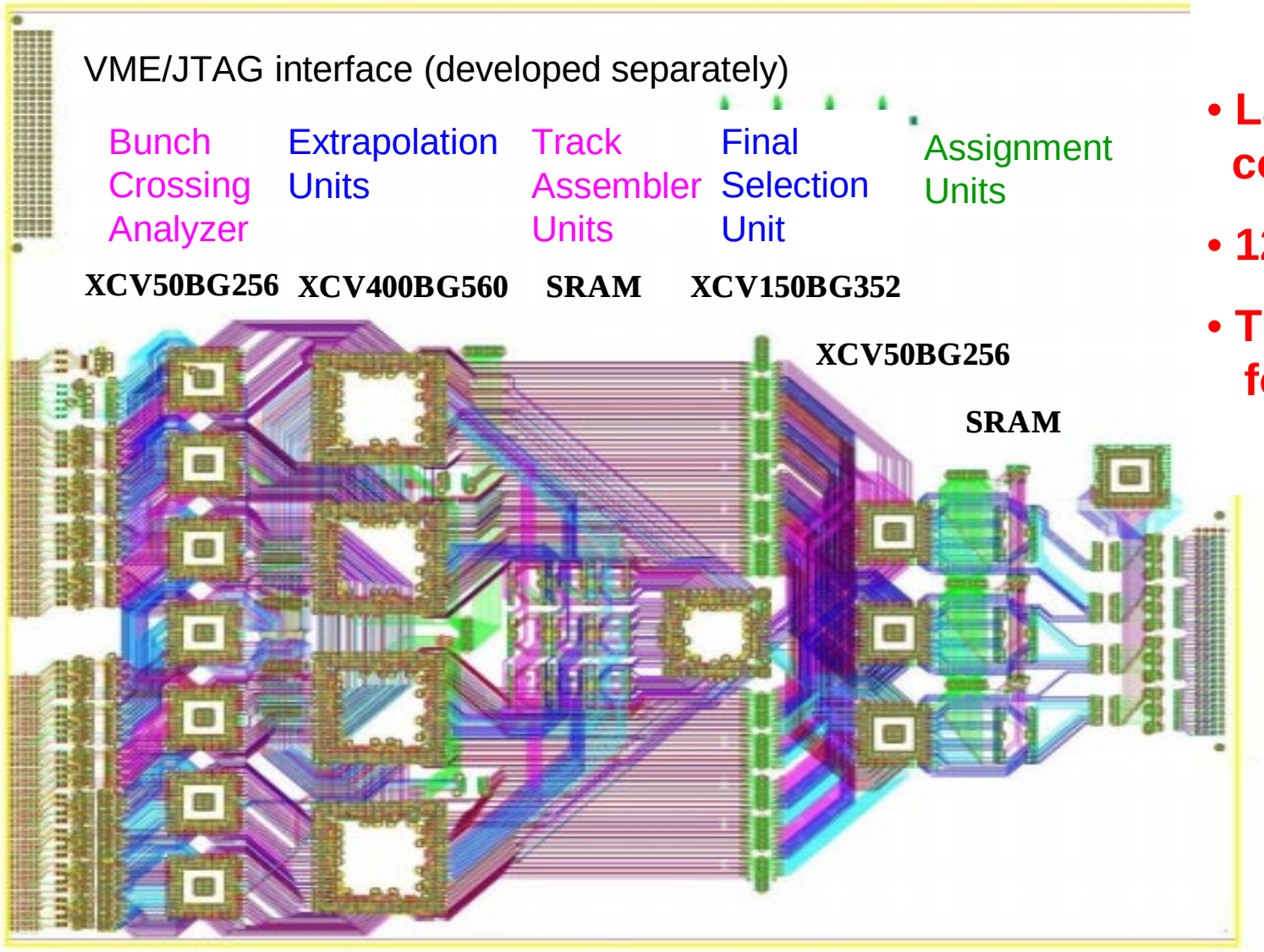
(Improves P_T resolution from 30% to 20%)

SP Prototype Layout

Florida

Standard VME

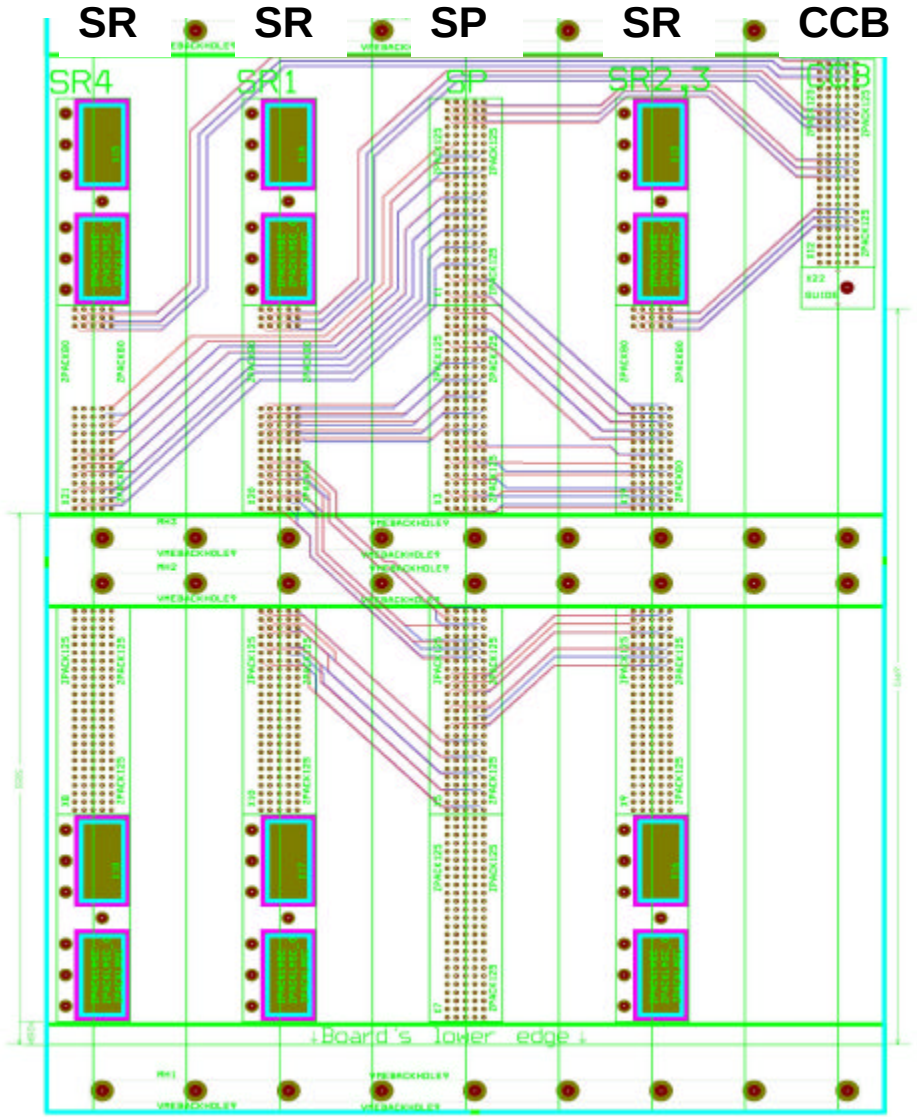
Custom ChannelLink backplane



- **Layout complete**
- **12 layers**
- **Tests set for 6/1/00**

Prototype Crate Layout

3.1.1.7



One sector is half of Track-Finder crate

Six crates for entire system

Fully routed for summer tests

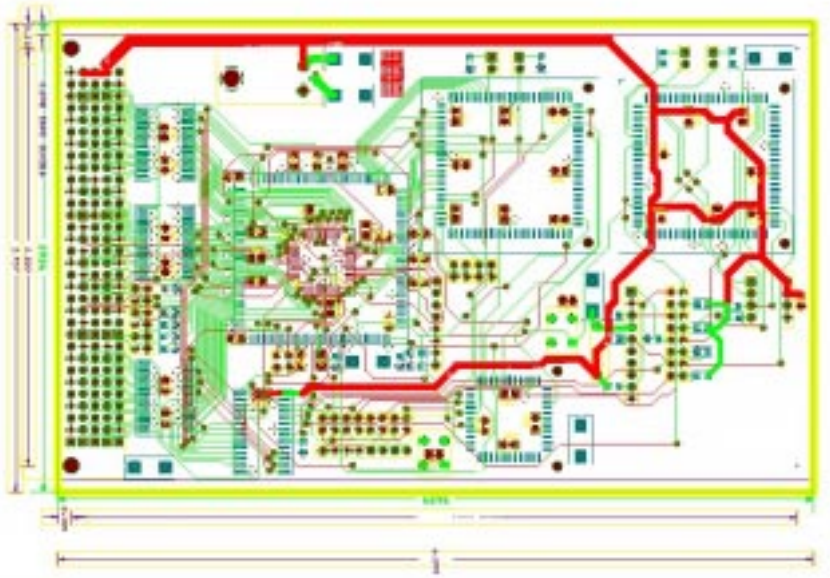
Smaller prototype tested already

Pre-Prototype Tests

Florida

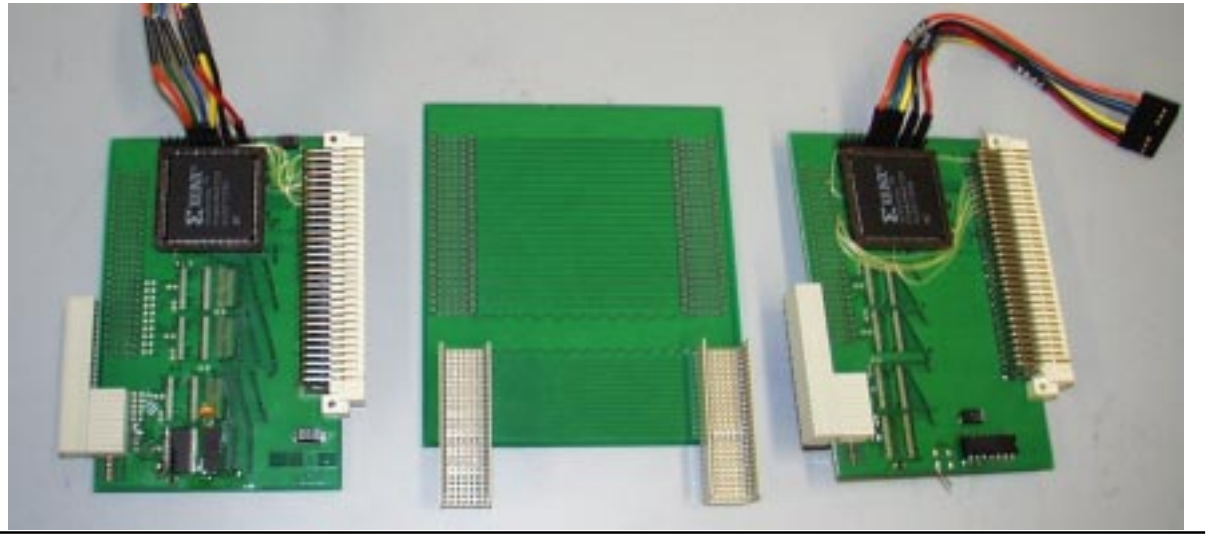
VME / JTAG interface for SR and SP:

Software & hardware for FPGA and SRAM downloading through VME works



Channel Link backplane and connector tests:

No errors found up to 58 MHz clock (400 MHz on backplane)



Muon Sorter Functionality

Rice

3.1.1.15

1. **Receive 36 muons from 12 Sector Processors**
   - 36×18 bits = 648 bits (& control bits)
2. **Sort and rank the best 4 muons**
   - Sort is based on 7 bits (5 bits for p_T and 2 bits for quality)
3. **Send the output to the Global Muon Trigger for association with RPC and DT triggers**
   - 4×22 bits = 88 bits

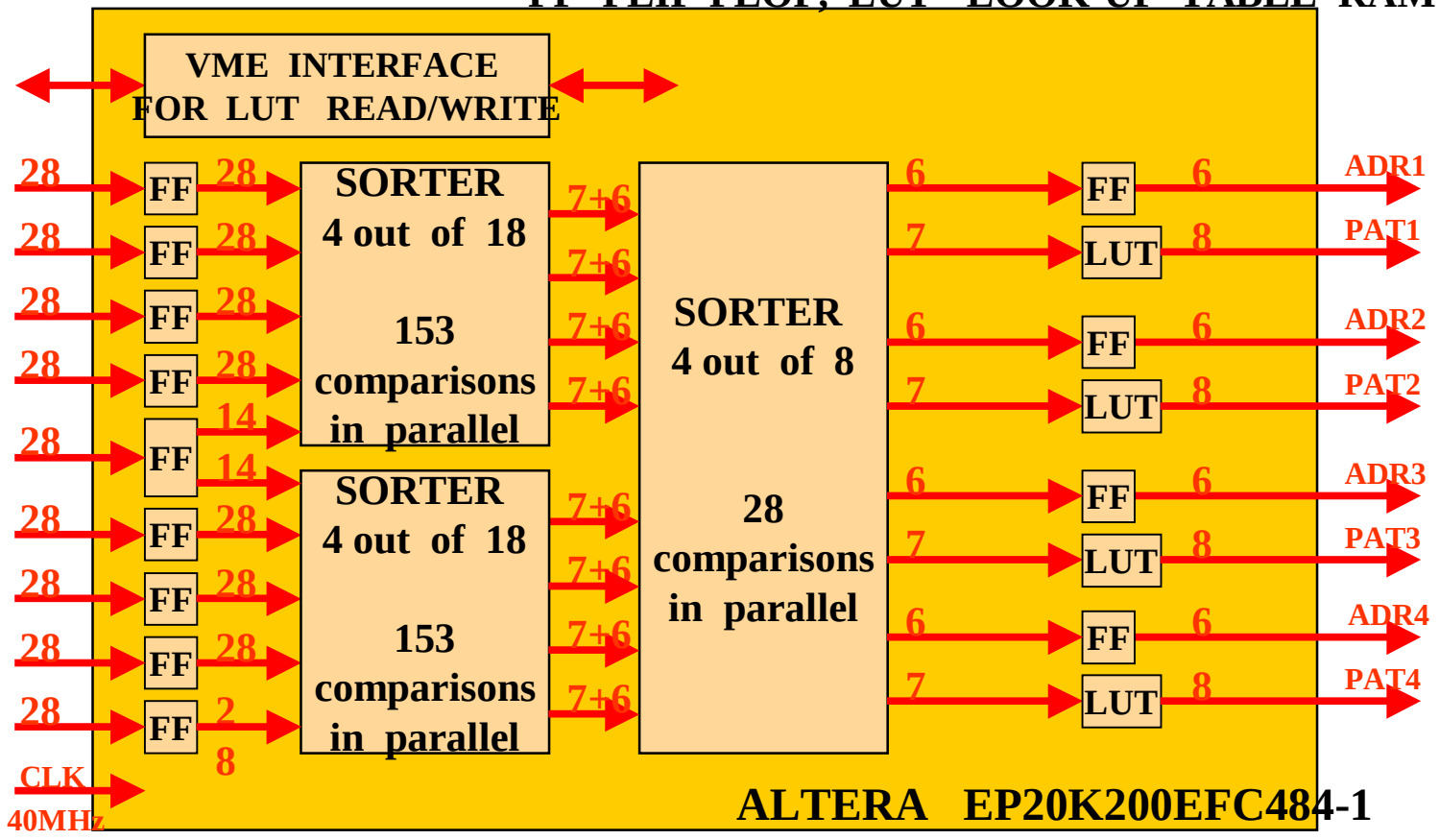
New since last Review:

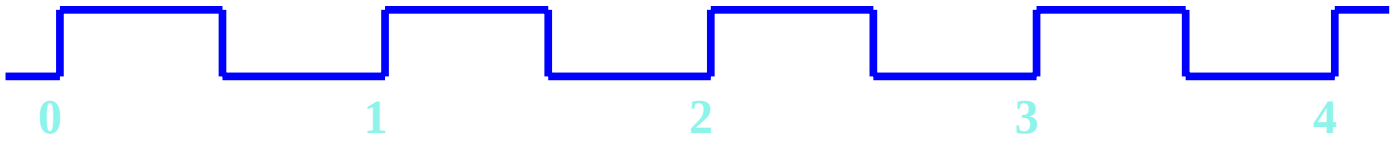
- **Reduction in muon count from 72 to 36 (inclusion of CSC/DT overlap in Sector Processor) allows sorting to be accomplished in one FPGA**

Muon Sorter Logic

Rice

FF- FLIP-FLOP, LUT - LOOK-UP TABLE RAM 3.1.1.15



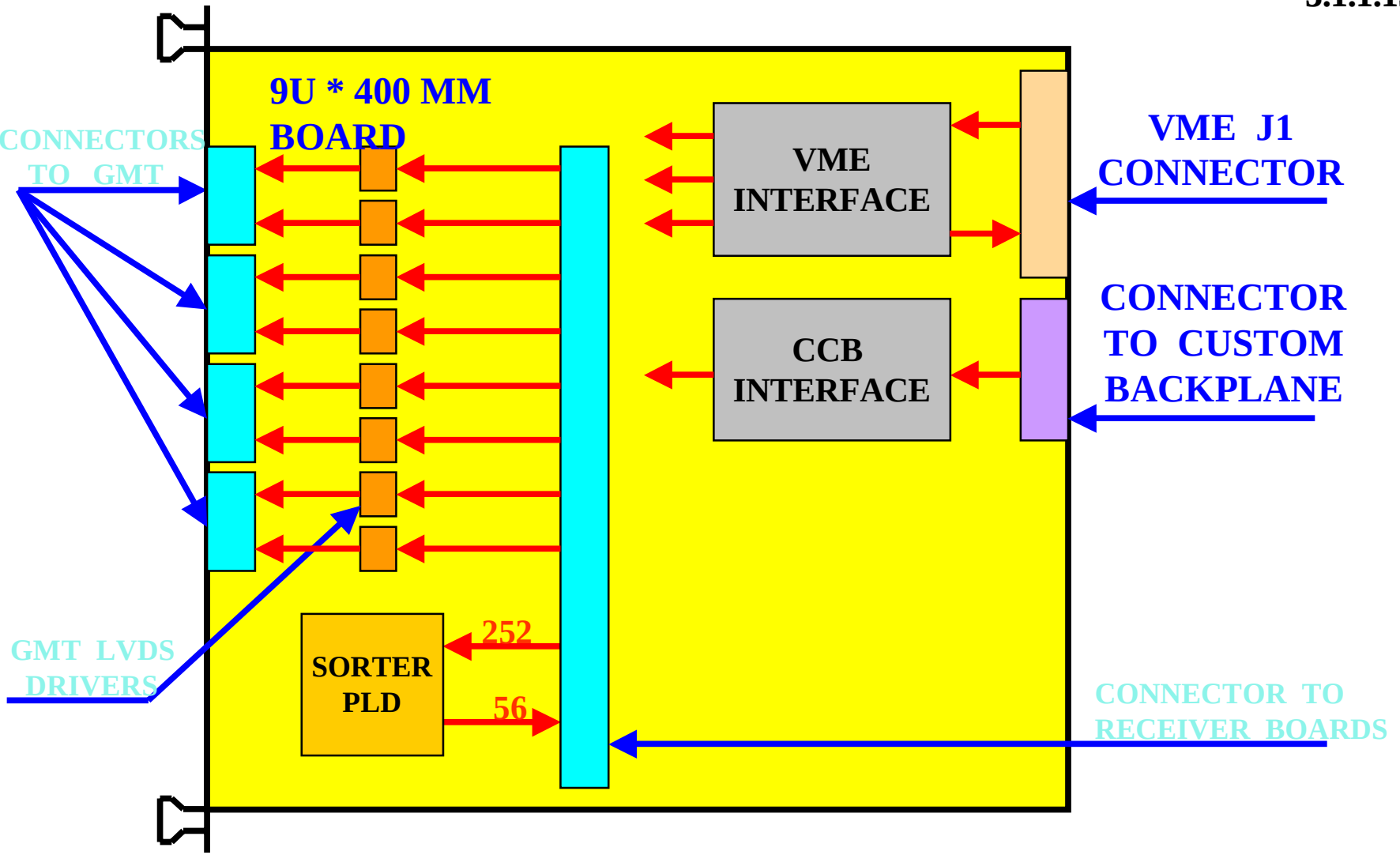


"4 out of 36" SINGLE-CHIP SORTER BLOCK DIAGRAM AND TIMING

Sorter Board Block Diagram

Rice

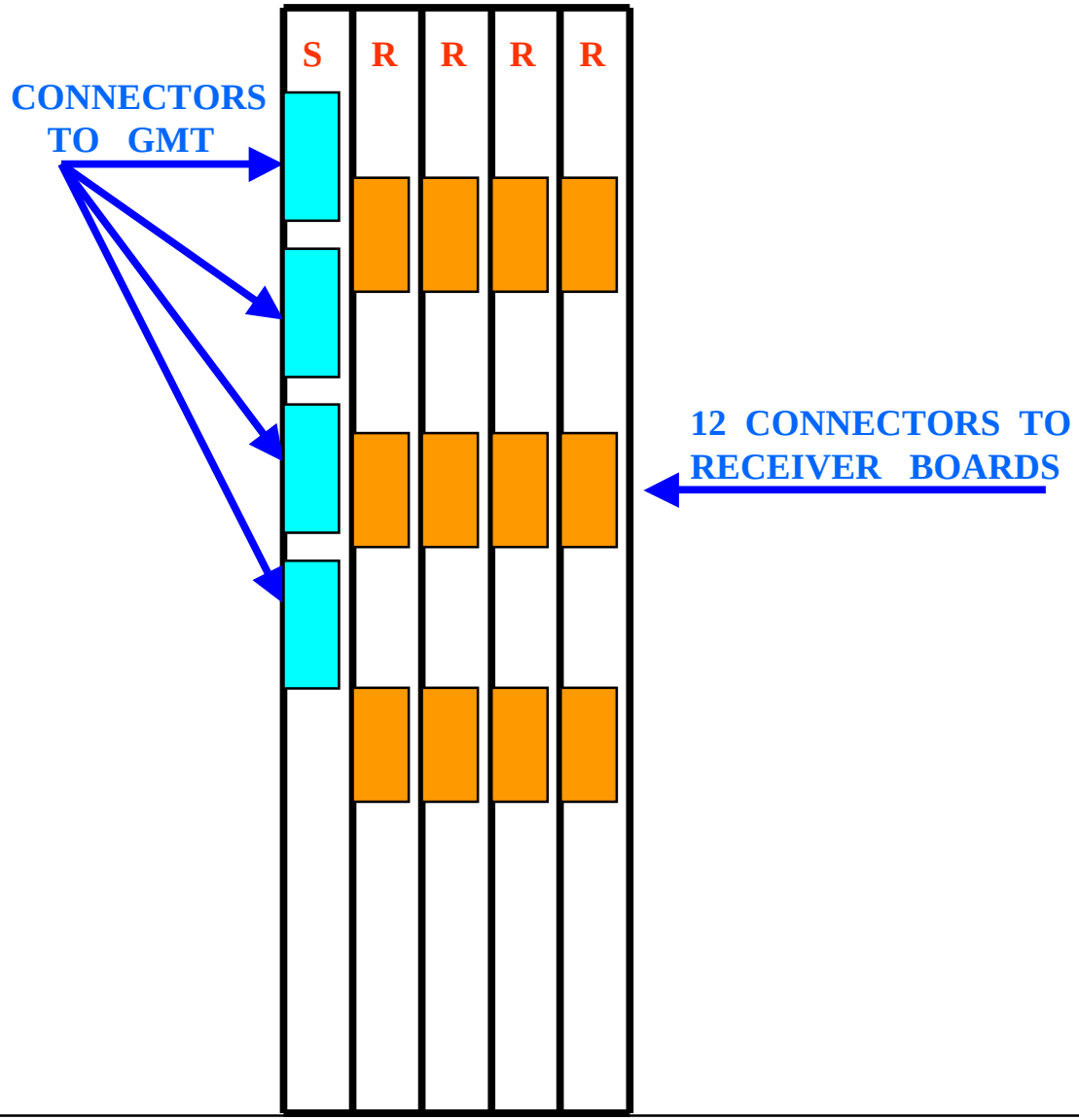
3.1.1.15



Muon Sorter Crate Layout

Rice

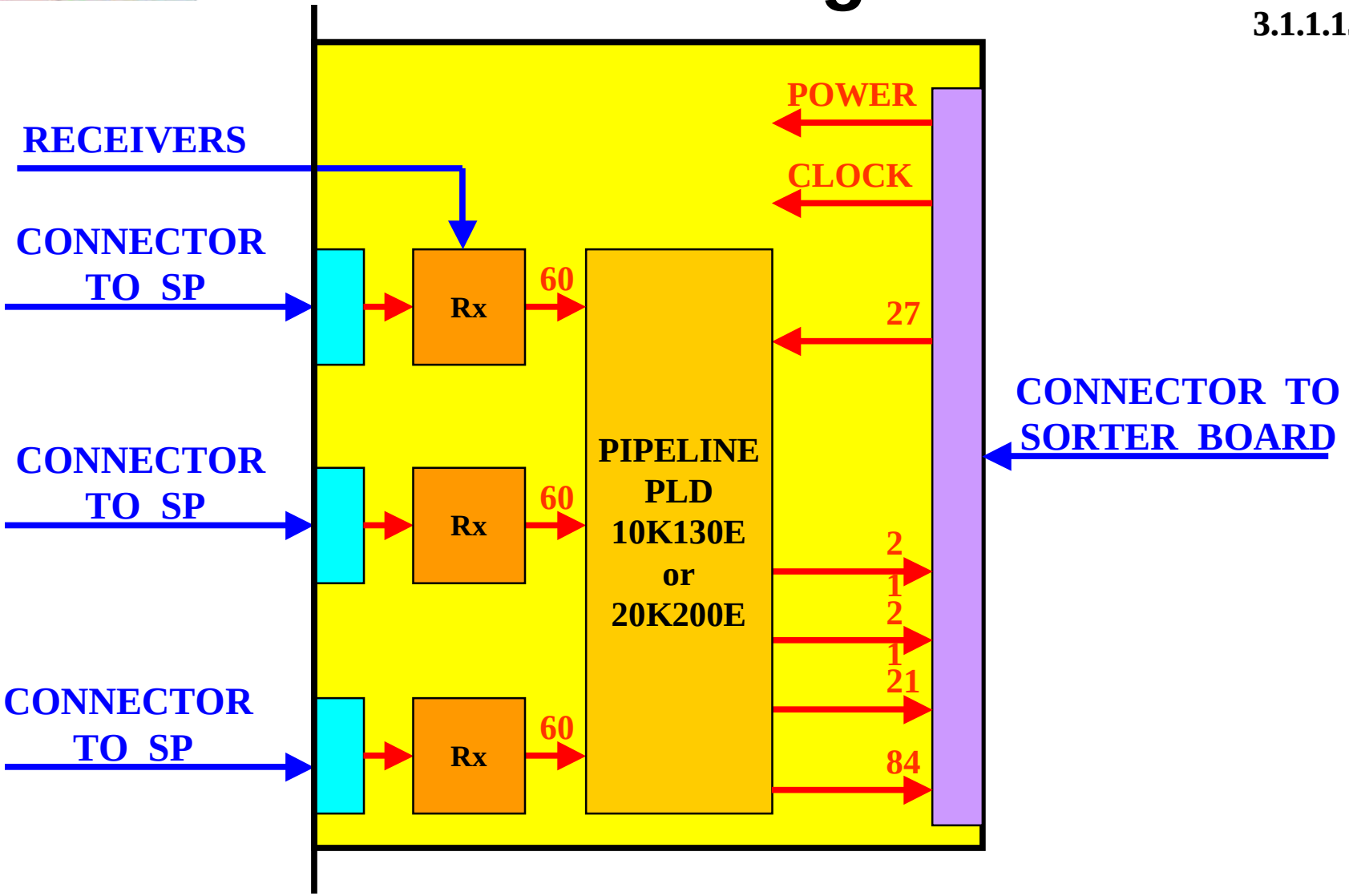
3.1.1.15



Sorter Receiver Board Block Diagram

Rice

3.1.1.15



Summer Plans

Crate test with prototype SR, SP, CCB (and TMB, MPC) scheduled for summer 2000

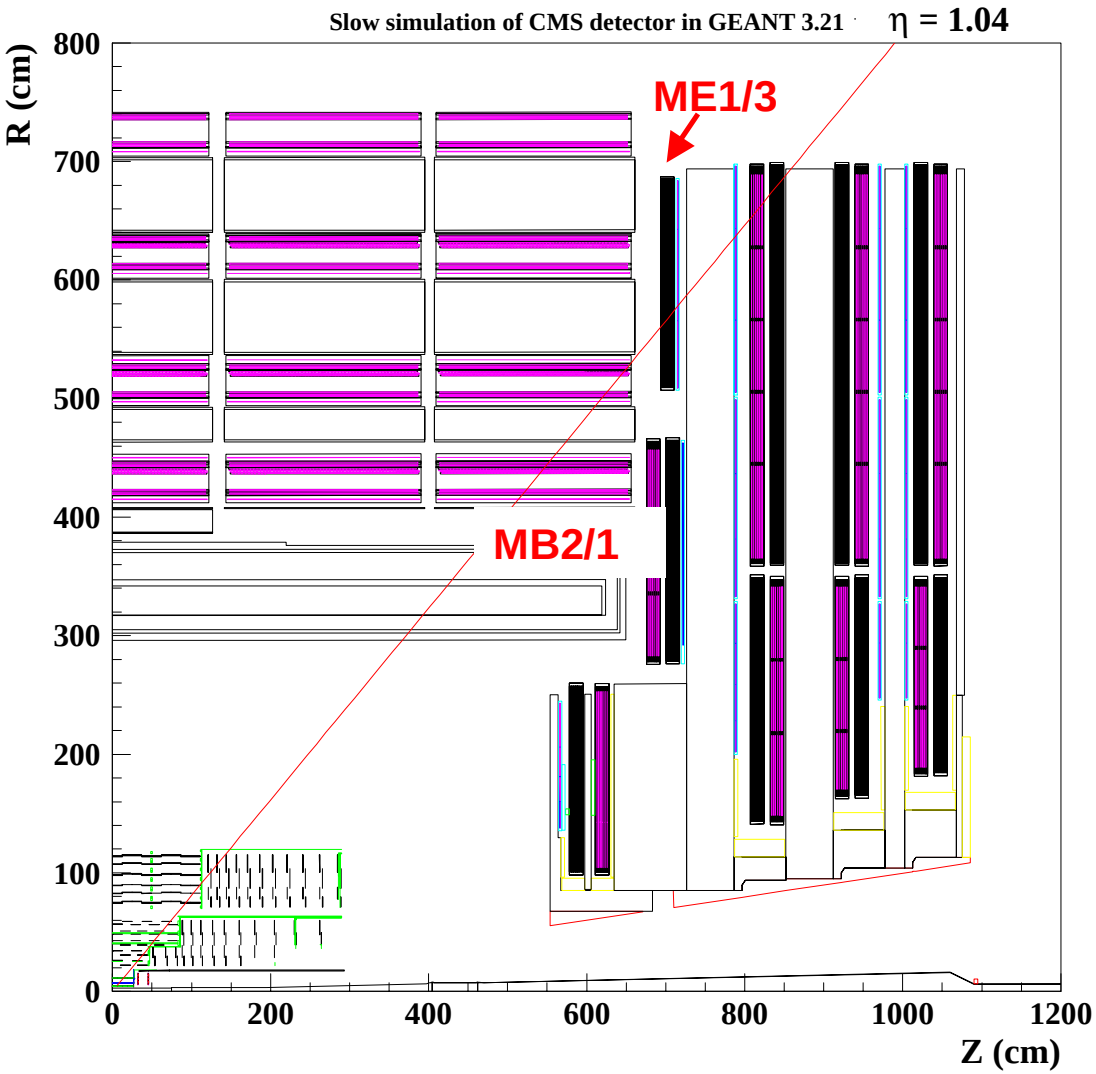
- Bench tests start June 1
- Integration tests start July 1
- Will test optical link connections and trigger algorithms at 40 MHz, verify output and latency

All designs are proceeding well, and we should be able to make milestone

- Conceptual design, schematics, and some layouts already exist

Development of test software started

Separation of DT/CSC Coverage



- Hard boundary defined η=1.04
- Separate Track-Finders optimized for each system
- Information shared across boundary for maximum efficiency
- Tentative agreement reached on DT/CSC interface Feb'00

Advantages of Proposal

- Interconnections are cut in half when track segments from ME 2/2 and MB 2/2 are not shared
  (only ME 1/3 and MB2/1 are shared)

- The mapping of 60° CSC trigger sectors onto 30° DT ones is avoided (no ME 2/2)
  - But, ME1 station has 30° or 20° subsectors, so there may still be a mapping problem

- The RPC data may be used by the GMT to settle any ghosting problem if a single muon is found by both Track-Finders

- ϕ_b and η do not need to be sent by the CSC Track-Finder for DT T-F extrapolations

Advantages Continued

- **The DT Track-Finder may trigger on MB1-MB2 type tracks**
  - These track segments and all those sent by the CSC trigger are assumed to be in barrel region
- **The CSC Track-Finder logic is considerably simplified with proposed boundary**
  - Already assumed in present prototype

Issues with Proposal

Must demonstrate acceptable efficiency by simulation

CSC Sector Receiver must be designed to send only 2 track segments (out of 3) for the barrel-overlap region