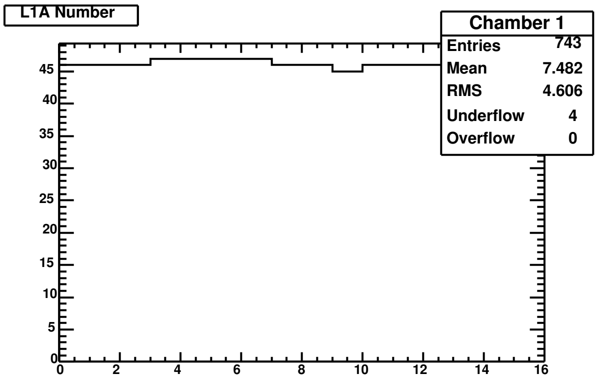
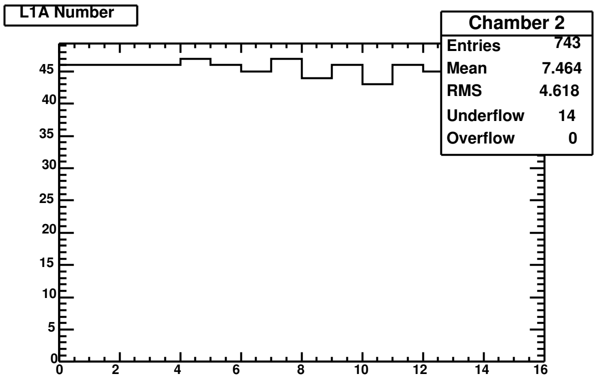
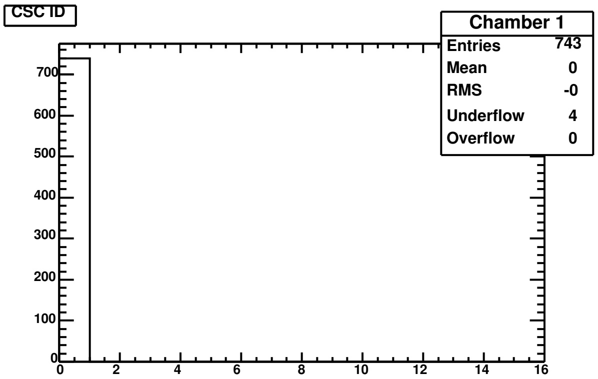
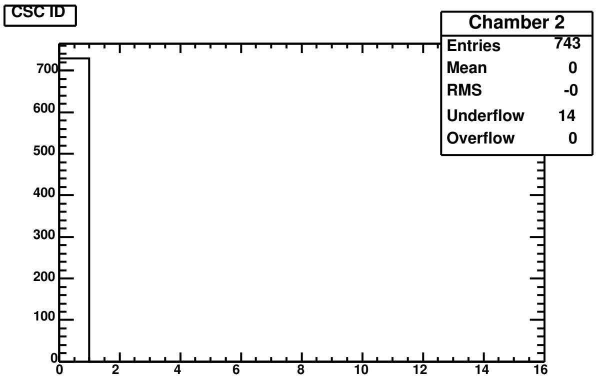
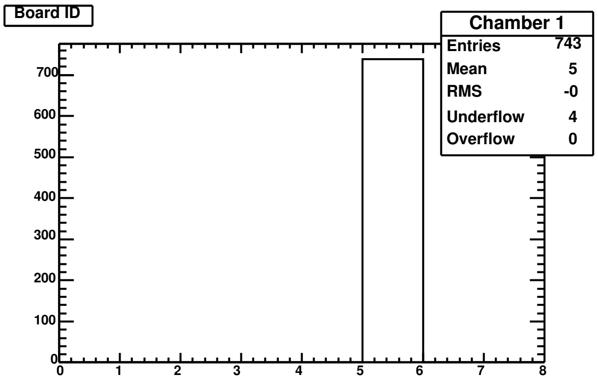
ALCT Header

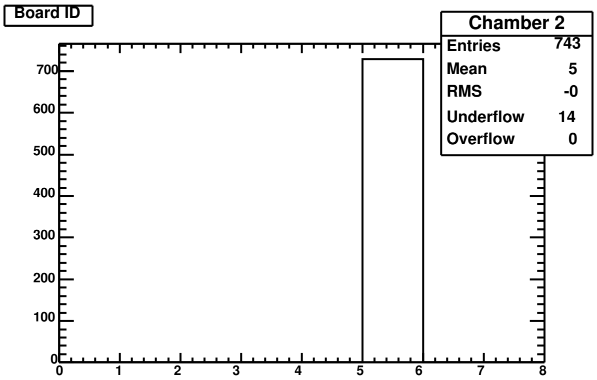


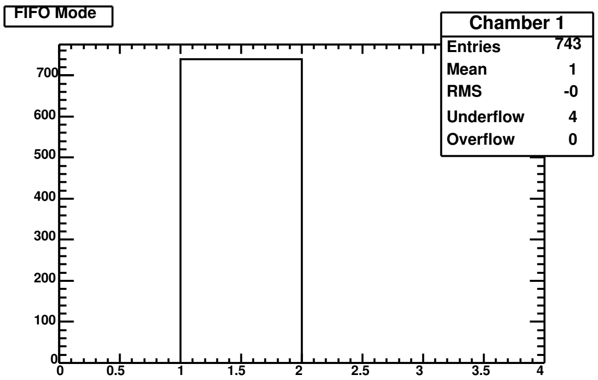


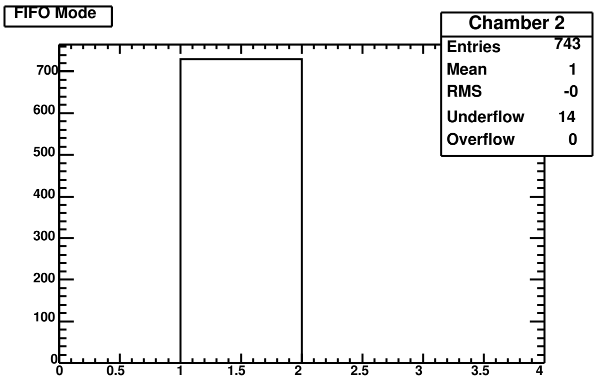












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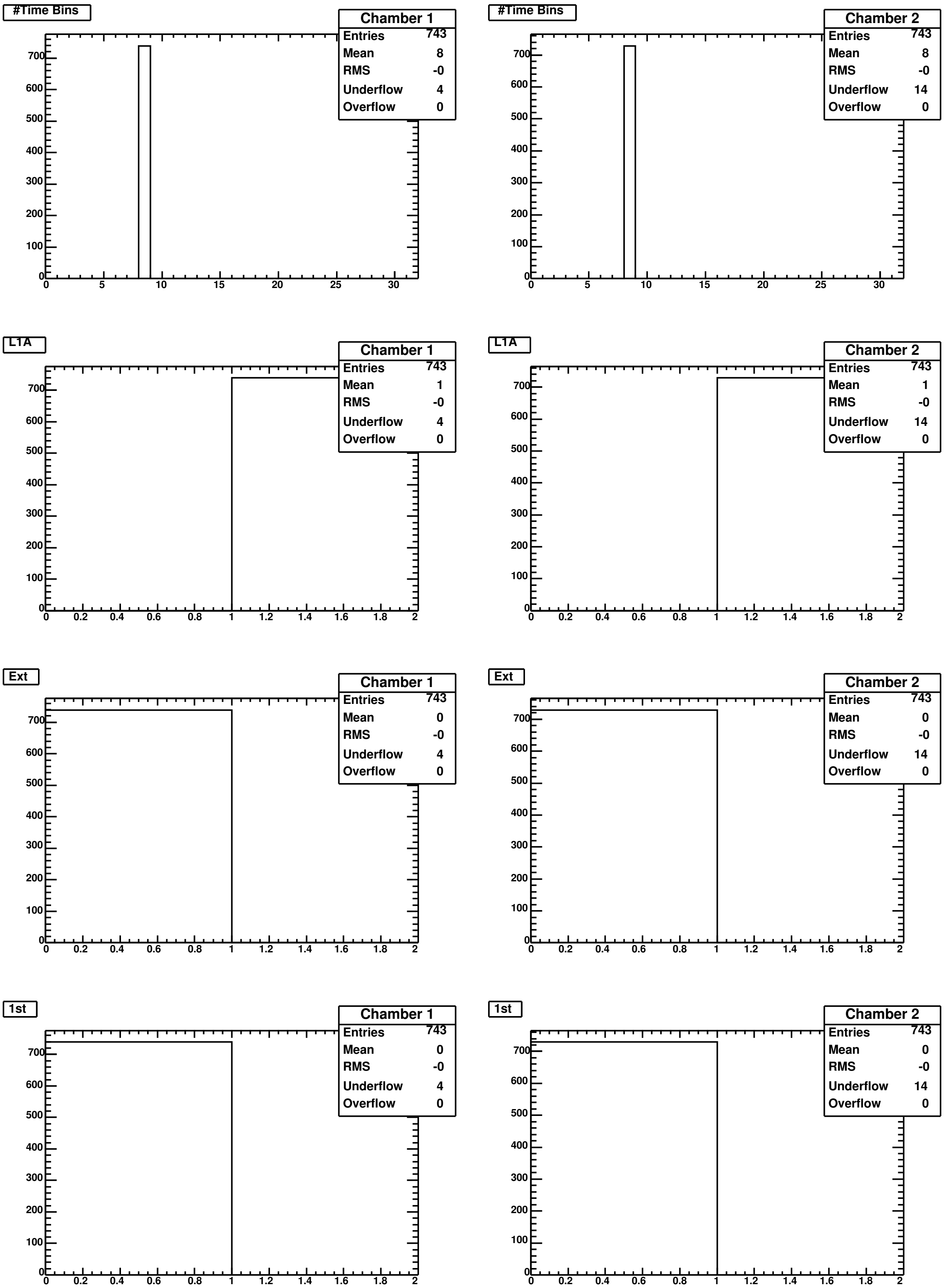
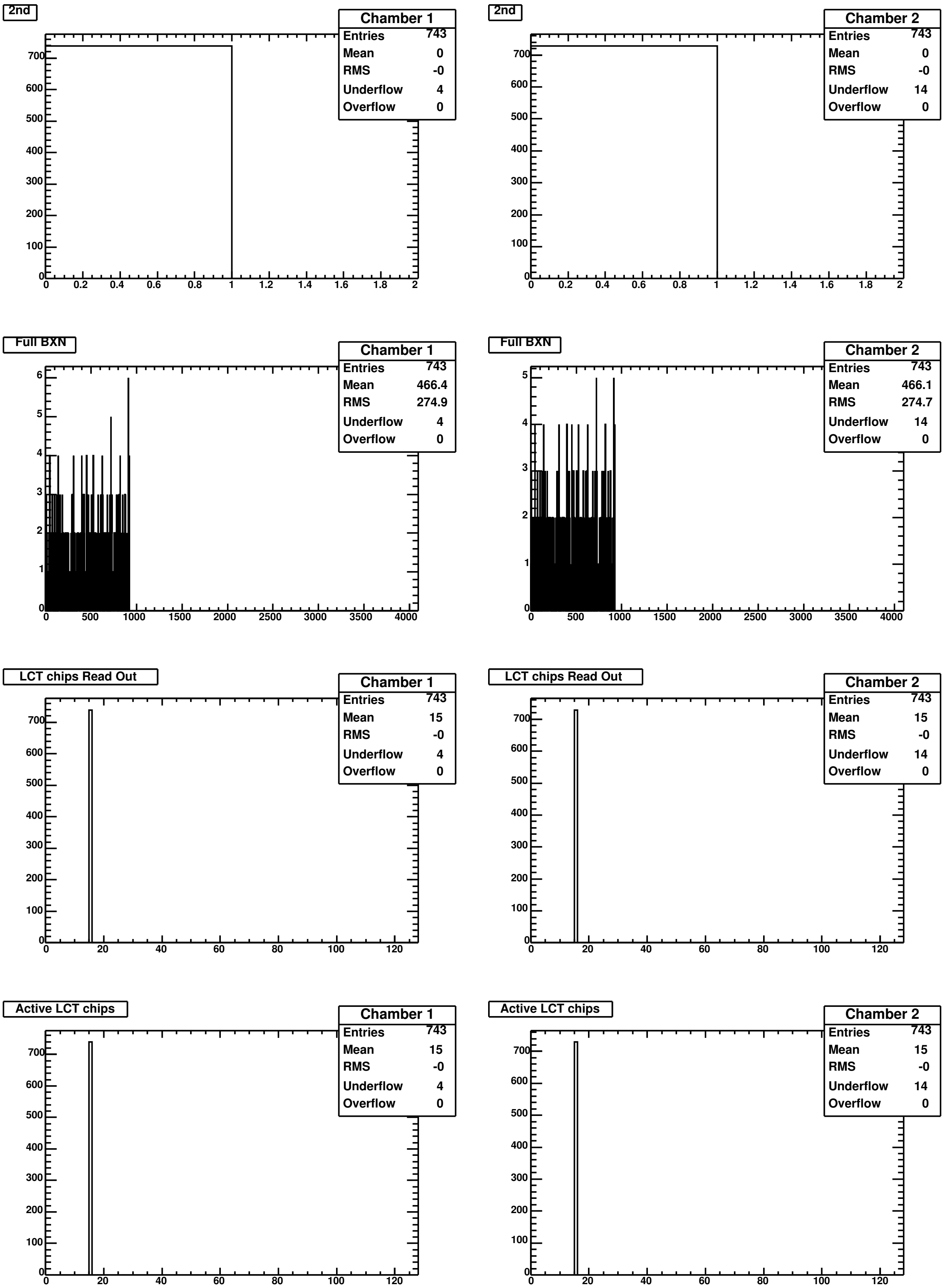
ALCT Header


#Time Bins
Chamber 1
Entries 743
Mean 8
RMS -0
Underflow 4
Overflow 0
#Time Bins
Chamber 2
Entries 743
Mean 8
RMS -0
Underflow 14
Overflow 0
L1A
Chamber 1
Entries 743
Mean 1
RMS -0
Underflow 4
Overflow 0
L1A
Chamber 2
Entries 743
Mean 1
RMS -0
Underflow 14
Overflow 0
Ext
Chamber 1
Entries 743
Mean 0
RMS -0
Underflow 4
Overflow 0
Ext
Chamber 2
Entries 743
Mean 0
RMS -0
Underflow 14
Overflow 0
1st
Chamber 1
Entries 743
Mean 0
RMS -0
Underflow 4
Overflow 0
1st
Chamber 2
Entries 743
Mean 0
RMS -0
Underflow 14
Overflow 0

ALCT Header



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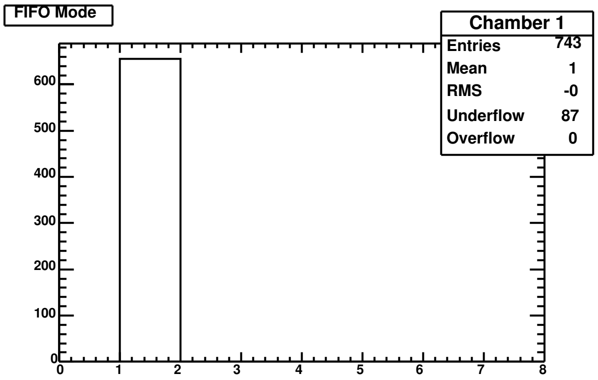
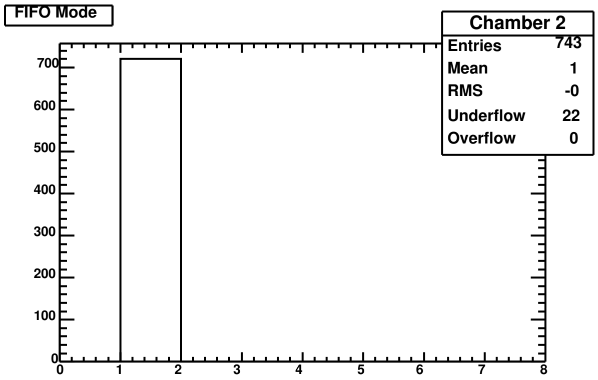
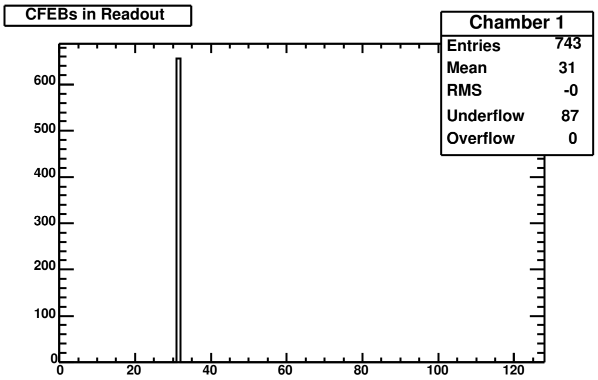
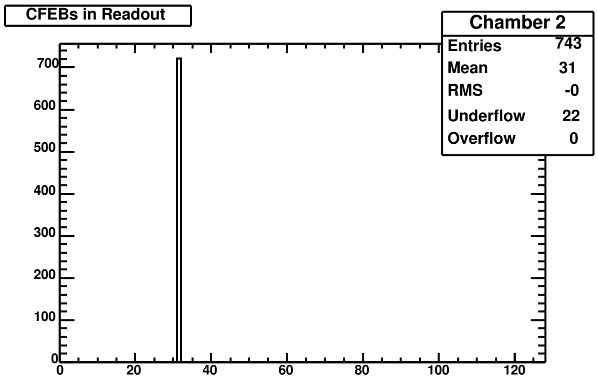
TMB Header


FIFO Mode
Chamber 1
Entries 743
Mean 1
RMS -0
Underflow 87
Overflow 0
0 100 200 300 400 500 600
0 1 2 3 4 5 6 7 8


FIFO Mode
Chamber 2
Entries 743
Mean 1
RMS -0
Underflow 22
Overflow 0
0 100 200 300 400 500 600 700
0 1 2 3 4 5 6 7 8


CFEBs in Readout
Chamber 1
Entries 743
Mean 31
RMS -0
Underflow 87
Overflow 0
0 100 200 300 400 500 600
0 20 40 60 80 100 120


CFEBs in Readout
Chamber 2
Entries 743
Mean 31
RMS -0
Underflow 22
Overflow 0
0 100 200 300 400 500 600 700
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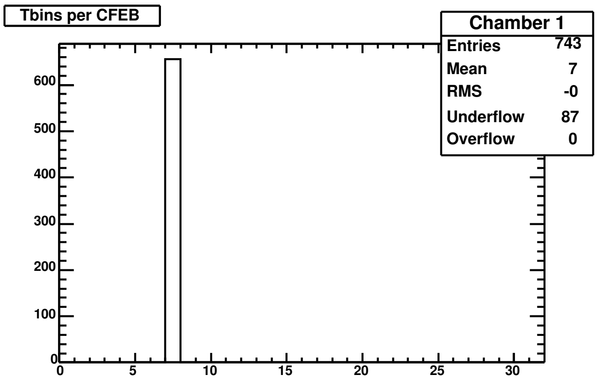
Tbins per CFEB
Chamber 1
Entries 743
Mean 7
RMS -0
Underflow 87
Overflow 0
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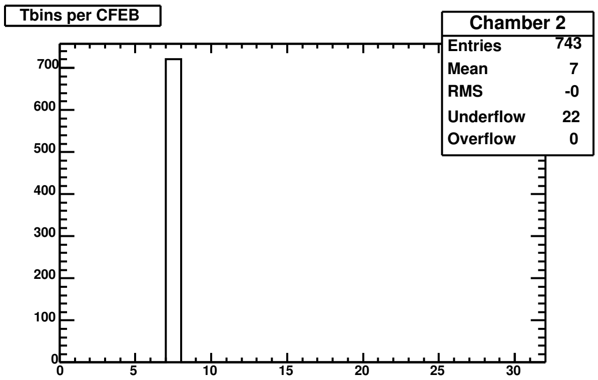
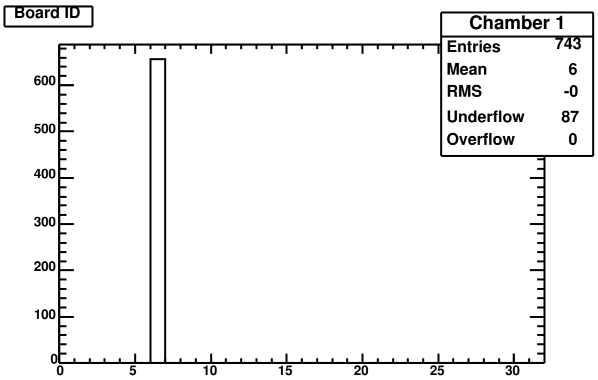
0 5 10 15 20 25 30


Tbins per CFEB
Chamber 2
Entries 743
Mean 7
RMS -0
Underflow 22
Overflow 0
0 100 200 300 400 500 600 700
0 5 10 15 20 25 30


Board ID
Chamber 1
Entries 743
Mean 6
RMS -0
Underflow 87
Overflow 0
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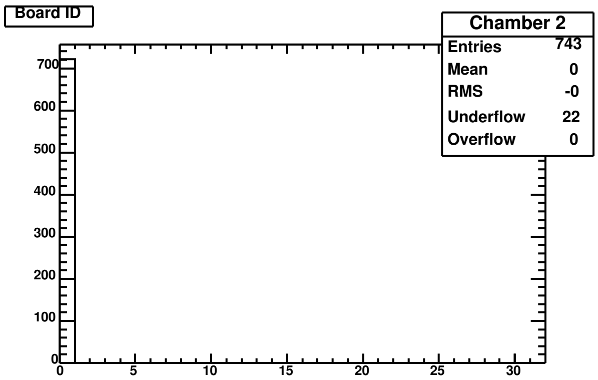
Board ID
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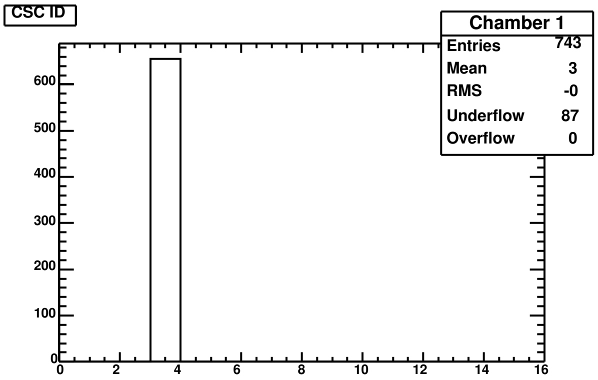
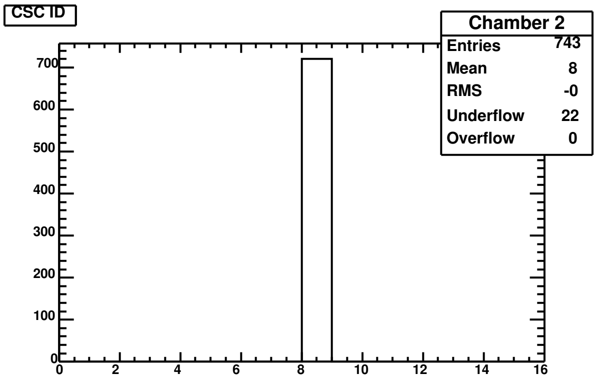
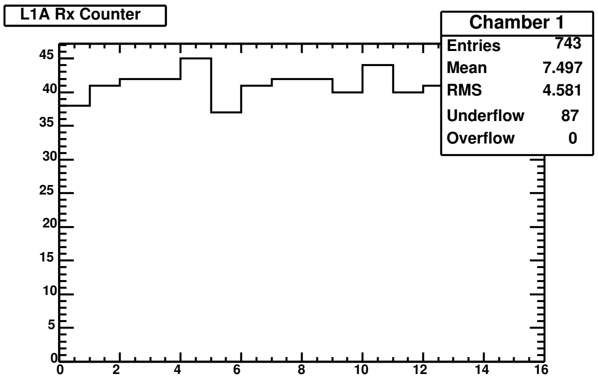
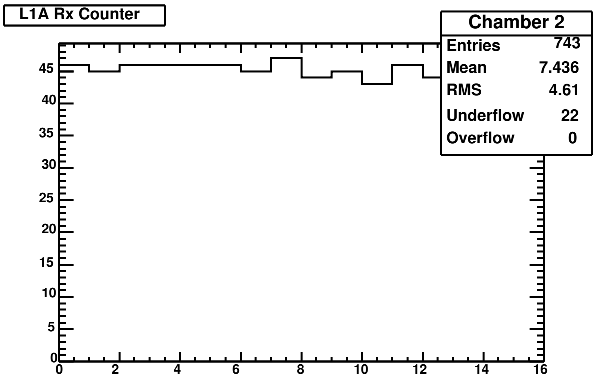
Entries 743
Mean 0
RMS -0
Underflow 22
Overflow 0
0 100 200 300 400 500 600 700
0 5 10 15 20 25 30

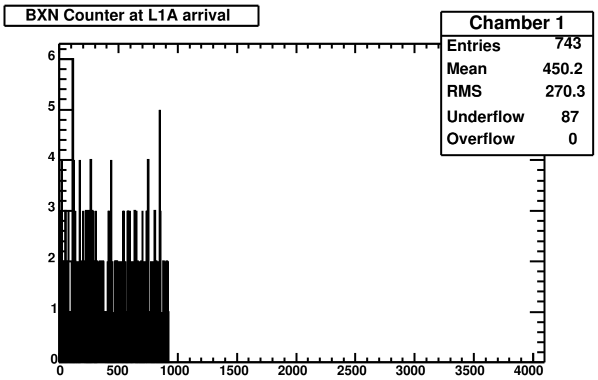
TMB Header

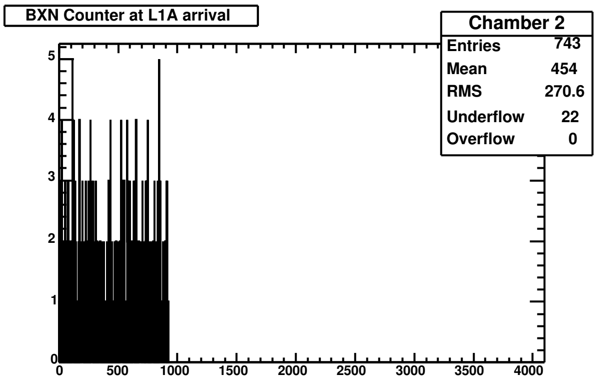


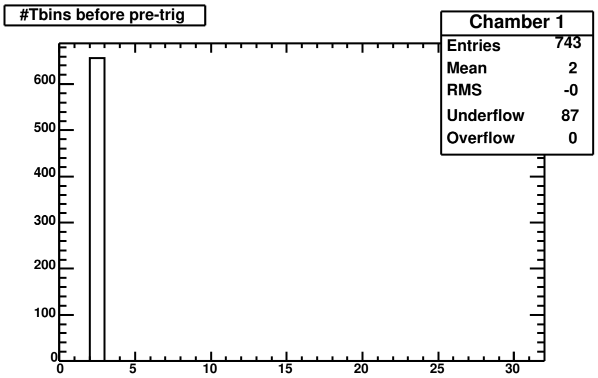


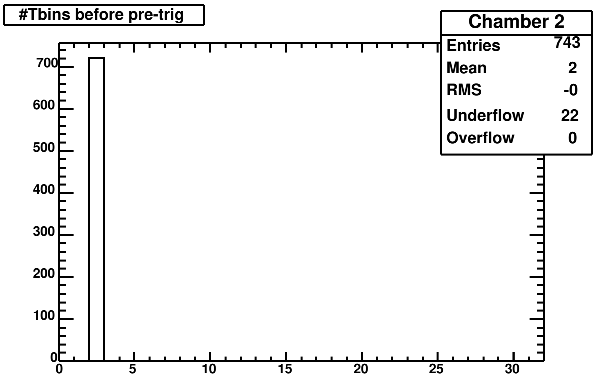












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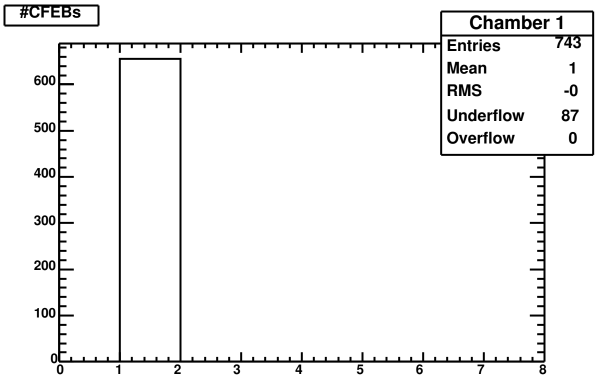
#CFEBs
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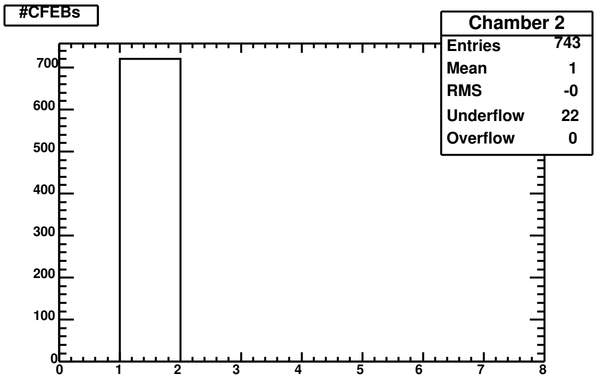
Entries 743
Mean 1
RMS -0
Underflow 87
Overflow 0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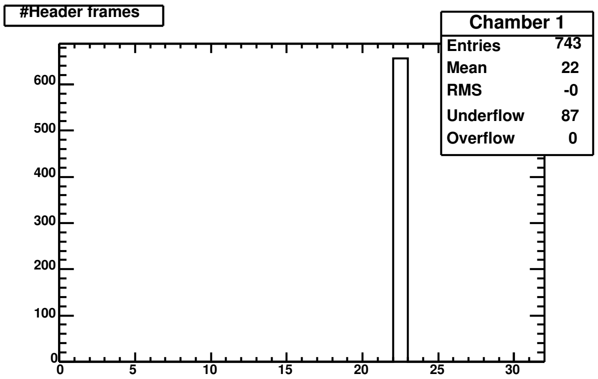
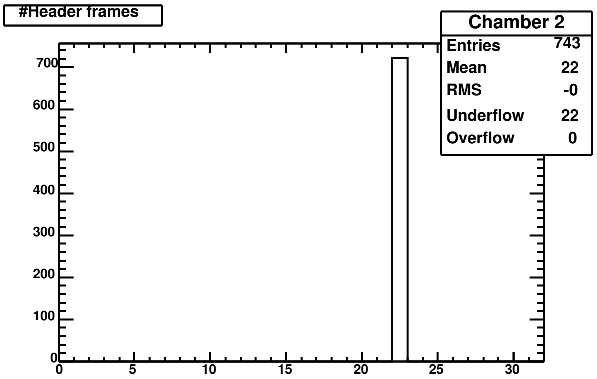
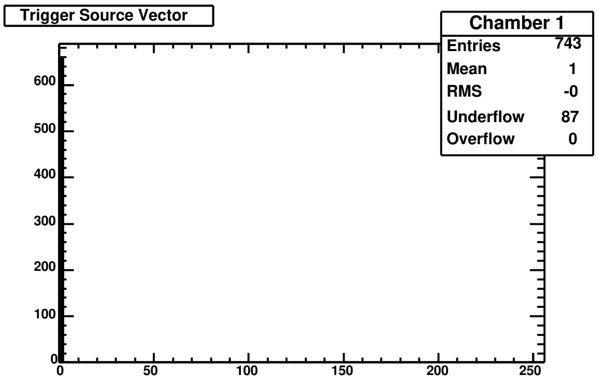
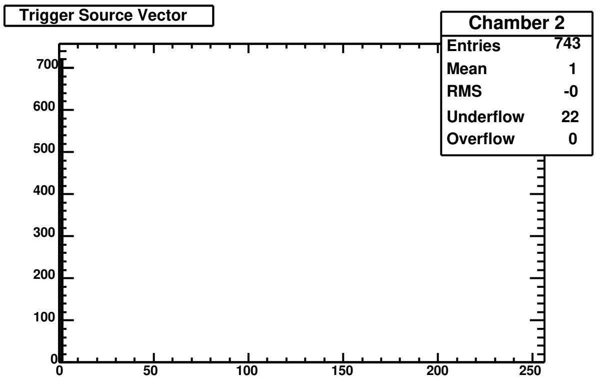
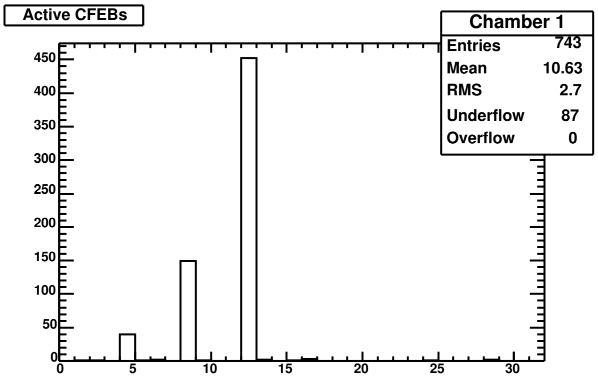
Chamber 2
Entries 743
Mean 1
RMS -0
Underflow 22
Overflow 0

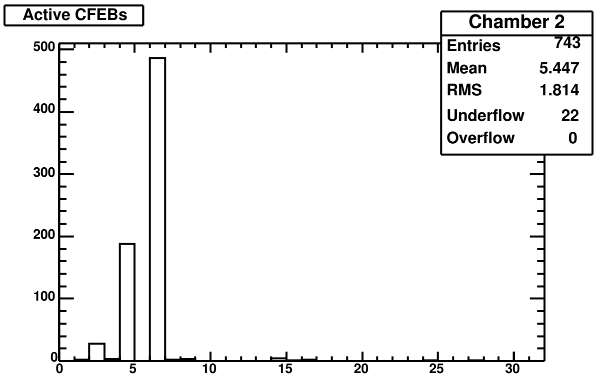

#Header frames
Chamber 1
Entries 743
Mean 22
RMS -0
Underflow 87
Overflow 0


#Header frames
Chamber 2
Entries 743
Mean 22
RMS -0
Underflow 22
Overflow 0

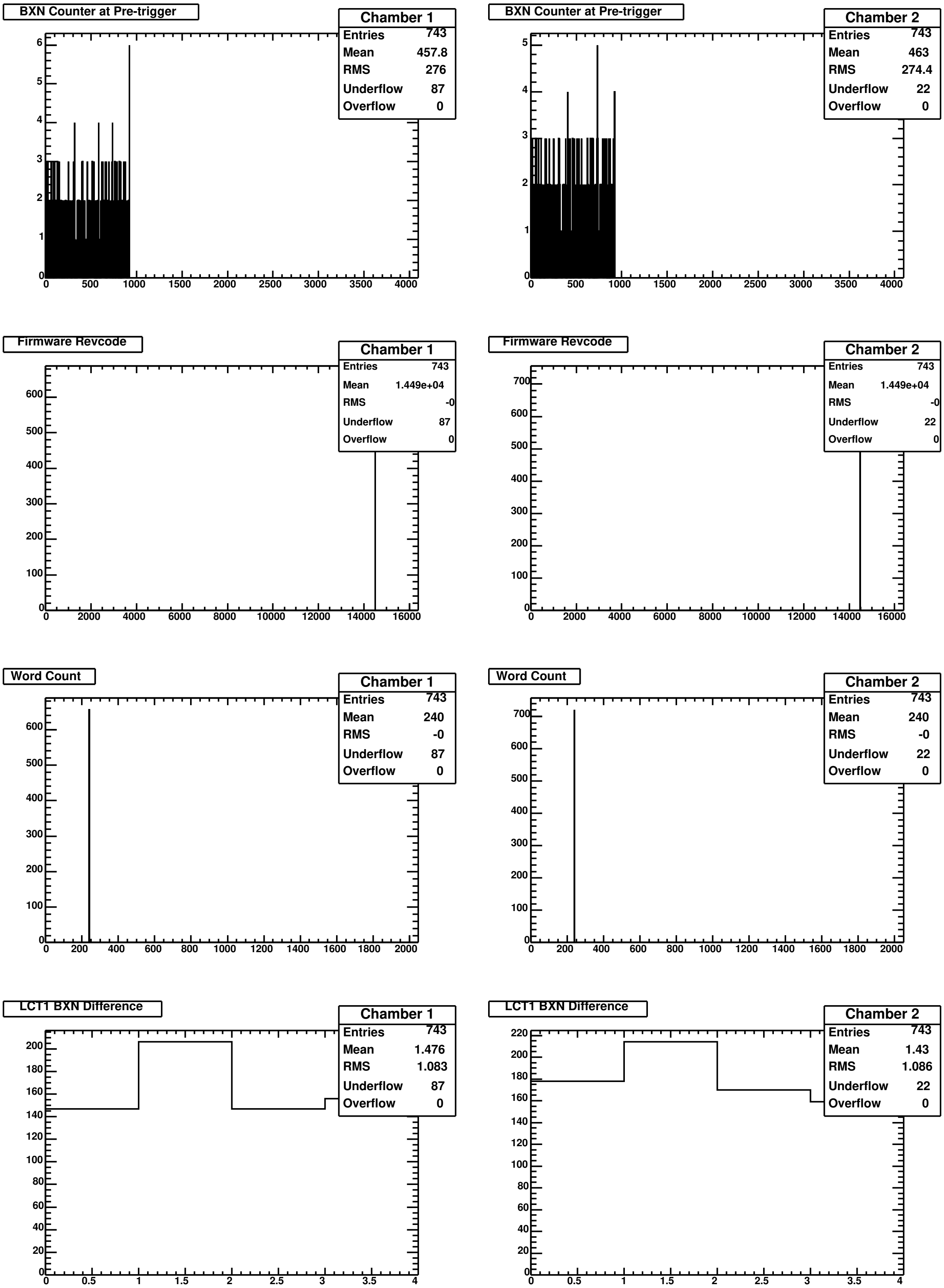

Trigger Source Vector
Chamber 1
Entries 743
Mean 1
RMS -0
Underflow 87
Overflow 0


Trigger Source Vector
Chamber 2
Entries 743
Mean 1
RMS -0
Underflow 22
Overflow 0


Active CFEBs
Chamber 1
Entries 743
Mean 10.63
RMS 2.7
Underflow 87
Overflow 0


Active CFEBs
Chamber 2
Entries 743
Mean 5.447
RMS 1.814
Underflow 22
Overflow 0

TMB Header



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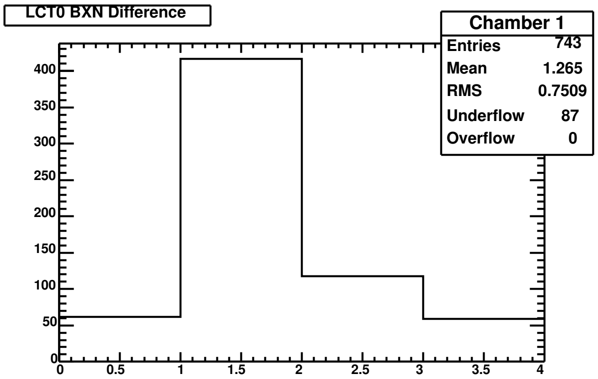

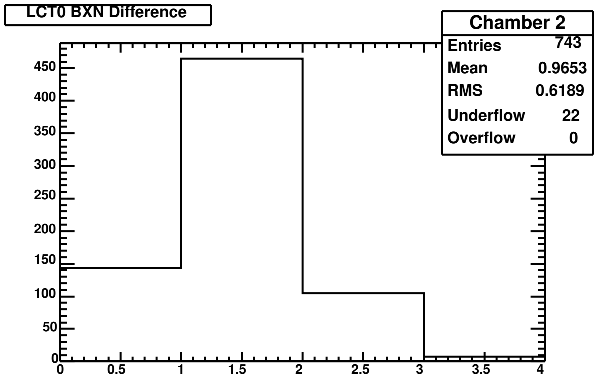

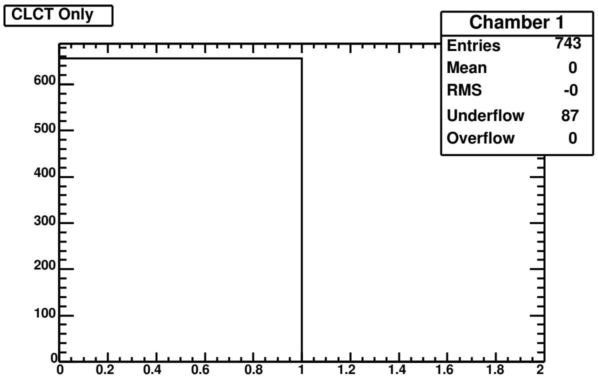

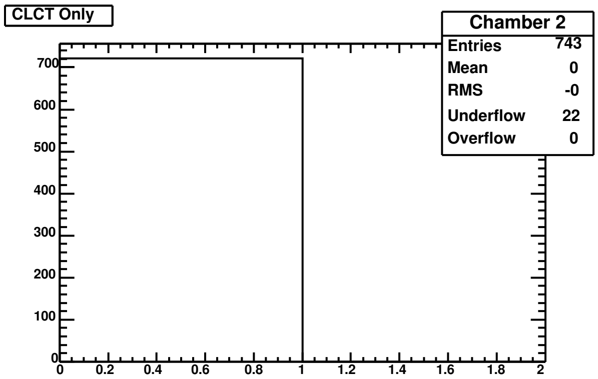

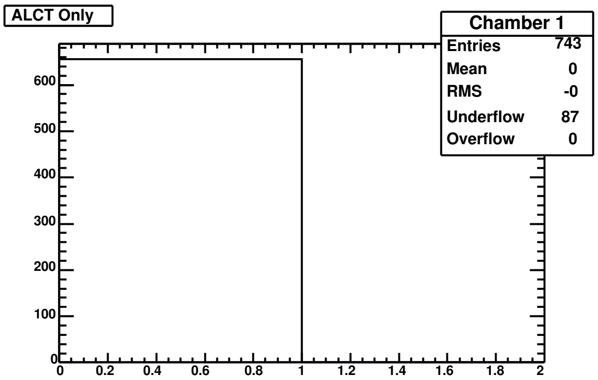

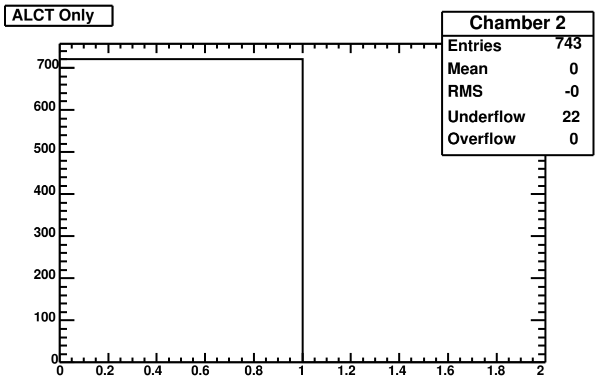

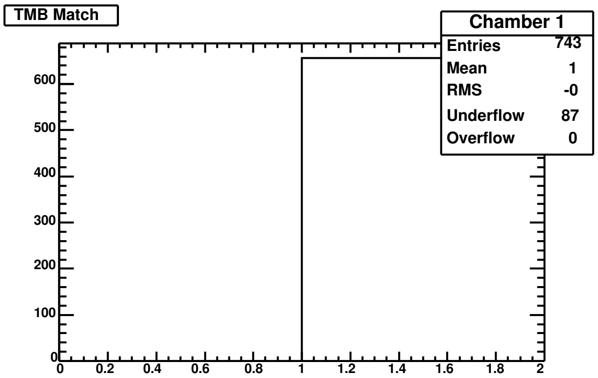

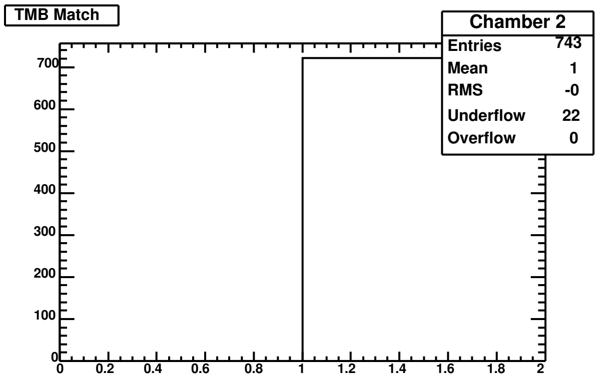

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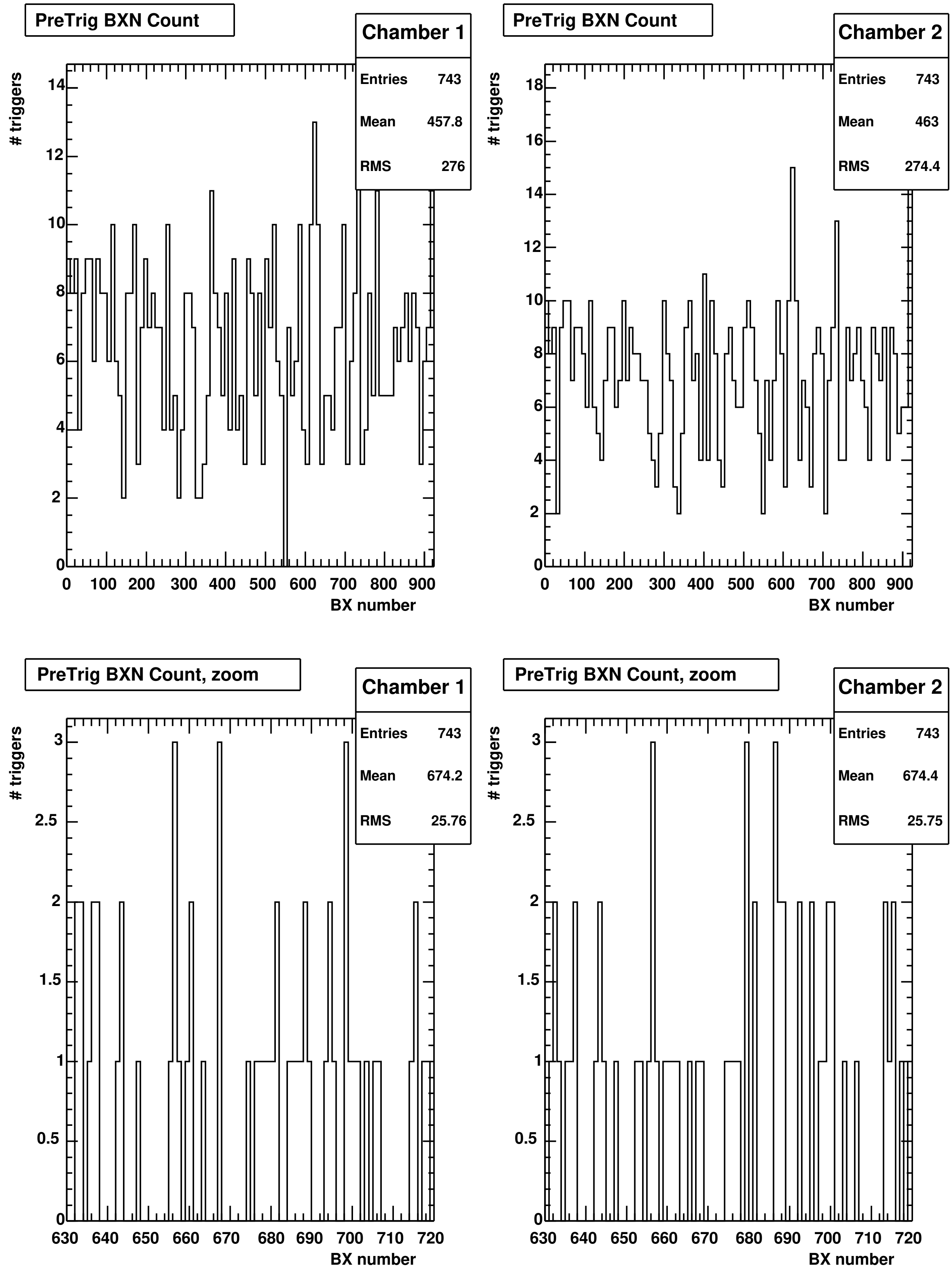
BXN Counter at Pre-trigger



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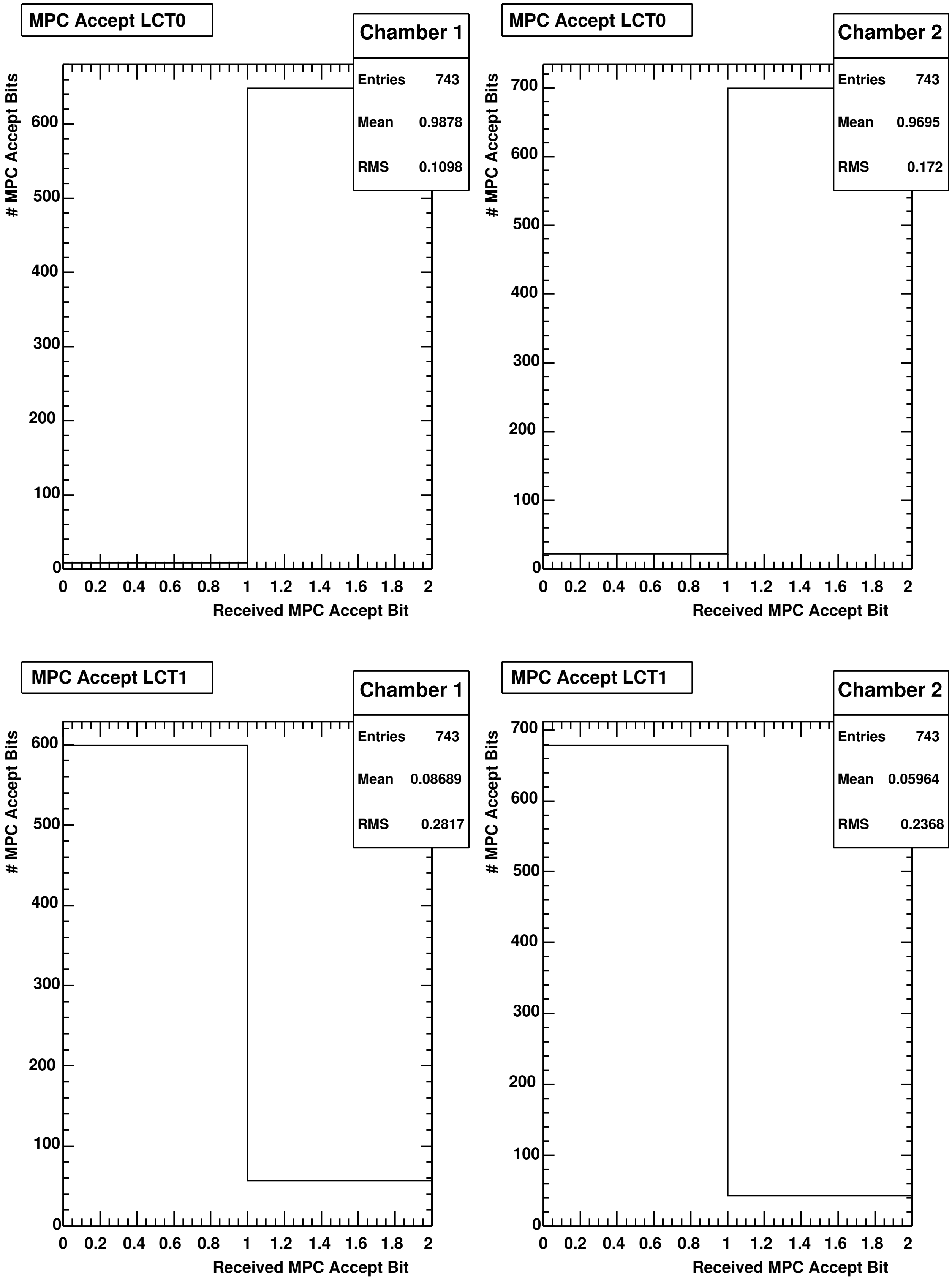
MPC Accept Bits



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