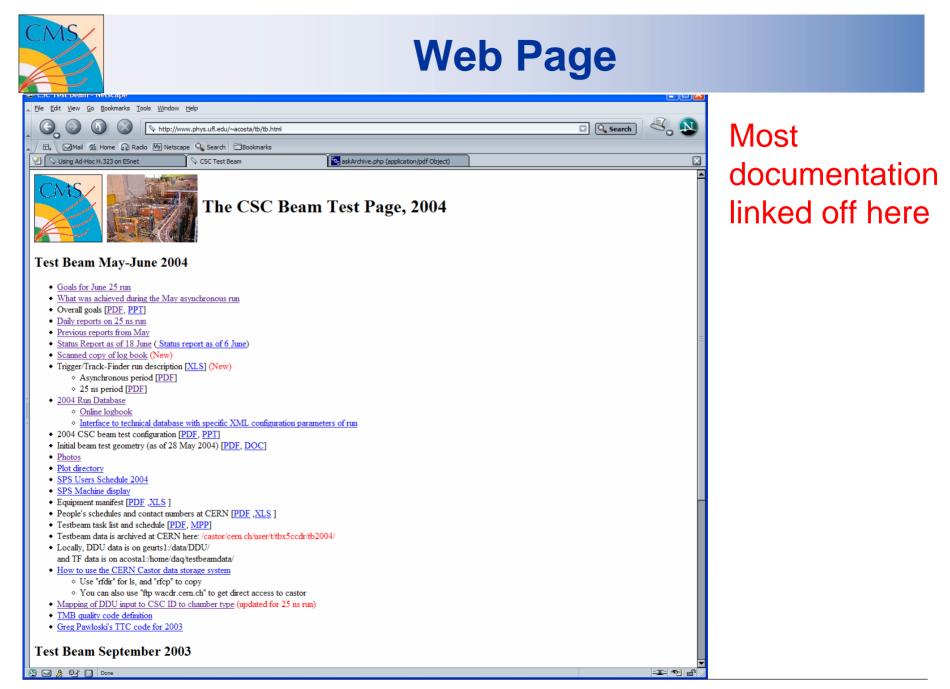
Test Beam Wrap-Up

Darin Acosta



Agenda

- Darin/UF: General recap of runs taken, tests performed,
- Track-Finder issues
- Martin/UCLA: Summary of RAT and RPC tests, and experience with TMB2004
- Stan(or Jason or Jianhui)/OSU: Experience with DMB and DDU using new
 CCB and with new peripheral crate software
- Frank/Rice: Summary of DAQ code development and event-builder tests
- Alex/Rice (also Rick?): Status of data unpacking software packages
- Andrey/UF: Testbeam summary from DQM point-of-view
- All: Discussion of September beam test goals at H2
- Frank/Rice: Possible CSC, crate, cable layout at H2





2004 Beam Test Goals

Base goal:

(As set out in April)

- Set up pre-production system of USCMS EMU electronics and repeat prior tests using LHC-like 25 ns structured beam
 - Test new radiation tolerant clock and control timing module (CCB 2004), which is required before production
- Additional goals:
 - Test CSC trigger primitive logic with RPC and CSC Anode transition card (so-called "RAT" transition card on TMB2004)
 - Use fully functional XDAQ-based run control and event builder
 - Use fully functional Level-1 Track-Finder system (self-triggering)
 - Use new DDU+DCC (so-called Front End Driver, FED, for DAQ)
 - Use new peripheral crate VME controller developed by OSU
 - Add in ME1/1 (Dubna groups)
 - Add an ME1/2 chamber (IHEP group)
 - Construct and mount an endcap RPC on ME1/2 (CERN, Korea, China)
 - Connect and test RPC trigger Link board to RAT (Warsaw)
 - Add a small block of iron absorber between to validate OSCAR/ORCA simulation

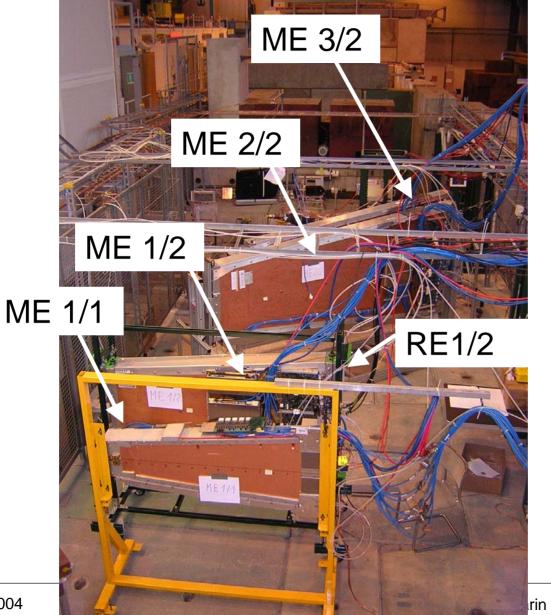


Even more goals added once started

- Test slow control (DCS) prototype
- Test data quality monitoring (DQM) prototype
- Test multiple peripheral crates
 - Toward a Slice Test of the CMS Endcap Muon system, where one peripheral crate corresponds to one disk
- Test multiple Sector Processors to one Muon Sorter
 - A 1/6 trigger "data challenge" of Track-Finder crate
 - Tests SP↔MS communication with real tracks
- Test new trigger primitive logic for anodes (ALCT) with ghost-busting improvements
- Spatial and HV scan of the Dubna ME1/1 chamber
- Unify TF and PC run control
- Add automated calls to DB to log run configuration
- Offline simulation of testbeam setup
- Injection of raw data into ORCA

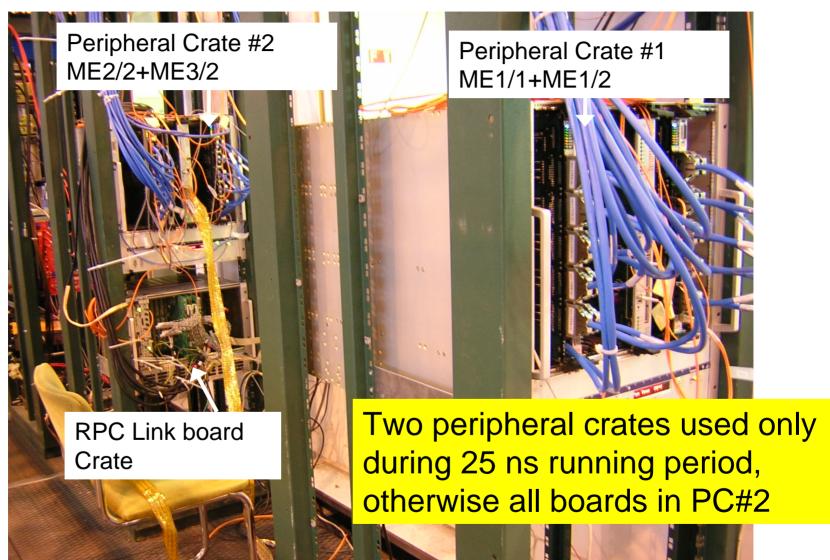


2004 CSC Beam Test Setup





Peripheral Electronics





Track-Finder, TTC & Trigger Electronics

TTCmi crate (machine interface for clock & orbit)



Machine clock and orbit signals only available during 25 ns run

We used Lev's XO for asynch period

TTC configuration

- Lindsey set up sending of spill start/stop signals in TTC asynchronous mode
- Lev & Mike set up synchronous TTC signals partway through 25 ns period

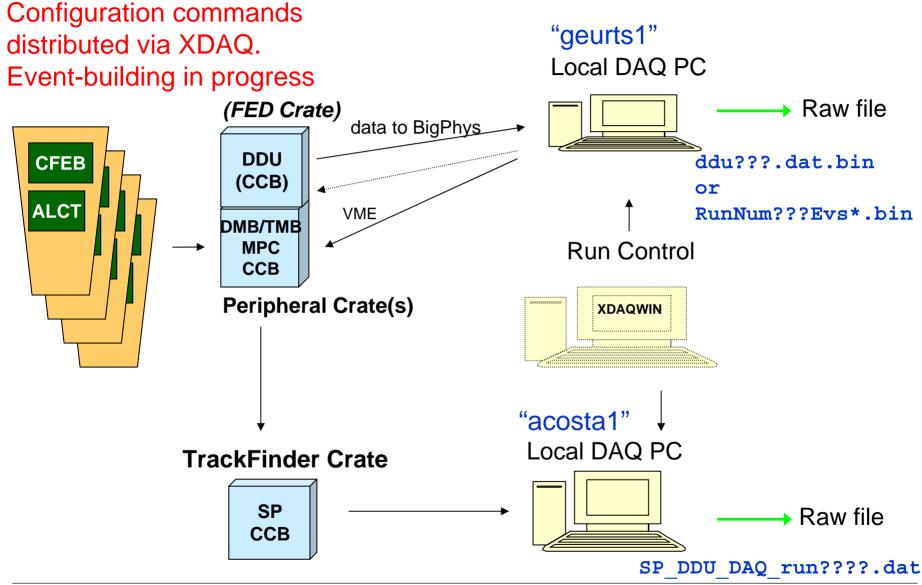
TTCvi crate

Level-1 Track-Finder crate





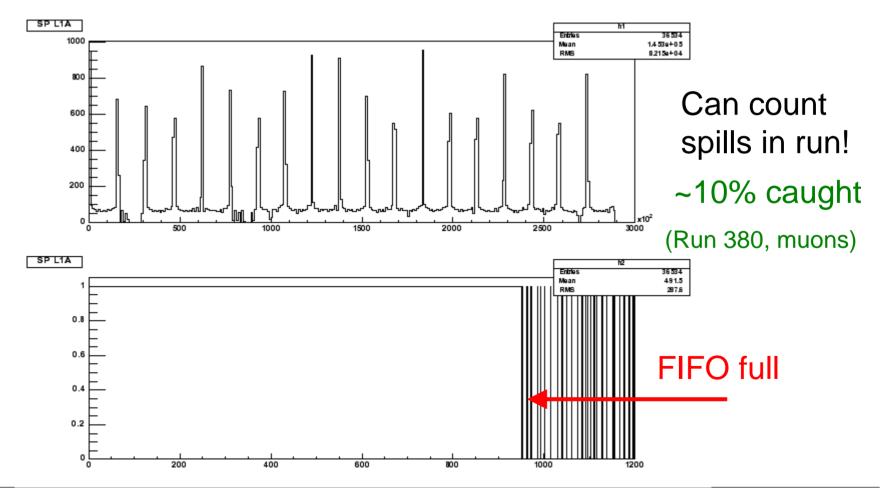
Test Beam 2004 DAQ Configuration





SP DAQ

The Track-Finder DAQ FIFO fills up because of slow VME readout (but complete record @ start of each spill)





The Integrated EMU GUI

		06-05-04 15:23:24,920 [1024] 06-05-04 15:23:26,82 [1026] II 06-05-04 15:23:26,121 [1026]
		GUIDriver XDAQ module \$Revisio
		GUIDriver_CTOR-INFO: Module lo
The Track-Fi	nder GUI has	CCB: Start Trigger
been extende	ed to include	CCB BCO CCB: BX-zero CCB: Enable TTC control CCB: CCDB (mach outfiller
the XDAQ-ba	CCB: CSRB1(read)=0xdff9changed CCB: Enable L1A CCB: CSRB1=0xdf70 TAKING DATA	
control syste		CCB: Disable LIA CCB: CSRB1 = 0xdff8 CCB: disable CCB: disable TTC control CCB: stop Trigger data taking disabled
Controls 4 cr	ates:	XDAQ output for host: acos
PC#1. PC#2.	TF. TTC	3/CSR1/1 3/CSR1/1 Enabled!

✓ =■ EMU Commander (the TFGUI-RunControl Lo

crate TTC Crate (http://acosta1:40000)
 crate TrackFinder Crate (http://acosta1:40000
 crate Peripheral Crate (http://geurts1:40100)

File XDAQ Edit View Help

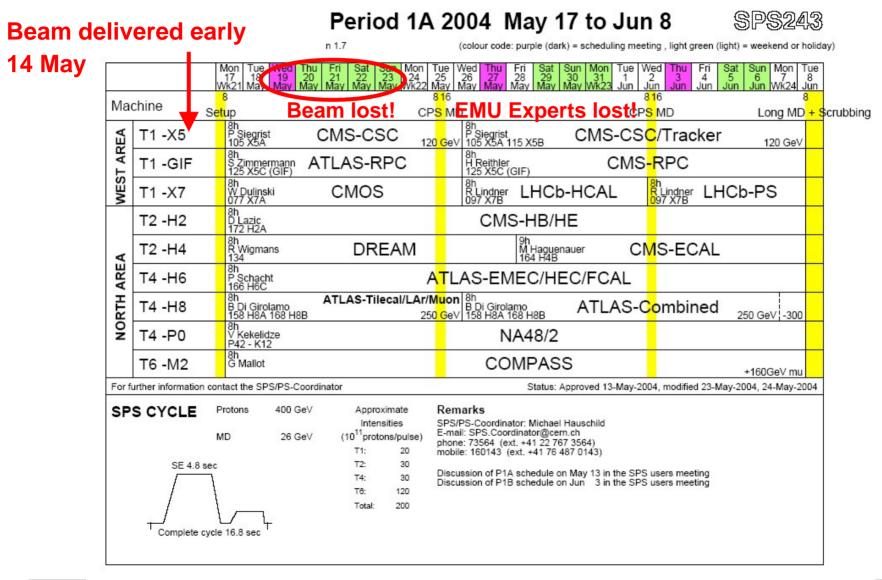
Is this a framework we should be working with for EMU Run Control?

] XDAQ output for host: acosta1:40000	🗗 📕 🛅 XDAQ errors for host: acosta1:40000
5-05-04 15:23:24,834 [1024] INFO [137.138.176.241:4	
6-05-04 15:23:24,860 [1024] INFO [137.138.176.241:4	
6-05-04 15:23:24,861 [1024] INFO [137.138.176.241:4	
6-05-04 15:23:24,865 [1024] INFO [137:138:176:241:4	
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6-05-04 15:23:24,887 [1024] INFO [137.138.176.241.4 6-05-04 15:23:24,920 [1024] INFO [137.138.176.241:4	
6-05-04 15:23:26,82 [1026] INFO [137.138.176.241:40	2000] 📄 CMS Beam Test Run Control 🖉 🖬
06-05-04 15:23:26,121 [1026] INFO [137.138.176.241:4	Help

GUIDriver XDAQ module \$Revision: 1.8 \$	Struct XML:
	Sequence File: Reset
GUIDriver_CTOR-INFO: Module load successful	
	Hardware Config File:
	Number of Events: 1500
	🐖 」 Set Run Type: 🗨
XDAQ output for host: geurts1:40100	
alling DDUttend	
XR and EVTCNTRST	Set Run Number: 0 🔲 Automatic Run #
CB: Start Trigger	
CB BC0	Choose Command: UckeyeShiftTest 🔻 Choose Board: DAQMB 💌
CB: BX-zero	
CB: Enable TTC control	Slot Number: Crate Number:
:CB: CSRB1(read)=0xdff9changed to CSRB1(set)=0xdff8	
CB: Enable L1A	Read XML File:
CB: CSRB1=0xdf70	
AKING DATA	
CB: Disable L1A	Setup Start Stop Execute
CB: CSRB1=0xdff8	
CB: disable	Events: 1500 Type: Uninit
CB: disable TTC control	
CB: Stop Trigger	Run #: 0 Status: Ready
lata taking disabled	
	s1
XDAQ output for host: acosta1:40100	ピ 🔐 🧮 XDAQ errors for host: acosta1:40100
ADAU UULDUL IUI NUSC ALUSLAI:40100	
7(5K1/1	
7CSK1/1 //CSR1/1	
7(5K1/1	
7CSR1/1 /CSR1/1 habled!	
7CSR1/1 /CSR1/1 nabled! Isabling TF and TTC Crates!	
7CSR1/1 /CSR1/1 nabled! isabling TF and TTC Crates! /B_GO_3_MODE/11	
/CsR1/1 /CSR1/1 nabled lisabling TF and TTC Crates! /8_GO_3_MODE/11 /8_GO_2_MODE/11	
7CSR1/1 /CSR1/1 nabledl Hsabling TF and TTC Cratesl /B_GO_3_MODE/11 /B_GO_1_MODE/11 /B_GO_1_MODE/11	
/CsR1/1 /CSR1/1 nabledl //B_GO_3_MODE/11 //B_GO_2_MODE/11 //B_GO_1_MODE/11 //B_GO_0_MODE/11 //B_GO_0_MODE/11	
TCSR1/1 /CSR1/1 nabledl isabling TF and TTC Crates! /B_GO_3_MODE/11 /B_GO_2_MODE/11 /B_GO_1_MODE/11 /B_GO_0_MODE/11 /CSR1/0	
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/CsR1/1 /CSR1/1 nabledl //s.GO.3.MODE/11 //s.GO.2.MODE/11 //s.GO.2.MODE/11 //s.GO.0.MODE/11 //s.GO.0.MODE/11 //LAR/12 /L1AR/12 /L1AR/12 2/CSRB1/57080 2/CSRB1/57080	
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TCSR11 TCSR11 TCSR11 isabling TF and TTC Crates! (8_G0_3_MODE/11 18_G0_1_MODE/11 18_G0_1_MODE/11 18_G0_0_MODE/11 15_571/0 1_L1AR/12 1_CSR1/57080 2/CSR81/57080	
SR1/1 SR1/1 SR2/1 sabled sabled sabled SG0_3_MODE/11 B_G0_1_MODE/11 B_G0_1_MODE/11 B_G0_1_MODE/11 CSR1/0 L1AR/12 L1AR/12 L1AR/12 L1AR/12 CSR81/57080 //VM/MA/CSR_FCC/0 /VM/MA/CSR_FCC/0 /VM/MA/CSR_FCC/0	
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CKT/1 CSR1/1 abled sabling TF and TTC Crates! B_GO_3_MODE/11 B_GO_2_MODE/11 B_GO_1_MODE/11 CSR1/0 L1AR/12 L1AR/	



May Test Beam Schedule





Configuration During Asynch Period

- Single peripheral crate configuration for all four TMB's + DMB's (+ DDU)
- CCB2004 in FPGA mode
- Scintillator-based L1A
- Muon beam only
- Most runs were ALCT studies varying chamber angles and ALCT parameters
 - Early runs recorded only by Track-Finder

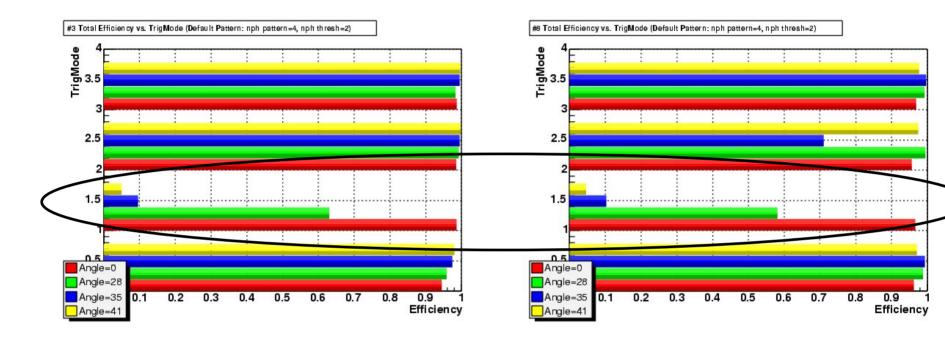


ALCT Variations

		all chambers	ALCT	CSC10					CSC1					CSC3					
"Run"	Nevents	ALCT Delay	firmware	Theta	patterns	trig mod	le nph pat	ttern nph three	sh Theta	patterns	trig mode	nph pattern	nph thres	h Theta	patterns	trig mod	le r		
72		0 ns	old		0 default		2	4	2	0 default		2 4		2	0 default		2		
73		5 ns	old		0 default		2	4	2	0 default	2	2 4		2	0 default	2	2		
74		10 ns	old		0 default		2	4	2	0 default		2 4		2	0 default		2		
75		15 ns	old		0 default		2	4	2	0 default		2 4		2	0 default	0	2		
76		20 ns	old	_	0 1 5 1		CSC1		0	0 1 2 1		CSC3		r	0 1 5 1		CSC8		
77		25 ns	old	Dur		Maurata			Anter annuale		and thereb					and there is		1	
78		30 ns	old	Run	000	Nevents	Theta		trig_mode 2		nph_thresh		patterns	trig_mode n	pn_pattern r	1pn_thresh 2	Theta	34 d	atterns
					238			0 default		4			default	2	4				
trigmode0		6 ns ?	old		239			0 default	2		-		miss4	2		2		34 m	
trigmode1		6 ns ?	old		240			0 default	2	4			miss4	2	5	2		34 m	
trigmode2		6 ns ?	old		241	_		0 default	2	4	-		miss4	0	5	2		34 m	
trigmode3		6 ns ?	old		242			0 default	2	4	-		miss4	1	5	2		34 m	
					243		15	0 default	2	4	2		miss4	3	5	2		34 m	
newFW trigmode0		6 ns ?	new		244			0 default	2	4	-		miss4	1	4	2		34 m	
newFW trigmode1		6 ns ?	new		245			0 default	2	4	-		miss4	1	4	2		34 m	
newFW trigmode2		6 ns ?	new		246			0 default	2	4	-		miss4	3	4	2	1	34 m	
newFW trigmode3		6 ns ?	new		247			0 default	2	4	. 2	34	miss4	0	4	2		34 m	niss4
patt5 6 0deg trigmo	de0	6 ns ?	new				CSC1					CSC3					CSC8		
patt5 6 0deg trigmo	de1	6 ns ?	new	Run		Nevents	Theta	patterns		nph_pattern	nph_thresh		patterns	trig_mode n	ph_pattern r	nph_thresh	Theta		atterns
patt5 6 0deg trigmo		6 ns ?	new		248			0 default	2	4	-		andrey	0	4	2	-	34 a	ndrey
patt5 6 0deg trigmo	de3	6 ns ?	new		249			0 default	2	4			andrey	1	4	2		34 a	ndrey
					250		2	0 default	2	4	2	34	andrey	2	4	2		34 a	ndrey
25deg trigmode0		6 ns ?	new		251			0 andrey	2	4	2	34	andrey	2	4	2		34 a	ndrey
25deg trigmode1		6 ns ?	new		252			0 andrey	0	4	2	34	andrey	0	4	2		34 a	ndrey
25deg trigmode2		6 ns ?	new		253			0 andrey	1	4	2	34	andrey	1	4	2		34 a	ndrey
25deg trigmode3		6 ns ?	new		254			0 andrey	3	4	2	34	andrey	3	4	2		34 a	ndrey
0_ 0					255			0 andrey	3	5	2	34	andrey	3	5	2		34 a	ndrey
IB trigmode0		6 ns ?	new		256			0 andrey	2	5	2	34	andrey	2	5	2		34 a	ndrey
IB trigmode0		6 ns ?	new		257			0 andrey	1	5	2	34	andrey	1	5	2		34 a	ndrey
IB trigmode0		6 ns ?	new		258			0 andrey	0	5	2	34	andrey	0	5	2	5	34 a	ndrey
IB trigmode0		6 ns ?	new		259			0 andrey	2	4	2	34	andrey	2	4	2		34 a	ndrey
	2				260			0 andrey	0	5	2	34	andrey	0	5	2		34 a	ndrey
patt5_6_25deg_trigm	ode0	6 ns ?	new										,				×		
patt5 6 25deg trigm		6 ns ?	new			Track-Find	er studies:												
patt5 6 25deg trigm		6 ns ?	new				CSC1					CSC3					CSC8		
patt5 6 25deg trigm		6 ns ?	new	Run		Nevents	Theta	patterns	trig mode	nph pattern	nph_thresh		patterns	trig mode n	ph pattern r	nph thresh	Theta	p	atterns
					261			0 andrey	2	4			andrey	2	4	2			ndrey
35deg trigmode0		6 ns ?	new		262		2	0 andrey	2	4			andrey	2	4	2			ndrey
35deg trigmode1		6 ns ?	new		263			0 andrey	2	4			andrey	2	4	2			ndrey
35deg trigmode2		6 ns ?	new		264		5	0 andrey	2	4			andrey	2	4	2			ndrey
35deg trigmode3		6 ns ?	new		265			0 andrey	2	4	-		andrey	2	4	2			ndrey
<u> </u>					265			0 andrey	2	4	-		andrey	2	4	2			ndrey
141		0	0		260			0 andrey	2	4	2		andrey	2	4	2			ndrey
					268			0 andrey	2	4			andrey	2	4	2			ndrey
					269		5	0 andrey	2	4			andrey	2	4	2			ndrey
					203		2	0 andrey	2	4			andrey	2	4	2			ndrey
					270		5	0 andrey	2	4			andrey	2	4	2	-		ndrey
					271		1	0 andrey	2	4			andrey	2	4	2			ndrey
18.lı	ine 20	04	USCM		272			0 andrey	2	4				2	4	2			
					213			o andrey	2	4	·	34	andrey	2	4	2	2	J4 a	ndrey



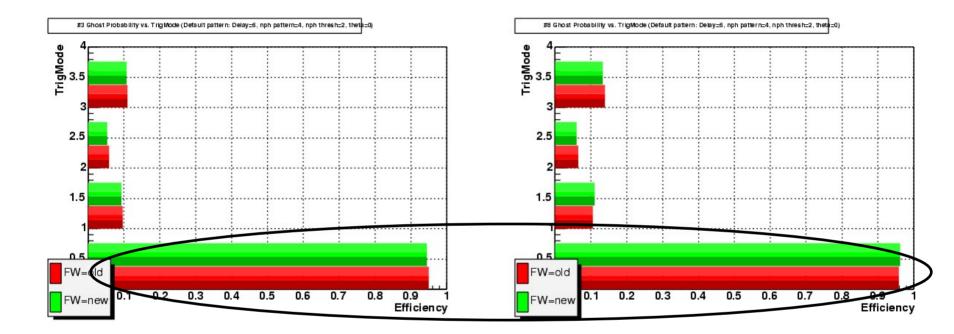
ALCT Efficiency



Accelerator pattern efficiency (straight tracks in WG) decreases with angle as you would expect



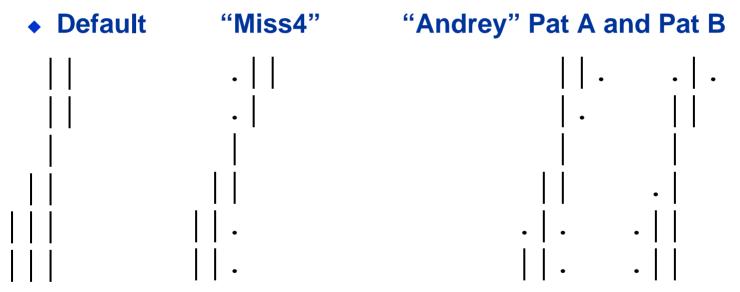
ALCT Ghost Rate



Ghost rate very high if accelerator patterns and collision patterns both enabled without ghost cancellation mode (would flood MPC)



- Several other ALCT parameters were varied and will be studied by REU student
- For example, ALCT Patterns:



 Goal is to achieve high efficiency, low ghost rate, and good discrimination between collision and accelerator patterns



- Can check MPC winner bits recorded by TMB in DDU data with that expected by MPC simulation
 - e.g. I wrote some code to do this check, putting LCT data on correct relative BX and running an MPC simulation based on 4 chamber input:
 - Conclusion: only 193 mismatches in 79408 events (0.25%)
 - Stale LCT data bug might have affected this
- Check LCTs reported by TMB in DDU data with that received by SR/SP, after running through MPC simulation
 - Last year had ~99.7% agreement
 - Still needs to be done for this year's data
 - Early check found ~97% agreement
- SP Track-Finding logic validation
 - Compare reported tracks with simulation
- Muon Sorter logic validation

Use 25 ns run data



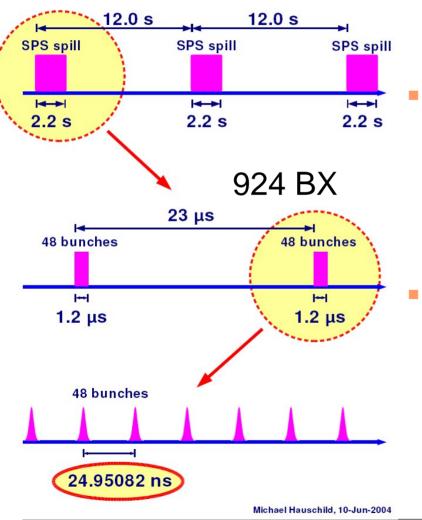
June Test Beam Schedule (25 ns)

SPS Operation Period 1B 2004 Jun 8 to Jul 1 SPS244 Schedule issue date: 3-Jun-2004 Version 1.7 (colour code; purple (dark) = scheduling meeting , light green (light) = weekend or holiday) Sat 12 Jun Sun 13 Jun Fri 18 Jun Mon 21 Wk26 Tue 22 Wed 23 Mon 28 Wk27 Tue 29 Jun Wed 30 Jun Wed Mon Wed Sun 20 Jun Fri 25 Jun Sat 26 Jun Sun 27 Jun Tue Fri Tue Sat 19 Thu 8 Ĩ 10 11 14 Wk25 15 16 Jun Jūn Jun Jun Jun Jun 10 ⁸--25ns---25ns---25ns---25ns--⁸ Machine Long MD + Scrubbing Scrubbing + Tech Stop Long MD 8h P Sieges MS-CSC/Tracker 105 X5A 115 X5B 120 GeV 8h ALICE-HMPID P Martinengo 105 X5A 120 GeV AREA T1 -X5 P Martinengo 125 X5C (GIF) H Reithler CMS-RPC ALICE-RPC T1 -GIF NEST 8h R Lindner 097 X7B 8h LHCb-HCAL free T1 -X7 8h D Lazic 172 H2A 8h D Lazic CMS-HB/HE/HO 172 H2A CMS-HF T2 -H2 8h M Haguenal MS-ECAL 164 H4B 8h M Haguenaue 164 H4B CMS-ECAL T2 -H4 ∢ ARE/ 8h h ATLASPEMEC/HEC/FCAL BAS-EMEC/HEC/FCAL T4 -H6 166 H6C 166 H6C 1268h A' B Di Girolamo 158 H8A 168 H8B NORTH 8h ATLAS-Combined ATLAS-Pixel T4 -H8 M Cobal +180 GeV 138 +180 GeV (high int.) 8h V Kekelidze 8h V Kekelidze NA48/2-calibration NA48/2 T4 - P0 P42 - K12 P42 - K12 8h G Mallot 8h G Mallot COMPASS-calibration COMPASS T6 - M2 +160GeV mu +160GeV mu For further information contact the SPS/PS-Coordinator Status: Approved 3-Jun-2004 Remarks SPS CYCLE Protons 400 GeV Approximate Intensities SPS/PS-Coordinator: Michael Hauschild E-mail: SPS.Coordinator@cern.ch (10¹¹protons/pulse) MD 26 GeV phone: 73564 (ext. +41 22 767 3564) T1: 2 mobile: 160143 (ext. +41 76 487 0143) SE 4.8 sec T2: 2 Discussion of P1B schedule on Jun 3 in the SPS users meeting T4: 2 Discussion of P1C schedule on Jun 24 in the SPS users meeting 2 T6: Jun 14 - Jun 21: 8 Total: 25ns bunched proton beam: 48 bunches, 400 GeV, 12.0 sec cycle, 2.2 sec spill length Complete cycle 16.8 sec



25 ns Structured Beam

25ns Structured Beam 2004



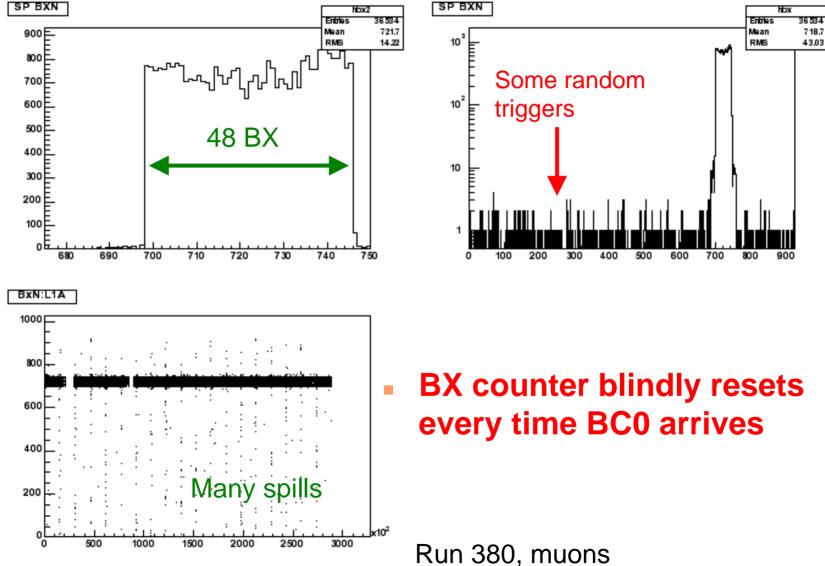
LHC-like bunch structure during synchronous running

Trigger rates at X5A during spill

- Muons: 3–10 kHz
- Pions: >100 kHz
- CSC readout system is designed for a L1A*LCT rate at LHC design luminosity of order 5 kHz



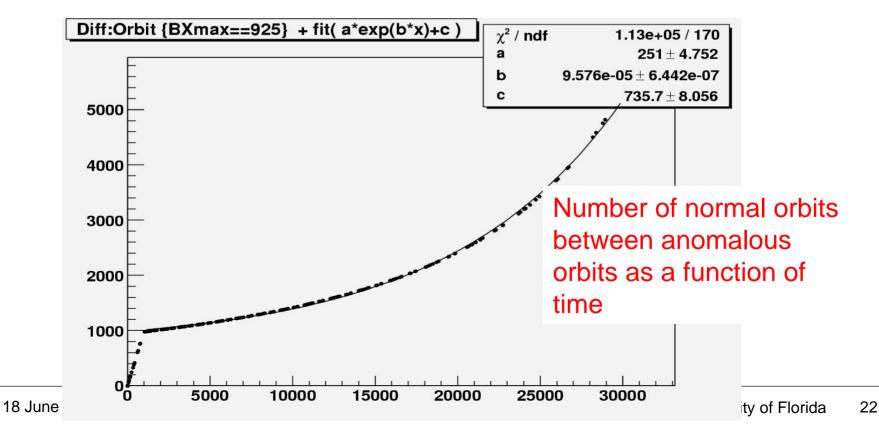
Sector Processor BX Distribution





Orbit Signal Varies?

- Lev's BX counter in SP initially did not blindly reset on each BC0 as did all other boards. Instead, he checked if BC0 came when counter rolled over to BX0.
 - This was not always the case! Sometimes orbit is 923 or 925 BX
 - Seen simultaneously in two SP's



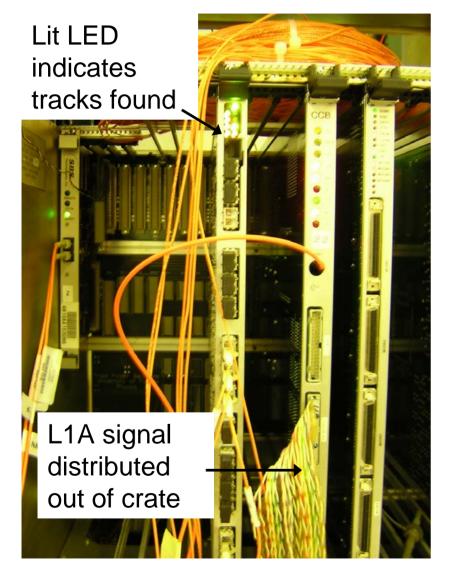


Configuration During 25 ns Period

- Went to 2 Peripheral Crate setup
 - PC #1: ME1/1 + ME1/2 (with RAT)
 - PC #2: ME2/2 + ME3/2
- TMB logic updated ⇒ New data format!
 - Accommodates RPC data, fixes stale data bug
 - Breaks RootEventDisplay?
- Went to discrete logic mode on CCB (runs > 293)
 - No programmable L1A delay (done in CCB2001 for TF L1A)
- Went to Track-Finder trigger (runs > 291)
 - Generally triggered on ME2/2+ME3/2
 - Aligned chambers in SR LUTs, but some features:
 - Can trigger on 1 chamber with ghost segment on second link
 - Accidentally had η offset in ME1
 - Never tried "transparent" mode of MPC (routing of specific MPC inputs to MPC outputs)
 - ◆ Sensitive to entire beam profile ⊗ CSC coverage:
 - Muon trigger rate increases from ~6500/spill to ~17000/spill
 - Pion trigger rate decreases from 240K/spill to 175K/spill (effect of η offset problem?)



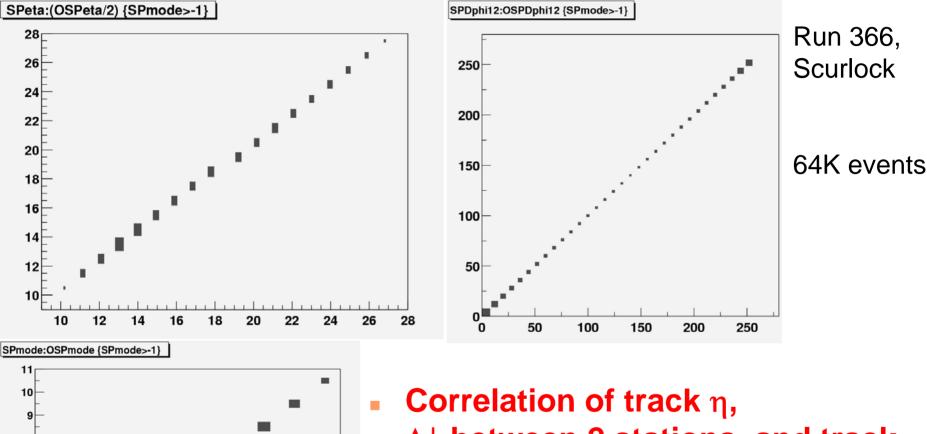
Track-Finder Tests



- First time we tested with full Track-Finding logic to identify tracks in data
- Full DAQ logging of inputs and outputs for offline comparisons
 - Can compare with data sent by Peripheral Crates as well as internal TF logic
- L1A generation a major synchronization accomplishment for trigger
 - Data must be aligned spatially and temporally
 - Very useful for slice tests



SP: ORCA vs. Hardware Check



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g

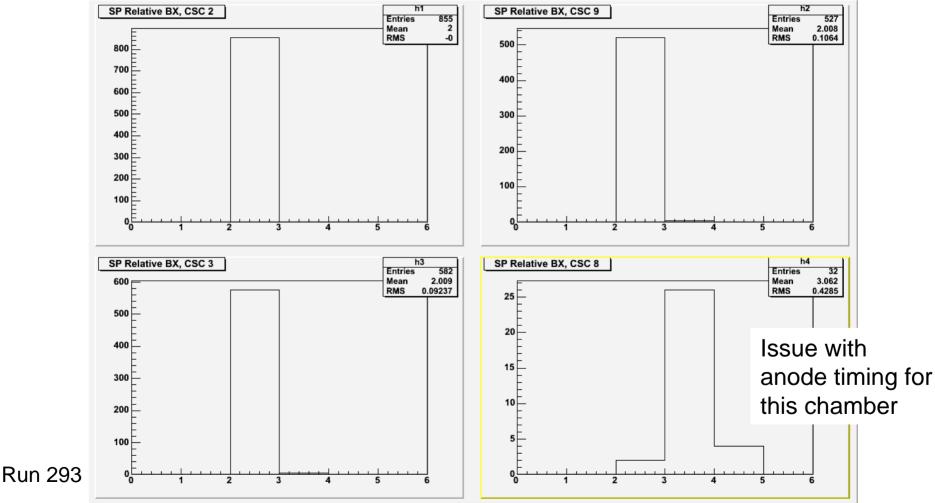
5

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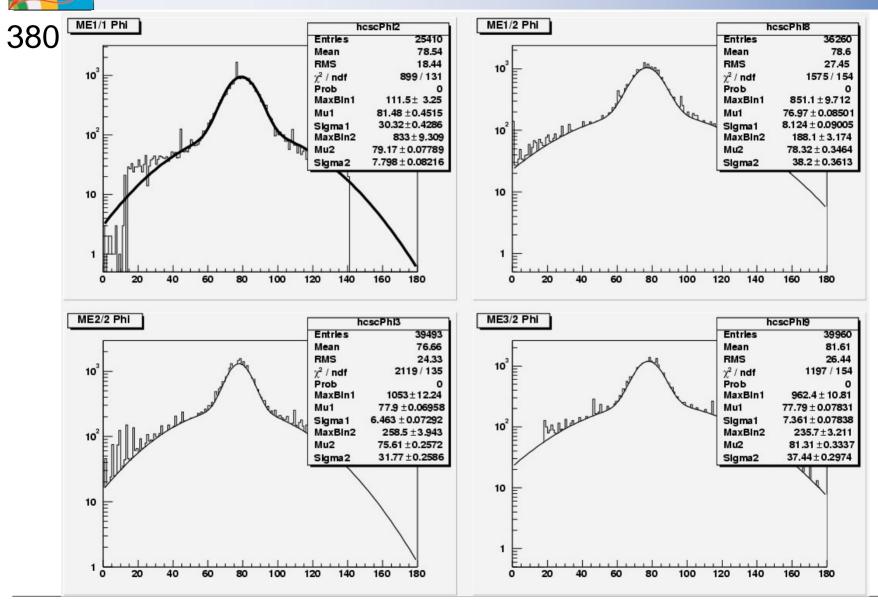
 $\Delta \phi$ between 2 stations, and track η, Δφ between 2 stations, and track type agrees perfectly between hardware and ORCA simulation

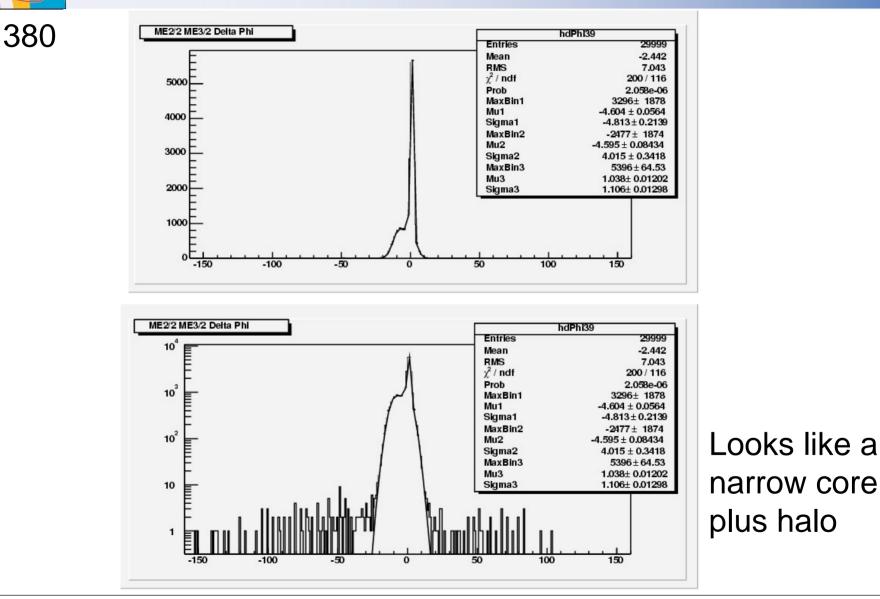
Time Alignment of CSC data in Track-Finder

Able to get all trigger data from multiple chambers and crates on same BX (at least for some runs):



Spatial Distribution in ϕ of Beam







Track-Finder Crate Tests Cont'd



- First test of multiple peripheral crates to TF crate
 - Synchronization test
- Various clocking solutions tried to test robustness of optical links
 - MPC used QPLL 80 MHz clock on backplane for 25 ns runs?

First test of multiple Sector Processors to one Muon Sorter

 Detailed offline checks of exchanged data should follow to validate boards



- Integration of DCS with Run Control system
 - Both systems tested are incompatible with each other
 - Eventually a common framework is needed
- Synchronization
 - Still more of an art than a science
 - For example, if I change the ALCT delay, LCT data moves on trigger path but is lost on DAQ path!
 - Eventually need a system-wide understanding and agreement on how this is done
 - BX counters: does software keep tracks of offsets, or does firmware synch-in so that BC0 means the 0th BX on each board?
 - Can procedure be automated?



System Issues (Cont'd)

DAQ data integrity

- The problems we have in unpacking software reflect that we sometimes have unexpected (corrupted) event data
- Rate dependent, but still observed at low rates
- Is this a feature of our DAQ?
- Eventually should have ways to monitor these problems



- Fall beam test offers a chance to correct some problems we had with May/June tests, and re-run
- Should be careful not to re-do too much, or 1 week may not be enough time to get everything working
- Should be careful not to get too distracted with HCAL synchronization
 - I think two separate subsystems, triggered by TF, and separately logging data is achievable
 - We do it already between PC and TF crates, and also with RPC system
 - Merging run control and DAQ systems should be done inasmuch as we think is on path for EMU development

Next test beam coordinator ought to be someone responsible for some of the overall system issues



Fall Schedule

