TMB 2004 Design

UCLA High Energy Physics
Version 2.01
June 9, 2004

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Changes from TMB2001

	Old TMB2001	New TMB2004
FPGA	Xilinx XCV1000E	Xilinx XC2V4000
EPROMs	2 x 18V04	4 x 18V04
Clock Delays	2 x PHOS4, 10 channels	3 x 3D3444, 12 channels with duty cycle correction
Voltage Regulators	+3.3V,+1.8V Not tested for rad tolerance	+1.8V,+1.5V/+1.2V Tested rad tolerant
Voltage Protection	Zener	MOSFET
RPC	Not implemented	RAT2004 Transition Module Receives 4 RPC link boards
ALCT Cables	Front panel entry	RAT2004 Transition Module and front panel entry

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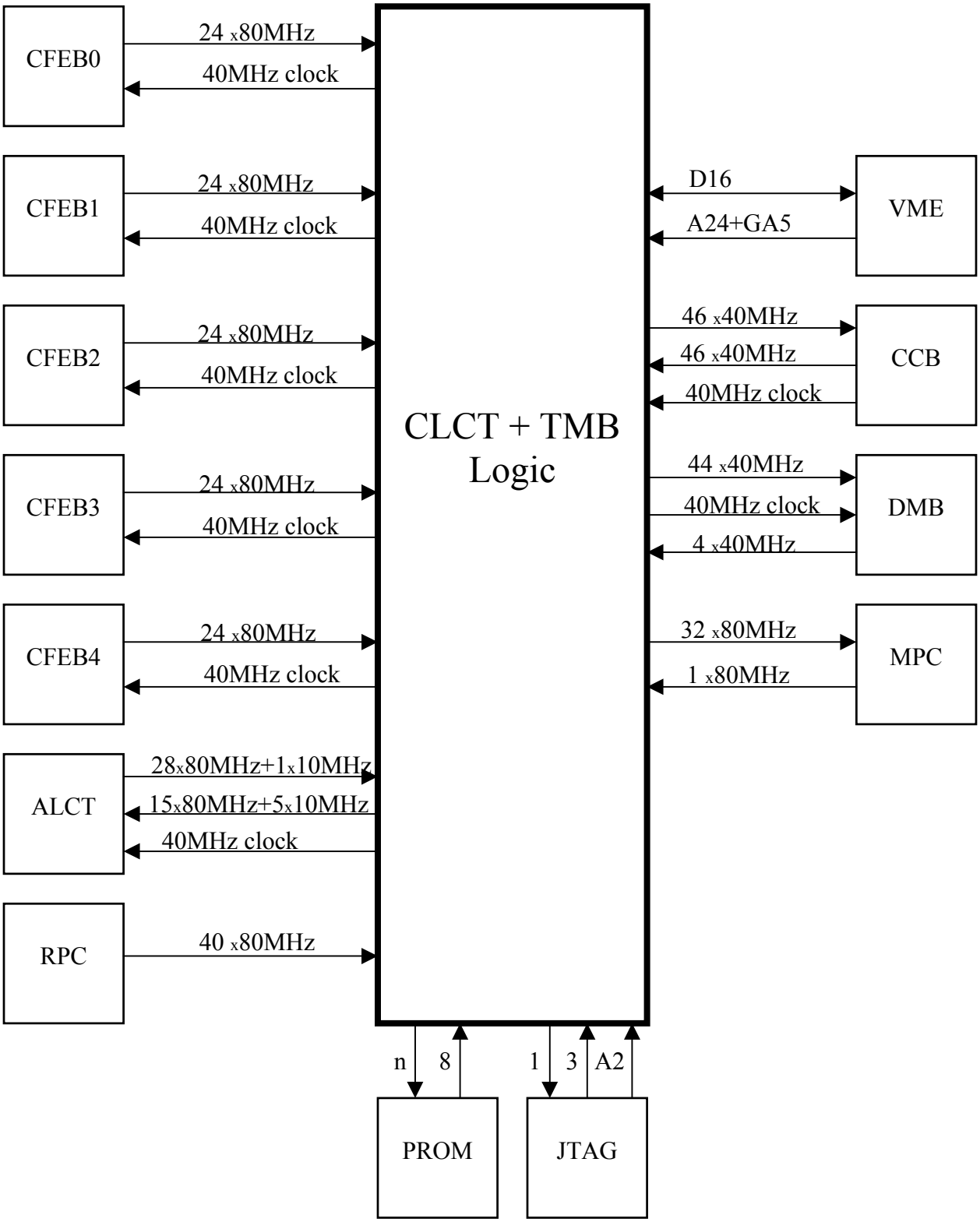
TMB Overview

Figure 1 TMB Overview



Cathode LCT Algorithm
(documentation incomplete 6/9/2004)

CFEB Demultiplex
(documentation incomplete 6/9/2004)

Triad Decode
(documentation incomplete 6/9/2004)

Layer Staggering
(documentation incomplete 6/9/2004)

DiStrip OR
(documentation incomplete 6/9/2004)

Pattern Cell Envelope
(documentation incomplete 6/9/2004)

Hit pattern LUTs for 1 layer: - = don't care, xxx= any one or more ½-strips hit

```
Default Cell Envelope
Key on Ly3
-------------
hs   0123 LUT
ly0  xxx- FEFE
ly1  xxx- FEFE
ly2  xxx- FEFE
ly3  -x-- CCCC
ly4  xxx- FEFE
ly5  xxx- FEFE
```

Priority Enocoding
(documentation incomplete 6/9/2004)

DiStrip Patterns
(documentation incomplete 6/9/2004)

DMB Active FEB Signal
(documentation incomplete 6/9/2004)

Best 2 LCTs
(documentation incomplete 6/9/2004)

CLCT Bend Patterns

(documentation incomplete 6/9/2004)

Hit pattern LUTs for 1 layer: - = don't care, x=one ½-strip hit, xx= one hit or the other or both

```
½-StripID=0123 LUT (look-up table contents)
Layer0    --x- F0F0
Layer1    --x- F0F0
Layer2    -xx- FCFC
Layer3    -x-- CCCC
Layer4    xx-- EEEE
Layer5    x--- AAAA
```

```
Pattern 7          Pattern 6          Pattern 5          Pattern 4          Pattern 3          Pattern 2          Pattern 1
-------------      -------------      -------------      -------------      -------------      -------------      -------------
hs   0123 LUT      hs   0123 LUT      hs   0123 LUT      hs   0123 LUT      hs   0123 LUT      hs   0123 LUT      hs   0123 LUT
ly0  -x-- CCCC     ly0  x--- AAAA     ly0  --x- F0F0     ly0  -x-- CCCC     ly0  -x-- CCCC     ly0  x--- AAAA     ly0  --x- F0F0
ly1  -x-- CCCC     ly1  x--- AAAA     ly1  --x- F0F0     ly1  -x-- CCCC     ly1  -x-- CCCC     ly1  x--- AAAA     ly1  --x- F0F0
ly2  -x-- CCCC     ly2  xx-- EEEE     ly2  -xx- FCFC     ly2  -x-- CCCC     ly2  -x-- CCCC     ly2  xx-- EEEE     ly2  -xx- FCFC
ly3  -x-- CCCC     ly3  -x-- CCCC     ly3  -x-- CCCC     ly3  -x-- CCCC     ly3  -x-- CCCC     ly3  -x-- CCCC     ly3  -x-- CCCC
ly4  -x-- CCCC     ly4  -x-- CCCC     ly4  -x-- CCCC     ly4  --x- F0F0     ly4  x--- AAAA     ly4  -xx- FCFC     ly4  xx-- EEEE
ly5  -x-- CCCC     ly5  -x-- CCCC     ly5  -x-- CCCC     ly5  --x- F0F0     ly5  x--- AAAA     ly5  --x- F0F0     ly5  x--- AAAA
```

Drift Delay

(documentation incomplete 6/9/2004)

CLCT Format

(documentation incomplete 6/9/2004)

ALCT+CLCT Matching Algorithm

(documentation incomplete 6/9/2004)

Matching Logic

(documentation incomplete 6/9/2004)

LCT Duplication

(documentation incomplete 6/9/2004)

```
// Fill in missing ALCT if CLCT has 2 muons, missing CLCT if ALCT has 2 muons
wire    no_alct  = !alct0_vpf;
wire    no_clct  = !clct0_vpf;

wire    one_alct = alct0_vpf && !alct1_vpf;
wire    one_clct = clct0_vpf && !clct1_vpf;

wire    two_alct = alct0_vpf && alct1_vpf;
wire    two_clct = clct0_vpf && clct1_vpf;

wire    dupe_alct = one_alct && two_clct;
wire    dupe_clct = one_clct && two_alct;

wire    [MXALCT-1:0]   alct_dummy = clct0_real[18:17] << 11;              // Inserts clct bxn into
wire    [MXCLCT-1:0]   clct_dummy = 0;                                    // frame for clct_only events

wire    [MXALCT-1:0]   alct0 = (no_alct  ) ? alct_dummy : alct0_real;     // Substitute dummy alct
wire    [MXALCT-1:0]   alct1 = (dupe_alct) ? alct0_real : alct1_real;

wire    [MXCLCT-1:0]   clct0 = (no_clct  ) ? clct0_real : clct0_real;     // Do not
wire    [MXCLCT-1:0]   clct1 = (dupe_clct) ? clct0_real : clct1_real;

wire first_vpf         = alct0_vpf || clct0_vpf;                          // First muon exists
wire second_vpf        = alct1_vpf || clct1_vpf;                          // Second muon exists
```

LCT Quality

(documentation incomplete 6/9/2004)

```
assign first_nlayers  = (alct_first_quality  + 3) + clct_first_nhit;
assign second_nlayers = (alct_second_quality + 3) + clct_second_nhit;

// Construct 1st LCT quality
reg     [3:0]  lct_first_quality;

always @(tmb_match or tmb_clct_only or tmb_alct_only or
         alct_first_amu or clct_first_hsds or first_nlayers)
begin
if (tmb_match && clct_first_hsds && first_nlayers >= 8)     // ALCT & CLCT match, CLCT 1/2-strip pattern
 lct_first_quality = 4'b1011 + first_nlayers[3:0]-8;

else if (tmb_match && !clct_first_hsds && first_nlayers >= 8)// ALCT & CLCT match, CLCT DiStrip pattern
 lct_first_quality = 4'b0110 + first_nlayers[3:0]-8;

else if (tmb_clct_only && clct_first_hsds)                  // CLCT no ALCT, CLCT 1/2-strip pattern
         lct_first_quality = 4'b0101;

else if (tmb_clct_only && !clct_first_hsds)                 // CLCT no ALCT, CLCT DiStrip pattern
         lct_first_quality = 4'b0100;

else if (tmb_alct_only)                                     // ALCT only
         lct_first_quality = 4'b0011;

else if (tmb_match && alct_first_amu)
        lct_first_quality = 4'b0010;

else if (tmb_alct_only && alct_first_amu)
         lct_first_quality = 4'b0001;

else
         lct_first_quality = 4'b000;
        end
```

MPC Format

(documentation incomplete 6/9/2004)

VME Registers

Addressing Modes

TMB2001 responds to A24D16 VME addressing modes:

Address Modifier 39_{16}, A24 non-privileged mode
Address Modifier $3D_{16}$, A24 supervisor mode

It does not respond to byte-addressing modes, so all valid addresses must be even numbers.

Base Address

TMB2001s "base address" bits A[23:19] select which TMB is being addressed by the VME crate controller. The base address is determined either by 5 VME-slot Geographic Address bits or by the Local Address set by two on-board hexadecimal rotary switches. Shunt SH62 selects between Geograpic [1-2] and Local [2-3] modes.

A[23:19] = VME Crate Slot Geographic Address, (Slot= 2 to 21)$_{10}$	SH62 [1-2]
A[23:19] = Hexadecimal Switch Address SW2x16+SW1	SH62 [2-3]

Multiple TMBs can be addressed simultaneously using a Global Address:

A[23:19] = 26_{10} Addresses all TMBs in parallel
A[23:19] = 27_{10} Address all peripheral crate modules

The Hardware Bootstrap Register has a special mode where it can use the Local Address set by the hexadecimal rotary switches as its Global Address

Register Addresses

Address Hexadecimal Add to Base	Register Name	Description
70000	ADR_BOOT	Hardware Bootstrap Register
00	ADR_IDREG0	ID Register 0
02	ADR_IDREG1	ID Register 1
04	ADR_IDREG2	ID Register 2
06	ADR_IDREG3	ID Register 3
08	ADR_VME_STATUS	VME Status Register
0A	ADR_VME_ADR0	VME Address read-back
0C	ADR_VME_ADR1	VME Address read-back
0E	ADR_LOOPBK	Loop-back Register
10	ADR_USR_JTAG	User JTAG
12	ADR_PROM	PROM
14	ADR_DDDSM	3D3444 State Machine Register + Clock DCMs
16	ADR_DDD0	3D3444 Delay Chip 0
18	ADR_DDD1	3D3444 Delay Chip 1
1A	ADR_DDD2	3D3444 Delay Chip 2
1C	ADR_DDDOE	3D3444 Delay Chip Output Enables
1E	ADR_RATCTRL	RAT Module Control
20	ADR_STEP	Step Register
22	ADR_LED	Front Panel +On-Board LEDs
24	ADR_ADC	ADCs
26	ADR_DSN	Digital Serials
28	ADR_MOD_CFG	TMB Configuration
2A	ADR_CCB_CFG	CCB Configuration
2C	ADR_CCB_TRIG	CCB Trigger Control
2E	ADR_CCB_STAT	CCB Status
30	ADR_ALCT_CFG	ALCT Configuration
32	ADR_ALCT_INJ	ALCT Injector Control
34	ADR_ALCT0_INJ	ALCT Injected ALCT0
36	ADR_ALCT1_INJ	ALCT Injected ALCT1
38	ADR_ALCT_STAT	ALCT Sequencer Control/Status
3A	ADR_ALCT0_RCD	ALCT LCT0 Received by TMB
3C	ADR_ALCT1_RCD	ALCT LCT1 Received by TMB
3E	ADR_ALCT_FIFO	ALCT FIFO RAM Status
40	ADR_DMB_MON	DMB Monitored signals

42	ADR_CFEB_INJ	CFEB Injector Control
44	ADR_CFEB_INJ_ADR	CFEB Injector RAM address
46	ADR_CFEB_INJ_WDATA	CFEB Injector Write Data
48	ADR_CFEB_INJ_RDATA	CFEB Injector Read Data
4A	ADR_HCM001	CFEB0 Ly0,Ly1 Hot Channel Mask
4C	ADR_HCM023	CFEB0 Ly2,Ly3 Hot Channel Mask
4E	ADR_HCM045	CFEB0 Ly4,Ly5 Hot Channel Mask
50	ADR_HCM101	CFEB1 Ly0,Ly1 Hot Channel Mask
52	ADR_HCM123	CFEB1 Ly2,Ly3 Hot Channel Mask
54	ADR_HCM145	CFEB1 Ly4,Ly5 Hot Channel Mask
56	ADR_HCM201	CFEB2 Ly0,Ly1 Hot Channel Mask
58	ADR_HCM223	CFEB2 Ly2,Ly3 Hot Channel Mask
5A	ADR_HCM245	CFEB2 Ly4,Ly5 Hot Channel Mask
5C	ADR_HCM301	CFEB3 Ly0,Ly1 Hot Channel Mask
5E	ADR_HCM323	CFEB3 Ly2,Ly3 Hot Channel Mask
60	ADR_HCM345	CFEB3 Ly4,Ly5 Hot Channel Mask
62	ADR_HCM401	CFEB4 Ly0,Ly1 Hot Channel Mask
64	ADR_HCM423	CFEB4 Ly2,Ly3 Hot Channel Mask
66	ADR_HCM445	CFEB4 Ly4,Ly5 Hot Channel Mask
68	ADR_SEQ_TRIG_EN	Sequencer Trigger Source Enables
6A	ADR_SEQ_TRIG_DLY0	Sequencer Trigger Source Delays
6C	ADR_SEQ_TRIG_DLY1	Sequencer Trigger Source Delays
6E	ADR_SEQ_ID	Sequencer Board + CSC ID
70	ADR_SEQ_CLCT	Sequencer CLCT Configuration
72	ADR_SEQ_FIFO	Sequencer FIFO Configuration
74	ADR_SEQ_L1A	Sequencer L1A Configuration
76	ADR_SEQ_OFFSET	Sequencer Counter Offsets
78	ADR_SEQ_CLCT0	Sequencer Latched CLCT0
7A	ADR_SEQ_CLCT1	Sequencer Latched CLCT1
7C	ADR_SEQ_TRIG_SRC	Sequencer Trigger Source Read-back
7E	ADR_DMB_RAM_ADR	Sequencer RAM Address
80	ADR_DMB_RAM_WDATA	Sequencer RAM Write Data
82	ADR_DMB_RAM_WDCNT	Sequencer RAM Word Count
84	ADR_DMB_RAM_RDATA	Sequencer RAM Read Data
86	ADR_TMB_TRIG	TMB Trigger Configuration / MPC Accept
88	ADR_MPC0_FRAME0	MPC0 Frame 0 Data sent to MPC
8A	ADR_MPC0_FRAME1	MPC0 Frame 1 Data sent to MPC
8C	ADR_MPC1_FRAME0	MPC1 Frame 0 Data sent to MPC
8E	ADR_MPC1_FRAME1	MPC1 Frame 1 Data sent to MPC

90	ADR_MPC_INJ	MPC Injector Control
92	ADR_MPC_RAM_ADR	MPC Injector RAM address
94	ADR_MPC_RAM_WDATA	MPC Injector RAM Write Data
96	ADR_MPC_RAM_RDATA	MPC Injector RAM Read Data
98	ADR_SCP_CTRL	Scope control
9A	ADR_SCP_RDATA	Scope read data
9C	ADR_CCB_CMD	CCB TTC Command Generator
9E	ADR_BUF_STAT	Buffer Status
A0	ADR_SRLPGM	SRL LUT Program
A2	ADR_ALCT_FIFO1	ALCT Raw hits RAM Control
A4	ADR_ALCT_FIFO2	ALCT Raw hits RAM data
A6	ADR_ADJCFEB0	CFEB Adjacent hs Mask lsbs
A8	ADR_ADJCFEB1	CFEB Adjacent hs Mask msbs
AA	ADR_ADJCFEB2	CFEB Adjacent ds Mask
AC	ADR_SEQMOD	Sequencer Trigger Modifiers
AE	ADR_SEQSM	Sequencer Machine State
B0	ADR_SEQCLCTM	Sequencer CLCT msbs
B2	ADR_TMBTIM	TMB Timing for ALCT*CLCT coincidence
B4	ADR_LHC_CYCLE	LHC Cycle period, Maximum BXN+1
B6	ADR_RPC_CFG	RPC Configuration
B8	ADR_RPC_RDATA	RPC Sync Mode Read Data
BA	ADR_RPC_RAW_DELAY	RPC Raw Hits Delay
BC	ADR_RPC_INJ	RPC Injector Control
BE	ADR_RPC_INJ_ADR	RPC Injector RAM Addresses
C0	ADR_RPC_INJ_WDATA	RPC Injector Write Data
C2	ADR_RPC_INJ_RDATA	RPC Injector Read Data
C4	ADR_RPC_BXN_DIFF	RPC BXN Differences
C6	ADR_RPC0_HCM	RPC0 Hot Channel Mask
C8	ADR_RPC1_HCM	RPC1 Hot Channel Mask
CA	ADR_RPC2_HCM	RPC2 Hot Channel Mask
CC	ADR_RPC3_HCM	RPC3 Hot Channel Mask

Register Definitions

Adr 70000_{16} ADR_BOOT **Hardware Bootstrap Register**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R=tdo	R=ready	free	free	/fpga vme_en	/en_fpga reset_alct	hard reset TMB	hard reset ALCT	JTAG source vme/fpga	sel3	sel2	sel1	sel0	tck	tms	tdi

Bit	Dir	Signal	Default	Description
[0]	R/W	jtag_vme1 (tdi)	0	vme tdi
[1]	R/W	jtag_vme2 (tms)	0	vme tms
[2]	R/W	jtag_vme3 (tck)	0	vme tck
[3]	R/W	sel_vme0	0	00XX ALCT JTAG Chain
[4]	R/W	sel_vme1	0	01XX TMB Mezzanine FPGA + FPGA PROMs Chain
[5]	R/W	sel_vme2	0	10XX TMB User PROMs JTAG chain
[6]	R/W	sel_vme3	0	11XX TMB FPGA User JTAG chain
[7]	R/W	vme/usr_en	0	1=JTAG sourced by Bootstrap Register, 0= from FPGA
[8]	R/W	hard_reset_alct_vme	0	1=Hard reset to ALCT FPGA
[9]	R/W	hard_reset_tmb_vme	0	1=Hard reset to TMB FPGA
[10]	R/W	/en_fpga_reset_alct	0	0=Allow TMB FPGA to hard reset ALCT
[11]	R/W	/fpga_vme_en	0	0=Allow TMB FPGA to issue VME commands
[12]	R/W	unassigned	0	Available for future use
[13]	R/W	unassigned	0	Available for future use
[14]	R	vme_ready	x	1=FPGA vme logic indicates ready
[15]	R	jtag_vme0 (tdo)	0	vme tdo
[14]	W	unassigned	-	No connection on PCB
[15]	W	unassigned	-	No connection on PCB

Adr 00 ADR_IDREG0 ID Register 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	ga4	ga3	ga2	ga1	ga0	fvers3	fvers2	fvers1	fvers0	ftype3	ftype2	ftype1	ftype0

Bits	Dir	Typical	Description
[03:00]	R	C	Firmware type, C=Normal CLCT/TMB, D=Debug loopback
[07:04]	R	D	Firmware version code
[12:08]	R	15	Geographic address for this board
[15:13]	R	0	Unassigned

Adr 02 ADR_IDREG1 ID Register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
month msd3	month msd2	month msd1	month msd0	month lsd3	month lsd2	month lsd1	month lsd0	day msd3	day msd2	day msd1	day msd0	day lsd3	day lsd2	day lsd1	day lsd0

Bits	Dir	Typical	Description
[07:00]	R	14	DD Firmware Version Day (BCD)
[15:08]	R	04	MM Firmware Version Month (BCD)

Adr 04 ADR_IDREG2 ID Register 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
year digit3 3	year digit3 2	year digit3 1	year digit3 0	year digit2 3	year digit2 2	year digit2 1	year digit2 0	year digit1 3	year digit1 2	year digit1 1	year digit1 0	year digit0 3	year digit0 2	year digit0 1	year digit0 0

Bits	Dir	Typical	Description
[15:00]	R	2002	YYYY Firmware Version Year (BCD)

Adr 06 ADR_IDREG3 ID Register 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rev code 15	rev code 14	rev code 13	rev code 12	rev code 11	rev code 10	rev code 9	rev code 8	rev code 7	rev code 6	rev code 5	rev code 4	rev code 3	rev code 2	rev code 1	rev code 0

Bits	Dir	Typical	Description
[15:00]	R		Firmware Revcode (as stored in raw hits header)

Adr 08 ADR_VME_STATUS VME Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMB ready	local/ geo	iack	acfail	sysreset	sysfail	sysclk	ds1	as	lword	gap	ga4	ga3	ga2	ga1	ga0

Bits	Dir	Typical	Description
[04:00]	R		Crate slot Geographic Address
[05]	R		Crate slot Geographic Address Parity
[06]	R		VME signal lword
[07]	R		VME signal as
[08]	R		VME signal ds1
[09]	R		VME signal sysclk
[10]	R		VME signal sysfail
[11]	R		VME signal sysreset
[12]	R		VME signal acfail
[13]	R		VME signal iack
[14]	R		1=Address mode set to local, 0=Geographic
[15]	R		1=TMB reports ready to boot register

Adr 0A ADR_VME_ADR0 VME Address Read-Back

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
a15	a14	a13	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	lword

Bits	Dir	Typical	Description
[15:00]	R	a[15:0]	VME Address captured at last write cycle {a[15:1},lword}

Adr 0C ADR_VME_ADR1 VME Address Read-Back

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMB ready	local/ geo	iack	acfail	sysreset	sysfail	sysclk	ds1	as	lword	gap	ga4	ga3	ga2	ga1	ga0

Bits	Dir	Typical	Description
[07:00]	R	a[23:16]	VME Address captured at last write cycle
[13:08]	R	am[5:0]	VME Address modifier
[15:14]	R	0	Unassigned

Adr 0E ADR_LOOPBK Loop-Back Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	gtl_ oe	gtl_ loop	dmb_ oe	dmb_ loop	rpc_ oe	rpc_ loop	alct_ oe	alct_ scsi_ rear	alct_ loop	cfeb_ oe

Bits	Dir	Signal	Default	Description
[00]	R	cfeb_oe	1	1=CFEB output enable
[01]	R	alct_loop	0	0=No ALCT loop-back
[02]	R/W	alct_scsi_rear	1	1=ALCT source=SCSI, 0=RAT module
[03]	R	alct_oe	0	0=ALCT driver enable
[04]	R	rpc_loop	0	No RPC Loop-back
[05]	R	rpc_oe	0	RPC driver enable
[06]	R	dmb_loop	0	0=No DMB loop-back
[07]	R	dmb_oe	0	0=DMB driver enable
[08]	R	gtl_loop	0	0=No GTL loop-back
[09]	R	gtl_oe	0	0=Enable GTL outputs
[15:10]	R	--	0	Unassigned

Adr 10 ADR_USR_JTAG User JTAG Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
tdo usr	0	0	0	0	0	0	0		sel3 usr	sel2 usr	sel1 usr	sel0 usr	tck usr	tms usr	tdi usr

Bits	Dir	Signal	Description
[00]	R/W	tdi_usr	User JTAG Chain TDI (output from FPGA)
[01]	R/W	tms_usr	User JTAG Chain TMS
[02]	R/W	tck_usr	User JTAG Chain TCK
[06:03]	R/W	sel_usr[3:0]	User JTAG Chain Select, 0=ALCT,1=Mez,2=UserPROMs,3=UserChain
[14:07]	R/W	-	Unassigned
[15]	R	tdo_usr	User JTAG Chain TDO (input to FPGA)

Adr 12 ADR_PROM User PROMs Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	prom_ src	prom1 ce	prom1 oe	prom1 clk	prom0 ce	prom0 oe	prom0 clk	prom_ led7	prom_ led6	prom_ led5	prom_ led4	prom_ led3	prom_ led2	prom_ led1	prom_ led0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	prom_led[7:0]	CD	PROM data bus shared with On-Board LEDs
[08]	R/W	prom0_clk	0	PROM 0 clock
[09]	R/W	prom0_oe	0	PROM 0 output enable
[10]	R/W	prom0_ce	1	PROM 0 /chip_enable
[11]	R/W	prom1_clk	0	PROM 1 clock
[12]	R/W	prom1_oe	0	PROM 1 output enable
[13]	R/W	prom1_ce	1	PROM 1 /chip_enable
[14]	R/W	prom_src	0	Data bus 0=on-board LEDs, 1=enabled PROM
[15]	R/W	--	0	Unassigned

Adr 14 ADR_DDDSM 3D3444 State Machine Control + DCM Lock Status

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rpc lock	dcc lock	mpc lock	alctd lock	alct lock	tmb1 lock	tmb0d lock	tmb0 lock	ddd verify	dddsm busy	auto start	serial from	serial to ddd	adr latch	ddd clock	ddd start

Bits	Dir	Signal	Default	Description
[00]	R/W	ddd_start_vme	0	Start DDD State Machine
[01]	R/W	ddd_clock	0	DDD manual-mode clock
[02]	R/W	ddd_adr_latch	0	DDD manual-mode address latch
[03]	R/W	ddd_serial_in	0	Serial data to DDD chain
[04]	R/W	ddd_serial_out	0	Serial data from DDD chain
[05]	R/W	ddd_auto_start	1	DDD State Machine autostart state
[06]	R	ddd_busy	0	DDD State Machine busy
[07]	R	ddd_verify	1	DDD data read back verified OK
[08]	R	lock_tmb_clock0	1	TMB clock 0 DCM locked
[09]	R	lock_tmb_clock0d	1	TMB clock 0d DCM locked
[10]	R	lock_tmb_clock1	1	TMB clock 1 DCM locked
[11]	R	lock_alct_clock	1	ALCT rxclock DCM locked
[12]	R	lock_alct_clockd	1	ALCT rxclockd DCM locked
[13]	R	lock_mpc_clock	1	MPC clock DCM locked
[14]	R	lock_dcc_clock	1	DCC clock DCM locked
[15]	R	lock_rpc_clock	1	RPC clock DCM locked

Adr 16 ADR_DDD0 3D3444 Chip 0 Delays, 1 step = 2ns

Bits	Dir	Signal	Default	Description
[03:00]	R/W	delay_ch0[3:0]	8	ALCT tx clock, 8 steps = 16ns delay
[07:04]	R/W	delay_ch1[3:0]	1	ALCT rx clock
[11:08]	R/W	delay_ch2[3:0]	2	DMB tx clock
[15:12]	R/W	delay_ch3[3:0]	0	RPC tx clock

Adr 18 ADR_DDD1 3D3444 Chip 1 Delays, 1 step = 2ns

Bits	Dir	Signal	Default	Description
[03:00]	R/W	delay_ch4[3:0]	0	TMB1 Clock
[07:04]	R/W	delay_ch5[3:0]	0	MPC Clock
[11:08]	R/W	delay_ch6[3:0]	0	DCC Clock (CFEB duty cycle correction)
[15:12]	R/W	delay_ch7[3:0]	7	CFEB 0 clock

Adr 1A ADR_DDD2 3D3444 Chip 2 Delays, 1 step = 2ns

Bits	Dir	Signal	Default	Description
[03:00]	R/W	delay_ch8[3:0]	7	CFEB 1 clock
[07:04]	R/W	delay_ch9[3:0]	7	CFEB 2 clock
[11:08]	R/W	delay_ch10[3:0]	7	CFEB 3 clock
[15:12]	R/W	delay_ch11[3:0]	7	CFEB 4 clock

Adr 1C ADR_DDDOE 3D3444 Chip Output Enables

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	cfeb 4	cfeb 3	cfeb 2	cfeb 1	cfeb 0	dcc	mpc	tmb1	rpc tx	dmb tx	alct rx	alct tx

[11:00]	R/W	ddd_oe[11:0]	0FFF	Bit(n)=1=Enable DDD output channel n
[15:12]	R/W	Unassigned	0	Unassigned

Adr 1E ADR_RATCTRL RAT Module Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	rpc dsn en	rpc free	rpc lptm	rpc posneg	rpc sync

Bits	Dir	Signal	Default	Description
[0]	R/W	rpc_sync	0	1=RPC 80MHz sync pattern mode
[1]	R/W	rpc_posneg	0	1=shift RPC data ½ cycle in RAT FPGA + dsn
[2]	R/W	rpc_lptmb	0	Not used (for matching rpc_tx array)
[3]	R/W	rpc_free_tx[0]	0	Unassigned
[4]	R/W	rat_dsn_en	0	1=Enable RAT dsn readout
[15:5]	R/W	--	0	Unassigned

Adr 20 ADR_STEP Clock Single-Step + Hard Resets

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	/tmb hard	/alct hard	alct clken	cfeb4 clken	cfeb3 clken	cfeb2 clken	cfeb1 clken	cfeb0 clken	step run	step cfeb	step rpc	step dmb	step alct

Bits	Dir	Signal	Default	Description
[00]	R/W	step_alct	0	Step ALCT clock
[01]	R/W	step_dmb	0	Step DMB clock
[02]	R/W	step_rpc	0	Step RPC clock
[03]	R/W	step_cfeb	0	Step CFEB clock
[04]	R/W	step_run	0	0=run mode, 1=step clocks
[05]	R/W	cfeb_clock_en0	1	1=enable CFEB0 clock
[06]	R/W	cfeb_clock_en1	1	1=enable CFEB0 clock
[07]	R/W	cfeb_clock_en2	1	1=enable CFEB0 clock
[08]	R/W	cfeb_clock_en3	1	1=enable CFEB0 clock
[09]	R/W	cfeb_clock_en4	1	1=enable CFEB0 clock
[10]	R/W	alct_clock_en	1	1=enable ALCT clock
[11]	R/W	/alct_hard_reset_en	1	1=disable ALCT hard reset
[12]	R/W	/tmb_hard_reset_en	1	1=disable TMB hard reset
[15:13]	R/W	--	0	Unassigned

Adr 22 ADR_LED Front Panel + On-Board LED Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
led bd7	led bd6	led bd5	led bd4	led bd3	led bd2	led bd1	led bd0	VME	NL1A	NMAT	INVP	L1A	CLCT	ALCT	LCT

Bits	Dir	Signal	Color	Description
[00]	R/W	led_fp_lct	Blue	LCT TMB matched ALCT+CLCT
[01]	R/W	led_fp_lct	Green	ALCT found a muon
[02]	R/W	led_fp_clct	Green	CLCT found a muon
[03]	R/W	led_fp_l1a	Green	L1A level 1 accept
[04]	R/W	led_fp_invp	Amber	INVP invalid pattern after CSC drift
[05]	R/W	led_fp_nmat	Amber	NMAT no match after ALCT or CLCT triggered
[06]	R/W	led_fp_nl1a	Red	NL1A no L1A after trigger
[07]	R/W	led_fp_vme	Green	VME power-up = on, off=vme access flash
[08]	R/W	led_bd0	Blue	Buffer busy[0]
[09]	R/W	led_bd1	Green	Buffer busy[1]
[10]	R/W	led_bd2	Green	Buffer busy[2]
[11]	R/W	led_bd3	Green	Buffer busy[3]
[12]	R/W	led_bd4	Green	Buffer busy[4]
[13]	R/W	led_bd5	Green	Buffer busy[5]
[14]	R/W	led_bd6	Green	Buffer busy[6]
[15]	R/W	led_bd7	Red	Buffer busy[7]

Adr 24 ADR_ADC ADC + Power Comparator Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	smb data	smb clk	ADC /cs	ADC din	ADC sclock	ADC dout	/tcrit	V1.5	V1.8	V3.3	V5.0

Bits	Dir	Signal	Typical	Description
[00]	R	vstat_5p0v	1	1 = 5.0V power supply OK
[01]	R	vstat_3p3v	1	1 = 3.3V power supply OK
[02]	R	vstat_1p8v	1	1 = 1.8V power supply OK
[03]	R	vstat_1p5v	1	1 = 1.5V power supply OK
[04]	R	/t_crit	1	1 = FPGA and Board Temperature OK
[05]	R	adc_dout	0	Voltage monitor ADC serial data receive
[06]	R/W	adc_sclock	0	Voltage monitor ADC serial clock
[07]	R/W	adc_din	0	Voltage monitor ADC serial data transmit
[08]	R/W	/adc_cs	1	Voltage monitor ADC chip select
[09]	R/W	smb_clk	0	Temperature monitor ADC serial clock
[10]	R/W	smb_data	1	Temperature monitor ADC serial data, open drain
[15:11]	R/W	--	0	Unassigned

Adr 26 ADR_DSN Digital Serial Numbers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RAT DSN Data	RAT DSN Busy	RAT DSN Init	RAT DSN Write	RAT DSN Start	Mez DSN Data	Mez DSN Busy	Mez DSN Init	Mez DSN Write	Mez DSN Start	TMB DSN Data	TMB DSN Busy	TMB DSN Init	TMB DSN Write	TMB DSN Start

Bits	Dir	Signal	Default	Description
[00]	R/W	tmb_sn_start	0	TMB Digital serial SM start
[01]	R/W	tmb_sn_write	0	TMB Digital serial write pulse
[02]	R/W	tmb_sn_init	0	TMB Digital serial Init pulse
[03]	R	tmb_sn_busy	-	TMB State DSN State Machine busy
[04]	R	tmb_sn_data	-	TMB State DSN read data
[05]	R/W	mez_sn_start	0	Mez Digital Serial State Machine start
[06]	R/W	mez_sn_write	0	Mez Digital Serial Write pulse
[07]	R/W	mez_sn_init	0	Mez Digital Serial Init pulse
[08]	R	mez_sn_busy	-	Mez State DSN State Machine busy
[09]	R	mez_sn_data	-	Mez State DSN read data
[10]	R/W	rat_sn_start	0	RAT Digital Serial State Machine start
[11]	R/W	rat_sn_write	0	RAT Digital Serial Write pulse
[12]	R/W	rat_sn_init	0	RAT Digital Serial Init pulse
[13]	R	rat_sn_busy	-	RAT State DSN State Machine busy
[14]	R	rat_sn_data	-	RAT State DSN read data
[15]	R/W	-	0	Unassigned

Adr 28 ADR_MOD_CFG TMB Module Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
mez done	ddd auto	power up	0	led flash rate 1	led flash rate 0	cfeb4 exists	cfeb3 exists	cfeb2 exists	cfeb1 exists	cfeb0 exists	bdled cylon	bdled vme	fpled flash	fpled cylon	fpled vme

Bits	Dir	Signal	Default	Description
[00]	R/W	led_fp_src_vme	0	1=Front Panel LEDs sourced from VME register
[01]	R/W	led_fp_cylon	0	1=FP LED Cylon mode, cool
[02]	R/W	led_flash_on_stop	1	1=Flash Front Panel LEDs on TTT stop_trigger
[03]	R/W	led_bd_src_vme	0	1=On-Board LEDs sourced from VME register
[04]	R/W	led_bd_cylon	0	1=BD LED Cylon mode, cool
[9:5]	R	cfeb_exists	1F	CFEB(n) instantiated in this firmware version
[11:10]	RW	led_flash_rate[1:0]	0	LED flash rate in Flash-on-stop mode
[12]	RW			Unassigned
[13]	R	power_up		Power-up FF
[14]	R	ddd_autostart		1=3D3444 auto-start enabled
[15]	R	mez_done		1=Mezzanine FPGA loaded from PROM

Adr 2A ADR_CCB_CFG CCB Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
adb pulse async	adb pulse sync	alct hard reset	tmb hard reset	tmb resout 2	tmb resout 1	tmb resout 0	tmb res1	tmb res0	l1a vme	clct status en	alct status en	/ccb status oe	int l1aen	disabl tx	ignore rx

Bits	Dir	Signal	Default	Description
[00]	R/W	ccb_ignore_rx	0	1=Ignore Received CCB backplane inputs
[01]	R/W	ccb_disable_tx	0	1=Disble tranmistted CCB backplane outputs
[02]	R/W	ccb_int_l1a_en	0	1=Enable internal L1A emulator
[03]	R/W	/ccb_status_oe_vme	1	1=Enable ALCT+CLCT status to CCB front panel
[04]	R/W	alct_status_en	1	1=Enable ALCT status GTL outputs
[05]	R/W	clct_status_en	1	1=Enable CLCT status GTL outputs
[06]	R/W	l1accept_vme	0	1=fire ccb_l1accept oneshot
[08:07]	R	tmb_reserved[1:0]		Future use
[11:09]	R	tmb_reserved_out[2:0]		Future use
[12]	R	tmb_hard_reset		Reload TMB_FPGA
[13]	R	alct_hard_reset		Reload ALCT FPGA
[14]	R	alct_adb_pulse_sync		ALCT synchronous test pulse
[15]	R	alct_adb_pulse_async		ALCT asynchronous test pulse

Adr 2C ADR_CCB_TRIG CCB Trigger Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
l1a delay vme7	l1a delay vme6	l1a delay vme5	l1a delay vme4	l1a delay vme3	l1a delay vme2	l1a delay vme1	l1a delay vme0	0	ccb exttrig bypas	ext trig both	clct ext trg vme	alct ext trg vme	seq trig l1aen	clct ext trg l1aen	alct ext trg l1aen

Bits	Dir	Signal	Default	Description
[00]	R/W	alct_ext_trig_l1aen	0	1=Request ccb l1a on alct ext_trig
[01]	R/W	clct_ext_trig_l1aen	0	1=Request ccb l1a on clct ext_trig
[02]	R/W	seq_trig_l1aen	1	1=Request ccb l1a on sequencer trigger
[03]	R/W	alct_ext_trig_vme	0	1=Fire alct_ext_trig oneshot
[04]	R/W	clct_ext_trig_vme	0	1=Fire clct_ext_trig oneshot
[05]	R/W	ext_trig_both	0	1=clct_ext_trig fires alct + alct fires clct_trig, DC
[06]	R/W	ccb_allow_extbypass	0	1=Allow clct_exttrig_ccb when ccb_ignore_rx=1
[07]	R/W	--	0	Unassigned
[15:08]	R/W	l1a_delay_vme	75_{16}	Internal L1A delay (not same as sequencer L1A)

Adr 2E ADR_CCB_STAT CCB Status

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ccb bx0	ccb bcntrs	ccb res4	ccb res3	ccb res2	ccb res1	ccb res0	ccb clock en	ccb cmd7	ccb cmd6	ccb cmd5	ccb cmd4	ccb cmd3	ccb cmd2	ccb cmd1	ccb cmd0

Bits	Dir	Signal	Default	Description
[07:00]	R	ccb_cmd[7:0]		CCB Command word from TTC
[08]	R	ccb_clock40_enable	1	1=TMB 40MHz clock from CCB enabled
[13:09]	R	ccb_reserved[4:0]		Future use
[14]	R	ccb_bcntres		Bunch counter reset from CCB (backplane)
[15]	R	ccb_bx0		Bunch crossing 0 from CCB (backplane)

Adr 30 ADR_ALCT_CFG ALCT Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	alct res in4	alct res in3	alct res in2	alct res in1	alct res in0	alct seq cmd2	alct seq cmd1	alct seq cmd0	assert alct ext inj	assert alct ext trg	alct ext inj en	alct ext trg en

Bits	Dir	Signal	Default	Description
[00]	R/W	cfg_alct_ext_trig_en	1	1=Enable alct_ext_trig_ from CCB
[01]	R/W	cfg_alct_ext_inject_en	0	1=Enable alct_ext_inject from CCB
[02]	R/W	cfg_alct_ext_trig	0	1=Assert alct_ext_trig
[03]	R/W	cfg_alct_ext_inject	0	1=Assert alct_ext_inject
[06:04]	R/W	alct_seq_cmd[2:0]	0	ALCT Sequencer command
[11:07]	R/W	alct_reserved_in[4:0]	0	ALCT Reserved for future use
[15:12]	R/W	--	0	Unassigned

Adr 32 ADR_ALCT_INJ ALCT Injector Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	inject delay 4	inject delay 3	inject delay 2	inject delay 1	inject delay 0	link inject w clct	start inject	clear alct

Bits	Dir	Signal	Default	Description
[00]	R/W	alct_clear	0	1=Blank ALCT received data
[01]	R/W	alct_inject_mux	0	1=Start ALCT injector State Machine
[02]	R/W	alct_sync_clct	0	1=Link ALCT injector with CLCT inject command
[07:03]	R/W	alct_inj_delay[7:0]	8_{16}	Injector delay
[15:08]	R/W	--	0	Unassigned

Adr 34 ADR_ALCT0_INJ ALCT0 1st Muon To Inject

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1st bxn 1	1st bxn 0	1st key 6	1st key 5	1st key 4	1st key 3	1st key 2	1st key 1	1st key 0	1st amu	1st qualty 1	1st qualty 0	1st vpf

Bits	Dir	Signal	Default	Description
[00]	R/W	alct_first_valid	1	Valid pattern flag
[02:01]	R/W	alct_first_quality[1:0]	3	Pattern quality
[03]	R/W	alct_first_amu	0	Accelerator muon flag
[10:04]	R/W	alct_first_key[6:0]	7	Injected ALCT0 key wire-group
[12:11]	R/W	alct_first_bxn[1:0]	1	Injected ALCT0 bunch crossing number
[15:13]	R/W	--	0	Unassigned

Adr 36 ADR_ALCT1_INJ ALCT1 2nd Muon To Inject

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	2nd bxn 1	2nd bxn 0	2nd key 6	2nd key 5	2nd key 4	2nd key 3	2nd key 2	2nd key 1	2nd key 0	2nd amu	2nd qualty 1	2nd qualty 0	2nd vpf

Bits	Dir	Signal	Default	Description
[00]	R/W	alct_second_valid	1	Valid pattern flag
[02:01]	R/W	alct_second_quality[1:0]	2	Pattern quality
[03]	R/W	alct_second_amu	0	Accelerator muon flag
[10:04]	R/W	alct_second_key[6:0]	61_{10}	Injected ALCT1 key wire-group
[12:11]	R/W	alct_second_bxn[1:0]	1	Injected ALCT1 bunch crossing number
[15:13]	R/W	--	0	Unassigned

Adr 38 ADR_ALCT_STAT ALCT Sequencer Control/Status

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	res out 3	res out 2	res out 1	res out 0	seu stat 1	seu stat 0	seq stat 1	seq stat 0	alct cfg done

Bits	Dir	Signal	Typical	Description
[00]	R	alct_cfg_done	1	ALCT FPGA Configuration done
[02:01]	R	seq_status[1:0]	0	ALCT Sequencer status
[04:03]	R	seu_status[1:0]	0	ALCT Single-event-upset status
[08:05]	R	reserved_out[3:0]	0	Future use
[15:09]	R	--	0	Unassigned

Adr 3A ADR_ALCT0_RCD ALCT 1st Muon Received by TMB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1st bxn 1	1st bxn 0	1st key 6	1st key 5	1st key 4	1st key 3	1st key 2	1st key 1	1st key 0	1st amu	1st qualty 1	1st qualty 0	1st vpf

Bits	Dir	Signal	Typical	Description
[00]	R	alct_first_valid	1	Valid pattern flag
[02:01]	R	alct_first_quality[1:0]	0-3	Pattern quality
[03]	R	alct_first_amu	0	Accelerator muon flag
[10:04]	R	alct_first_key[6:0]	0-111	Injected ALCT0 key wire-group
[12:11]	R	alct_first_bxn[1:0]	0-3	Injected ALCT0 bunch crossing number
[15:13]	R	--	0	Unassigned

Adr 3C ADR_ALCT0_RCD ALCT 2nd Muon Received by TMB

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	2nd bxn 1	2nd bxn 0	2nd key 6	2nd key 5	2nd key 4	2nd key 3	2nd key 2	2nd key 1	2nd key 0	2nd amu	2nd qualty 1	2nd qualty 0	2nd vpf

Bits	Dir	Signal	Typical	Description
[00]	R	alct_second_valid	1	Valid pattern flag
[02:01]	R	alct_second_quality[1:0]	0-3	Pattern quality
[03]	R	alct_second_amu	0	Accelerator muon flag
[10:04]	R	alct_second_key[6:0]	0-111	Injected ALCT1 key wire-group
[12:11]	R	alct_second_bxn[1:0]	0-3	Injected ALCT1 bunch crossing number
[15:13]	R	--	0	Unassigned

Adr 3E ADR_ALCT_FIFO ALCT FIFO RAM Status

(Split with Adr A2 ADR_ALCT_FIFO1 and A4 ADR_ALCT_FIFO2)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	alct data17	alct data16	alct wdcnt 10	alct wdcnt 9	alct wdcnt 8	alct wdcnt 7	alct wdcnt 6	alct wdcnt 5	alct wdcnt 4	alct wdcnt 3	alct wdcnt 2	alct wdcnt 1	alct wdcnt 0	alct RAM done	alct RAM busy

Bits	Dir	Signal		Description
[00]	R	alct_raw_busy		ALCT raw hits FIFO busy writing ALCT data
[01]	R	alct_raw_done		ALCT raw hits ready for VME readout
[12:02]	R	alct_raw_wdcnt[10:0]		ALCT raw hits word count stored in RAM
[14:13]	R	alct_raw_rdata[17:16]		ALCT raw hits data MSBs
[15]	R	--	0	Unassigned

Adr 40 ADR_DMB_MON DMB Monitored Signals

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	2nd bxn 1	2nd bxn 0	2nd key 6	2nd key 5	2nd key 4	2nd key 3	2nd key 2	2nd key 1	2nd key 0	2nd amu	2nd qualty 1	2nd qualty 0	2nd vpf

Bits	Dir	Signal	Typical	Description
[02:00]	R	dmb_cfeb_calibrate[2:0]	0	DMB calibration
[03]	R	dmb_l1a_release	0	DMB test
[08:04]	R	dmb_reserved_out[4:0]	0	DMB future use
[11:09]	R	dmb_reserved_in[2:0]	0	DMB future use
[15:12]	R	dmb_rx_ff[3:0]	0	DMB received

Adr 42 ADR_CFEB_INJ CFEB Injector Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
inj start	inj mask 4	inj mask 3	inj mask 2	inj mask 1	inj mask 0	inj febsel 4	inj febsel 3	inj febsel 2	inj febsel 1	inj febsel 0	mask all cfeb4	mask all cfeb3	mask all cfeb2	mask all cfeb1	mask all cfeb0

Bits	Dir	Signal	Default	Description
[04:00]	R/W	mask_all[4:0]	11111_2	1=Enable, 0=Turn off all CFEBn inputs
[09:05]	R/W	inj_febsel[4:0]	0	1=Select CFEBn for RAM read/write
[14:10]	R/W	injector_mask[4:0]	11111_2	Enable CFEBn for injector trigger
[15]	R/W	inj_trig_vme	0	Start pattern injector

Adr 44 ADR_CFEB_INJ_ADR CFEB Injector RAM Address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	inj adr 7	inj adr 6	inj adr 5	inj adr 4	inj adr 3	inj adr 2	inj adr 1	inj adr 0	inj ren 2	inj ren 1	inj ren 0	inj wen 2	inj wen 1	inj wen 0

Bits	Dir	Signal	Default	Description
[02:00]	R/W	inj_wen[2:0]	0	1=Write enable injector RAMn (Ly01,23,45)
[05:03]	R/W	inj_ren[2:0]	0	1=Read enable Injector RAMn
[13:06]	R/W	inj_rwadr[7:0]	0	Injector RAM read/write address
[15:14]	R/W	--	0	Unassigned

Adr 46 ADR_CFEB_INJ_WDATA CFEB Injector Write Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
inj wdata 15	inj wdata 14	inj wdata 13	inj wdata 12	inj wdata 11	inj wdata 10	inj wdata 9	inj wdata 8	inj wdata 7	inj wdata 6	inj wdata 5	inj wdata 4	inj wdata 3	inj wdata 2	inj wdata 1	inj wdata 0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	inj_wdata[7:0]	0	Triad bit for addressed Tbin Ly0 (or 2,4)
[15:08]	R/W	inj_wdata[15:8]	0	Triad bit for addressed Tbin Ly1 (or 3,5)

Adr 48 ADR_CFEB_INJ_RDATA CFEB Injector Read Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
inj rdata 15	inj rdata 14	inj rdata 13	inj rdata 12	inj rdata 11	inj rdata 10	inj rdata 9	inj rdata 8	inj rdata 7	inj rdata 6	inj rdata 5	inj rdata 4	inj rdata 3	inj rdata 2	inj rdata 1	inj rdata 0

Bits	Dir	Signal	Default	Description
[07:00]	R	inj_rdata[7:0]	0	Triad bit for addressed Tbin Ly0 (or 2,4)
[15:08]	R	inj_rdata[15:8]	0	Triad bit for addressed Tbin Ly1 (or 3,5)

Adr 4A ADR_HCM001 CFEB0 Ly0,Ly1 Hot Channel Mask

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ly1 distrip 7	ly1 distrip 6	ly1 distrip 5	ly1 distrip 4	ly1 distrip 3	ly1 distrip 2	ly1 distrip 1	ly1 distrip 0	ly0 distrip 7	ly0 distrip 6	ly0 distrip 5	ly0 distrip 4	ly0 distrip 3	ly0 distrip 2	ly0 distrip 1	ly0 distrip 0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	cfeb0_ly0_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 0
[15:08]	R/W	cfeb0_ly1_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 1

Adr 4C ADR_HCM023 CFEB0 Ly2,Ly3 Hot Channel Mask

[07:00]	R/W	cfeb0_ly2_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 2
[15:08]	R/W	cfeb0_ly3_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 3

Adr 4E ADR_HCM045 CFEB0 Ly4,Ly5 Hot Channel Mask

[07:00]	R/W	cfeb0_ly4_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 4
[15:08]	R/W	cfeb0_ly5_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 5

Adr 50 ADR_HCM101 CFEB1 Ly0,Ly1 Hot Channel Mask

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ly1 distrip 7	ly1 distrip 6	ly1 distrip 5	ly1 distrip 4	ly1 distrip 3	ly1 distrip 2	ly1 distrip 1	ly1 distrip 0	ly0 distrip 7	ly0 distrip 6	ly0 distrip 5	ly0 distrip 4	ly0 distrip 3	ly0 distrip 2	ly0 distrip 1	ly0 distrip 0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	cfeb1_ly0_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 0
[15:08]	R/W	cfeb1_ly1_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 1

Adr 52 ADR_HCM123 CFEB1 Ly2,Ly3 Hot Channel Mask

[07:00]	R/W	cfeb1_ly2_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 2
[15:08]	R/W	cfeb1_ly3_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 3

Adr 54 ADR_HCM145 CFEB1 Ly4,Ly5 Hot Channel Mask

[07:00]	R/W	cfeb0_ly4_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 4
[15:08]	R/W	cfeb0_ly5_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 5

Adr 56 ADR_HCM201 CFEB2 Ly0,Ly1 Hot Channel Mask

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ly1 distrip 7	ly1 distrip 6	ly1 distrip 5	ly1 distrip 4	ly1 distrip 3	ly1 distrip 2	ly1 distrip 1	ly1 distrip 0	ly0 distrip 7	ly0 distrip 6	ly0 distrip 5	ly0 distrip 4	ly0 distrip 3	ly0 distrip 2	ly0 distrip 1	ly0 distrip 0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	cfeb2_ly0_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 0
[15:08]	R/W	cfeb2_ly1_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 1

Adr 58 ADR_HCM223 CFEB2 Ly2,Ly3 Hot Channel Mask

[07:00]	R/W	cfeb2_ly2_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 2
[15:08]	R/W	cfeb2_ly3_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 3

Adr 5A ADR_HCM245 CFEB2 Ly4,Ly5 Hot Channel Mask

[07:00]	R/W	cfeb2_ly4_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 4
[15:08]	R/W	cfeb2_ly5_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 5

Adr 5C ADR_HCM301 CFEB3 Ly0,Ly1 Hot Channel Mask

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ly1 distrip 7	ly1 distrip 6	ly1 distrip 5	ly1 distrip 4	ly1 distrip 3	ly1 distrip 2	ly1 distrip 1	ly1 distrip 0	ly0 distrip 7	ly0 distrip 6	ly0 distrip 5	ly0 distrip 4	ly0 distrip 3	ly0 distrip 2	ly0 distrip 1	ly0 distrip 0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	cfeb3_ly0_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 0
[15:08]	R/W	cfeb3_ly1_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 1

Adr 5E ADR_HCM323 CFEB3 Ly2,Ly3 Hot Channel Mask

[07:00]	R/W	cfeb3_ly2_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 2
[15:08]	R/W	cfeb3_ly3_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 3

Adr 60 ADR_HCM345 CFEB3 Ly4,Ly5 Hot Channel Mask

[07:00]	R/W	cfeb3_ly4_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 4
[15:08]	R/W	cfeb3_ly5_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 5

Adr 62 ADR_HCM401 CFEB4 Ly0,Ly1 Hot Channel Mask

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ly1 distrip 7	ly1 distrip 6	ly1 distrip 5	ly1 distrip 4	ly1 distrip 3	ly1 distrip 2	ly1 distrip 1	ly1 distrip 0	ly0 distrip 7	ly0 distrip 6	ly0 distrip 5	ly0 distrip 4	ly0 distrip 3	ly0 distrip 2	ly0 distrip 1	ly0 distrip 0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	cfeb4_ly0_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 0
[15:08]	R/W	cfeb4_ly1_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 1

Adr 64 ADR_HCM423 CFEB4 Ly2,Ly3 Hot Channel Mask

[07:00]	R/W	cfeb4_ly2_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 2
[15:08]	R/W	cfeb4_ly3_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 3

Adr 66 ADR_HCM445 CFEB4 Ly4,Ly5 Hot Channel Mask

[07:00]	R/W	cfeb4_ly4_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 4
[15:08]	R/W	cfeb4_ly5_hcm[7:0]	11111111_2	1=Enable DiStrip[7:0] Layer 5

Adr 68 ADR_SEQ_TRIG_EN Sequencer Trigger Source Enables

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	all cfebs active	ext trig inject	vme trig	alct ext trig en	clct ext trig en	adb ext trig en	adb ext trig en	alct*clct pat trig en	alct pat trig en	clct pat trig en

Bits	Dir	Signal	Default	Description
[00]	R/W	clct_pat_trig_en	1	1=Allow CLCT pattern triggers (CLCT Active FEB)
[01]	R/W	alct_pat_trig_en	0	1=Allow ALCT pattern triggers (ALCT Active FEB)
[02]	R/W	match_pat_trig_en	0	1=ALCT*CLCT pattern triggers
[03]	R/W	adb_ext_trig_en	0	1=Allow ADB external triggers from CCB
[04]	R/W	dmb_ext_trig_en	0	1=Allow DMB external triggers
[05]	R/W	clct_ext_trig_en	0	1=Allow CLCT external triggers (scintillator) from CCB
[06]	R/W	alct_ext_trig_en	0	1=Allow ALCT external triggers from CCB
[07]	R/W	vme_ext_trig	0	1=Initiate Sequencer trigger (write 0 to recover)
[08]	R/W	ext_trig_inject	0	1=Change clct_ext_trig to fire pattern injector
[09]	R/W	all_cfebs_active	0	1=Make all CFEBs active when triggered
[15:10]	R/W	--	0	Unassigned

Adr 6A ADR_SEQ_TRIG_DLY0 Sequencer Trigger Source Delays

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
adb delay 3	adb delay 2	adb delay 1	adb delay 0	alct aff delay 3	alct aff delay 2	alct aff delay 1	alct aff delay 0	alct pretrig delay	alct pretrig delay 2	alct pretrig delay 1	alct pretrig delay 0	alct width 3	alct width 2	alct width 1	alct width 0

Bits	Dir	Signal	Default	Description
[03:00]	R/W	alct_trig_width[3:0]	3	ALCTCLCT Pre-trigger window width
[07:04]	R/W	alct_pre_trig_dly	0 (2)	ALCT Pre-trigger delay for ALCT*CLCT
[11:08]	R/W	alct_pat_trig_dly[3:0]	0	Delay alct_pat_trig (active feb flag from ALCT)
[15:12]	R/W	adb_ext_trig_dly[3:0]	1	Delay adb_ext_trig from CCB

Adr 6C ADR_SEQ_TRIG_DLY1 Sequencer Trigger Source Delays

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	alct ext delay 3	alct ext delay 2	alct ext delay 1	alct ext delay 0	clct ext delay 3	clct ext delay 2	clct ext delay 1	clct ext delay 0	dmb ext delay 3	dmb ext delay 2	dmb ext delay 1	dmb ext delay 0

Bits	Dir	Signal	Default	Description
[03:00]	R/W	dmb_ext_trig_dly[3:0]	1	Delay dmb_ext_trig from DMB
[07:04]	R/W	clct_ext_trig_dly[3:0]	7	Delay clct_ext_trig (scintillator) from CCB
[11:08]	R/W	alct_ext_trig_dly[3:0]	7	Delay alct_ext_trig from CCB
[15:12]	R/W	--	0	Unassigned

Adr 6E ADR_SEQ_ID Sequencer Board + CSC Ids

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	run id 3	run id 2	run id 1	run id 0	csd id 3	csd id 2	csd id 1	csd id 0	board id 4	board id 3	board id 2	board id 1	board id 0

Bits	Dir	Signal	Default	Description
[04:00]	R/W	board_id[4:0]	21	Board ID = VME Slot Geographic Adr
[08:05]	R/W	csc_id[3:0]	5	CSC Chamber ID number
[12:09]	R/W	run_id[3:0]	0	Run ID number
[15:13]	R/W	--	0	Unassigned

Adr 70 ADR_SEQ_CLCT Sequencer CLCT Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
pretrig halt	drft delay 0	drft delay 0	nph patrn 2	nph patrn 1	nph patrn 0	ds thresh 2	ds thresh 1	ds thresh 0	hs thresh 2	hs thresh 1	hs thresh 0	triad persist 3	triad persist 2	triad persist 1	triad persist 0

Bits	Dir	Signal	Default	Description
[03:00]	R/W	triad_persist	5	Triad One-Shot Persistence (5=150ns)
[06:04]	R/W	hs_thresh[2:0]	4	½-Strip Pre-trigger threshold
[09:07]	R/W	ds_thresh[2:0]	4	Di-Strip Pre-trigger threshold
[12:10]	R/W	nph_pattern[2:0]	4	Minimum pattern hits for a valid pattern
[14:13]	R/W	drift_delay[1:0]	2	CSC Drift delay, number 25ns clock periods
[15]	R/W	pretrig_halt	0	Pretrigger and halt until unhalt arrives

Adr 72 ADR_SEQ_FIFO Sequencer FIFO Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	fifo pretrig 4	fifo pretrig 3	fifo pretrig 2	fifo pretrig 1	fifo pretrig 0	fifo tbins 4	fifo tbins 3	fifo tbins 2	fifo tbins 1	fifo tbins 0	fifo mode 2	fifo mode 1	fifo mode 0

Bits	Dir	Signal	Default	Description
[02:00]	R/W	fifo_mode[2:0]	1	FIFO Mode: 0=no CFEB raw hits full header 1=all CFEB raw hits full header 2=local CFEB raw hits full header 3=no CFEB raw hits short header 4=no CFEB raw hits no header
[07:03]	R/W	fifo_tbins[4:0]	7	Number FIFO time bins to read out
[12:08]	R/W	fifo_pretrig[4:0]	2	Number FIFO time bins before pretrigger
[15:13]	R/W	--	0	Unassigned

Adr 74 ADR_SEQ_L1A Sequencer L1A Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	l1a intern	l1a windo 3	l1a windo 2	l1a windo 1	l1a windo 0	l1a delay 7	l1a delay 6	l1a delay 5	l1a delay 4	l1a delay 3	l1a delay 2	l1a delay 1	l1a delay 0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	l1a_delay[7:0]	128_{10}	Level1 Accept delay from pretrig status output
[11:08]	R/W	l1a_window[3:0]	3	Level1 Accept window width after delay
[12]	R/W	l1a_internal	0	Generate internal Level 1, overrides external
[15:13]	R/W	--	0	Unassigned

Adr 76 ADR_SEQ_OFFSET Sequencer Counter Offsets

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
bxn offset 11	bxn offset 10	bxn offset 9	bxn offset 8	bxn offset 7	bxn offset 6	bxn offset 5	bxn offset 4	bxn offset 3	bxn offset 2	bxn offset 1	bxn offset 0	l1a offset 3	l1a offset 2	l1a offset 1	l1a offset 0

Bits	Dir	Signal	Default	Description
[03:00]	R/W	l1a_offset[3:0]	0	L1A counter preset value
[15:04]	R/W	bxn_ofset[11:0]	0	BXN offset at reset

Adr 78 ADR_SEQ_CLCT0 Sequencer Latched CLCT0 (LSBs)
(Split with Adr B0 ADR_SEQCLCTM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st cfeb 1	1st cfeb 0	1st key 4	1st key 3	1st key 2	1st key 1	1st key 0	bend pat 0	hs/ds pat 3	shape pat 2	shape pat 1	shape pat 0	hits pat 2	hits pat 1	hits pat 0	1st vpf

Bits	Dir	Signal	Typical	Description
[00]	R	clct_first_valid	1	Valid pattern flag
[03:01]	R	clct_first_nhit[2:0]	4-6	Hits on pattern: 0 to 6
[06:04]	R	clct_first_pat[2:0]	0-7	Pattern shape 0 to 7
[07]	R	clct_first_pat[3]	0-1	1=½-Strip, 0=Di-Strip
[08]	R	clct_first_pat[0]	0	Bend direction (=pattern lsb with current pattern set)
[13:09]	R	clct_first_key[4:0]	$0\text{-}31_{10}$	Key ½-strip (Di-Strips point to lower ½-Strip)
[16:14]	R	clct_first_cfeb[2:0]	0-4	Key CFEB ID
[18:17]	R	clct_first_bxn[1:0]	0-3	Bunch crossing number
[19]	R	sync_err	0	Sync error
[20]	R	bx0_local	0	BXN=0 on this TMB

Adr 7A ADR_SEQ_CLCT1 Sequencer Latched CLCT1 (LSBs)
(Split with Adr B0 ADR_SEQCLCTM)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2nd cfeb 1	2nd cfeb 0	2nd key 4	2nd key 3	2nd key 2	2nd key 1	2nd key 0	bend pat 0	hs/ds pat 3	shape pat 2	shape pat 1	shape pat 0	hits pat 2	hits pat 1	hits pat 0	2nd vpf

Bits	Dir	Signal	Typical	Description
[00]	R	clct_second_valid	1	Valid pattern flag
[03:01]	R	clct_second_nhit[2:0]	4-6	Hits on pattern: 0 to 6
[06:04]	R	clct_second_pat[2:0]	0-7	Pattern shape 0 to 7
[07]	R	clct_second_pat[3]	0-1	1=½-Strip, 0=Di-Strip
[08]	R	clct_second_pat[0]	0	Bend direction (=pattern lsb with current pattern set)
[13:09]	R	clct_second_key[4:0]	$0\text{-}31_{10}$	Key ½-strip (Di-Strips point to lower ½-Strip)
[16:14]	R	clct_second_cfeb[2:0]	0-4	Key CFEB ID
[18:17]	R	clct_second_bxn[1:0]	0-3	Bunch crossing number
[19]	R	sync_err	0	Sync error
[20]	R	bx0_local	0	BXN=0 on this TMB

Adr 7C ADR_SEQ_TRIG_SRC Sequencer Trigger Source Read-back

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	vme trig	alct ext trig en	clct ext trig en	adb ext trig en	adb ext trig en	alct*clct pat trig en	alct pat trig en	clct pat trig en

Bits	Dir	Signal	Typical	Description
[00]	R	clct_pat_trig_en	1	CLCT pattern triggered sequencer
[01]	R	alct_pat_trig_en	0	ALCT pattern triggered sequencer
[02]	R	match_pat_trig_en	0	ALCT*CLCT pattern triggered sequencer
[03]	R	adb_ext_trig_en	0	ADB external triggered sequencer
[04]	R	dmb_ext_trig_en	0	DMB external triggered sequencer
[05]	R	clct_ext_trig_en	0	CLCT (CCB scintillator) external triggered sequencer
[06]	R	alct_ext_trig_en	0	ALCT (CCB) external triggered sequencer
[07]	R	vme_ext_trig	0	VME triggered sequencer
[15:07]	R/W	--	0	Unassigned

Adr 7E ADR_DMB_RAM_ADR Sequencer RAM Address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
dmb wdata 17	dmb wdata 16	dmb reset	dmb wr	dmb adr 11	dmb adr 10	dmb adr 9	dmb adr 8	dmb adr 7	dmb adr 6	dmb adr 5	dmb adr 4	dmb adr 3	dmb adr 2	dmb adr 1	dmb adr 0

Bits	Dir	Signal	Default	Description
[11:00]	R/W	dmb_adr[11:0]	0	Raw hits RAM VME read/write address
[12]	R/W	dmb_wr	0	Raw hits RAM VME write enable
[13]	R/W	dmb_reset	0	Raw hits RAM VME address reset
[15:14]	R/W	dmb_wdata[17:16]	0	Raw hits RAM VME write data MSBs

Adr 80 ADR_DMB_RAM_WDATA Sequencer RAM Write Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
dmb wdata 15	dmb wdata 14	dmb wdata 13	dmb wdata 12	dmb wdata 11	dmb wdata 10	dmb wdata 9	dmb wdata 8	dmb wdata 7	dmb wdata 6	dmb wdata 5	dmb wdata 4	dmb wdata 3	dmb wdata 2	dmb wdata 1	dmb wdata 16

Bits	Dir	Signal	Default	Description
[15:00]	R/W	dmb_wdata[15:0]	0	Raw hits RAM VME write data (msb in adr 76)

Adr 82 ADR_DMB_RAM_WDCNT Sequencer RAM Word Count

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	dmb busy	dmb rdata 17	dmb wdata 16	dmb wdcnt 11	dmb wdcnt 10	dmb wdcnt 9	dmb wdcnt 8	dmb wdcnt 7	dmb wdcnt 6	dmb wdcnt 5	dmb wdcnt 4	dmb wdcnt 3	dmb wdcnt 2	dmb wdcnt 1	dmb wdcnt 0

Bits	Dir	Signal	Default	Description
[11:00]	R	dmb_wdcnt[11: 0]	0	Raw hits RAM VME word count
[13:12]	R	dmb_rdata[17:16];	0	Raw hits RAM VME read data MSBs
[14]	R	dmb_busy	0	Raw hits RAM VME
[15]	R	--	0	Unassigned

Adr 84 ADR_DMB_RAM_RDATA Sequencer RAM Read Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
dmb rdata 15	dmb rdata 14	dmb rdata 13	dmb rdata 12	dmb rdata 11	dmb rdata 10	dmb rdata 9	dmb rdata 8	dmb rdata 7	dmb rdata 6	dmb rdata 5	dmb rdata 4	dmb rdata 3	dmb rdata 2	dmb rdata 1	dmb rdata 16

Bits	Dir	Signal	Default	Description
[15:00]	R	dmb_rdata[15:0]	0	Raw hits RAM VME read data (msb in adr 7A)

Adr 86 ADR_TMB_TRIG TMB Trigger Configuration / MPC Accept

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	mpc reserved 1	mpc reserved 0	mpc accept 1	mpc accept 0	mpc delay 3	mpc delay 2	mpc delay 1	mpc delay 0	allow clct+alct match	allow clct only	allow alct only	sync err en 1	sync err en 0

Bits	Dir	Signal	Default	Description
[01:00]	R/W	tmb_sync_err_en[1:0]	11_2	Allow sync_err to MPC for either muon
[02]	R/W	tmb_allow_alct	0	Allow ALCT-only L1A (not used in current version)
[03]	R/W	tmb_allow_clct	1	Allow CLCT0-only L1A
[04]	R/W	tmb_allow_match	1	Allow ALCT+CLCT match pre-trigger
[08:05]	R/W	mpc_delay	7	MPC accept response delay
[10:09]	R	mpc_accept[1:0]	-	MPC accept latched after delay
[12:11]	R	mpc_reserved[1:0]	-	MPC reserved latched after delay
[15:13]	R/W	--	0	Unassigned

Adr 88 ADR_MPC0_FRAME0 MPC0 Frame0 Data Sent to MPC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st vpf	lct 1st q 3	lct 1st q 2	lct 1st q 1	lct 1st q 0	clct 1st hsds	clct 1st pat 2	clct 1st pat 1	clct 1st pat 0	alct 1st wg 6	alct 1st wg 5	alct 1st wg 4	alct 1st wg 3	alct 1st wg 2	alct 1st wg 1	alct 1st wg 0

Bits	Dir	Signal	Typical	Description
[06:00]	R	alct_first_key[6:0]	$0\text{-}111_{10}$	ALCT first key wire-group
[09:07]	R	clct_first_pat[2:0]	4-6	CLCT first pattern number
[10]	R	clct_first_hsds	0-1	CLCT 1=1/2-Strip Pattern, 0=DiStrip Pattern
[14:11]	R	lct_first_quality[3:0]	8	LCT first muon quality
[15]	R	first_vpf	1	First valid pattern flag

Adr 8A ADR_MPC0_FRAME1 MPC0 Frame1 Data Sent to MPC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
csc id 3	csc id 2	csc id 1	csc id 0	tmb bx0 local	alct 1st bxn 0	sync err	clct 1st bend	clct 1st key 7	clct 1st key 6	clct 1st key 5	clct 1st key 4	clct 1st key 3	clct 1st key 2	clct 1st key 1	clct 1st key 0

Bits	Dir	Signal	Typical	Description
[07:00]	R	clct_first_key[7:0]	$0\text{-}159_{10}$	CLCT first muon key ½-strip
[08]	R	clct_first_bend	0	CLCT first muon bend direction
[09]	R	sync_err	0	BXN does not match at BX0
[10]	R	alct_first_bxn[0]	0-1	ALCT first muon bunch crossing number
[11]	R	clct_first_bx0_local	0-1	1=TMBs bxn[11:0]==0
[15:12]	R	csc_id[3:0]	1-9	CSC chamber ID

Adr 8C ADR_MPC1_FRAME0 MPC1 Frame0 Data Sent to MPC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2nd vpf	lct 2nd q 3	lct 2nd q 2	lct 2nd q 1	lct 2nd q 0	clct 2nd hsds	clct 2nd pat 2	clct 2nd pat 1	clct 2nd pat 0	alct 2nd wg 6	alct 2nd wg 5	alct 2nd wg 4	alct 2nd wg 3	alct 2nd wg 2	alct 2nd wg 1	alct 2nd wg 0

Bits	Dir	Signal	Typical	Description
[06:00]	R	alct_second_key[6:0]	$0\text{-}111_{10}$	ALCT second key wire-group
[09:07]	R	clct_second_pat[2:0]	4-6	CLCT second pattern number
[10]	R	clct_second_hsds	0-1	CLCT 1=1/2-Strip Pattern, 0=DiStrip Pattern
[14:11]	R	lct_second_quality[3:0]	8	LCT second muon quality
[15]	R	second_vpf	1	Second valid pattern flag

Adr 8E ADR_MPC1_FRAME1 MPC1 Frame1 Data Sent to MPC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
csc id 3	csc id 2	csc id 1	csc id 0	tmb bx0 local	alct 2^{nd} bxn 0	sync err	clct 2^{nd} bend	clct 2^{nd} key 7	clct 2^{nd} key 6	clct 2^{nd} key 5	clct 2^{nd} key 4	clct 2^{nd} key 3	clct 2^{nd} key 2	clct 2^{nd} key 1	clct 2^{nd} key 0

Bits	Dir	Signal	Typical	Description
[07:00]	R	clct_second_key[7:0]	$0\text{-}159_{10}$	CLCT second muon key ½-strip
[08]	R	clct_second_bend	0	CLCT second muon bend direction
[09]	R	sync_err	0	BXN does not match at BX0
[10]	R	alct_second_bxn[0]	0-1	ALCT second muon bunch crossing number
[11]	R	clct_second_bx0_local	0-1	1=TMBs bxn[11:0]==0
[15:12]	R	csc_id[3:0]	1-9	CSC chamber ID

Adr 90 ADR_MPC_INJ MPC Injector Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	mpc reserv 1	mpc reserv 0	mpc accept 1	mpc accept 0	mpc inject	mpc nfram 7	mpc nfram 6	mpc nfram 5	mpc nfram 4	mpc nfram 3	mpc nfram 2	mpc nfram 1	mpc nfram 0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	mpc_nframes[7:0]	5	Number frames to inject
[08]	R/W	mpc_inject	0	1=Start MPC test pattern injector
[09]	R/W	ttc_mpc_inj_en	1	1=Enable injector start by TTC command
[11:10]	R	mpc_accept[1:0]	-	MPC accept stored at injector RAM address
[13:12]	R	mpc_reserved[1:0]	-	MPC reserved stored at injector RAM address
[15:14]	R/W	--	0	Unassigned

Adr 92 ADR_MPC_RAM_ADR MPC Injector RAM Address

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
mpc adr 7	mpc adr 6	mpc adr 5	mpc adr 4	mpc adr 3	mpc adr 2	mpc adr 1	mpc adr 0	mpc ren 3	mpc ren 2	mpc ren 1	mpc ren 0	mpc wen 3	mpc wen 2	mpc wen 1	mpc wen 0

Bits	Dir	Signal	Default	Description
[03:00]	R/W	mpc_wen[3:0]	0	Select RAM to write
[07:04]	R/W	mpc_ren[3:0]	0	Select RAM to read
[15:08]	R/W	mpc_adr[7:0]	0	Injector RAM read/write address

Adr 94 ADR_MPC_RAM_WDATA MPC Injector RAM Write Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
mpc wdata 7	mpc wdata 6	mpc wdata 5	mpc wdata 4	mpc wdata 3	mpc wdata 2	mpc wdata 1	mpc wdata 0	mpc wdata 3	mpc wdata 2	mpc wdata 1	mpc wdata 0	mpc wdata 3	mpc wdata 2	mpc wdata 1	mpc wdata 0

Bits	Dir	Signal	Default	Description
[15:00]	R/W	mpc_wdata[15:0]	0	MPC Injector RAM write data

Adr 96 ADR_MPC_RAM_RDATA MPC Injector RAM Read Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
mpc rdata 7	mpc rdata 6	mpc rdata 5	mpc rdata 4	mpc rdata 3	mpc rdata 2	mpc rdata 1	mpc rdata 0	mpc rdata 3	mpc rdata 2	mpc rdata 1	mpc rdata 0	mpc rdata 3	mpc rdata 2	mpc rdata 1	mpc rdata 0

Bits	Dir	Signal	Default	Description
[15:00]	R	mpc_rdata[15:0]	0	MPC Injector RAM read data

Adr 98 ADR_SCP_CTRL Scope Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
radr 7	radr 6	radr 5	radr 4	radr 3	radr 2	radr 1	radr 0	trig done	waitin for trigger	auto	ram sel 2	ram sel 1	ram sel 0	force	run stop

Bits	Dir	Signal	Default	Description
[00]	R/W	scp_runstop	0	1=Run, 0=Stop
[01]	R/W	scp_force_trig	0	1=Force a trigger (set 0,1,0 in 3 writes)
[04:02]	R/W	scp_ram_sel[2:0]	0	RAM bank to read / last RAM adr if scp_auto=1
[05]	R/W	scp_auto	0	Sequencer readout mode 1=insert in DMB data
[06]	R	scp_waiting		Scope waiting for trigger
[07]	R	scp_trig_done		Scope triggered, ready for readout
[15:08]	R/W	scp_radr[7:0]		Scope data read address

Adr 9A ADR_SCP_RDATA Scope Read data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
scp ch 15	scp ch 14	scp ch 13	scp ch 12	scp ch 11	scp ch 10	scp ch 9	scp ch 8	scp ch 7	scp ch 6	scp ch 5	scp ch 4	scp ch 3	scp ch 2	scp ch 1	scp ch 0

Bits	Dir	Signal		Description
[15:00]	R	scp_data[15:0]		See channel assignments on page 44

Adr 9C ADR_CCB_CMD CCB TTC Command Generator (Internal)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ccb cmd 7	ccb cmd 6	ccb cmd 5	ccb cmd 4	ccb cmd 3	ccb cmd 2	ccb cmd 1	ccb cmd 0	0	0	fmm state 1	fmm state 0	subadr strobe	data strobe	brcst strobe	dis con ccb

Bits	Dir	Signal	Default	Description
[00]	R/W	vme_ccb_cmd_enable	0	1=Disconnect CCB backplane ccb_cmd[7:0]
[01]	R/W	vme_ccb_cmd_strobe	0	1=Assert internal ccb_cmd brcst strobe
[02]	R/W	vme_ccb_data_strobe	0	1=Assert internal ccb_cmd data strobe
[03]	R/W	vme_ccb_subaddr_strobe	0	1=Assert internal ccb_cmd sub-adr strobe
[05:04]	R	fmm_state[1:0]		FMM machine state
[07:06]	R/W	-		Unassigned
[15:08]	R/W	vme_ccb_cmd[7:0]	0	TTC command to generate

Adr 9E ADR_BUF_STAT Buffer Status

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
buffer busy 7	buffer busy 6	buffer busy 5	buffer busy 4	buffer busy 3	buffer busy 2	buffer busy 1	buffer busy 0	peak busy 3	peak busy 2	peak busy 1	peak busy 0	nbusy 3	nbusy 2	nbusy 1	nbusy 0

Bits	Dir	Signal		Description
[03:00]	R	buf_nbusy[3:0]		Number of buffer busy
[07:04]	R	buf_nbusy_peak[3:0]		Peak buffer usage
[15:08]	R	buf_busy[7:0]		List of busy buffers

Adr A0 ADR_SRLPGM SRL LUT Program

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	resq 0	srl dsq 4	srl dsq 3	srl dsq 2	srl dsq 1	srl dsq 0	srl hsq 4	srl hsq 3	srl hsq 2	srl hsq 1	srl hsq 0

Bits	Dir	Signal	Default	Description
[04:00]	R	srl_hsq[4:0]		CFEB ½-Strip SRL serial data out
[09:05]	R	srl_dsq[4:0]		CFEB Di-Strip SRL serial data out
[10]	R	srl_resq		Resolver SRL serial data out
[15:11]	R	-	0	Unassigned

Adr A2 ADR_ALCTFIFO1 ALCT Raw Hits RAM Control
(Split with Adr 3E ADR_ALCT_FIFO0 and Adr A4 ADR_ALCT_FIFO2)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	alct radr 10	alct radr 9	alct radr 8	alct radr 7	alct radr 6	alct radr 5	alct radr 4	alct radr 3	alct radr 2	alct radr 1	alct radr 0	alct raw reset

Bits	Dir	Signal	Default	Description
[00]	R/W	alct_raw_reset	0	Reset ALCT raw hits FIFO controller
[11:01]	R/W	alct_raw_radr[10:0]	0	ALCT raw hits RAM address to read
[12]	R/W	alct_raw_sync	0	1=Sync alct FIFO write to TMB readout
[15:13]	R/W	--	0	Unassigned

Adr A4 ADR_ALCTFIFO2 ALCT Raw Hits RAM data (LSBs)
(Split with Adr 3E ADR_ALCT_FIFO0 and Adr A2 ADR_ALCT_FIFO1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
alct fifo 15	alct fifo 14	alct fifo 13	alct fifo 12	alct fifo 11	alct fifo 10	alct fifo 9	alct fifo 8	alct fifo 7	alct fifo 6	alct fifo 5	alct fifo 4	alct fifo 3	alct fifo 2	alct fifo 1	alct fifo 0

Bits	Dir	Signal	Default	Description
[15:00]	R	alct_raw_rdata[15:0]		ALCT FIFO data (msbs in adr_alct_fifo)

Adr A6 ADR_ADJCFEB0 CFEB Adjacent hs Mask (LSBs)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
hs 15	hs 14	hs 13	hs 12	hs 11	hs 10	hs 9	hs 8	hs 7	hs 6	hs 5	hs 4	hs 3	hs 2	hs 1	hs 0

Bits	Dir	Signal	Default	Description
[15:00]	R/W	adjcfeb_mask_hs[15:0]	000F	1=Enable ½-Strip for adjecent CFEB hit in aff

Adr A8 ADR_ADJCFEB1 CFEB Adjacent hs Mask (MSBs)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
hs 31	hs 30	hs 29	hs 28	hs 27	hs 26	hs 25	hs 24	hs 23	hs 22	hs 21	hs 20	hs 19	hs 18	hs 17	hs 16

Bits	Dir	Signal	Default	Description
[15:00]	R/W	adjcfeb_mask_hs[31:16]	F000	1=Enable ½-Strip for adjecent CFEB hit in aff

Adr AA ADR_ADJCFEB2 CFEB Adjacent ds Mask

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	ds 7	ds 6	ds 5	ds 4	ds 3	ds 2	ds 1	ds 0

Bits	Dir	Signal	Default	Description
[07:00]	R/W	adjcfeb_mask_ds[7:0]	81_{16}	1=Enable DiStrip for adjecent CFEB hit in aff
[15:08]	R/W	-	0	Unassigned

Adr AC ADR_SEQMOD Sequencer Trigger Modifiers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Scint veto state	Clear scint veto	L1A alct only	L1A tmb nol1a	L1A no tmb	L1A tmb trig	valid clct requir	wr buf requir	ranlct	clct turbo	flush timer 3	flush timer 2	flush timer 1	flush timer 0

Bits	Dir	Signal	Default	Description
[03:00]	R/W	clct_flush_delay[3:0]	1	Trigger sequencer flush state timer
[04]	R/W	clct_turbo	0	Trigger sequencer turbo mode! (no raw hits)
[05]	R/W	ranlct_enable	0	1=Enable OSU random LCT generator Requires external trigger mode + pat thresh=7
[06]	R/W	wr_buf_required	1	Require wr_buffer available to pre-trigger
[07]	R/W	valid_clct_required	1	Require valid CLCT after drift delay
[08]	R/W	l1a_allow_match	1	Readout allows tmb trig pulse in L1A window
[09]	R/W	l1a_allow_notmb	0	Readout allows notmb trig pulse in L1A window
[10}	R/W	l1a_allow_nol1a	0	Readout allows tmb trig pulse outside L1A wind
[11]	R/W	l1a_allow_alct_only	0	Allow ALCT-only events to readout at L1A
[12]	R/W	scint_veto_clr	0	Clear scintillator veto FF
[13]	R	scint_veto_vme		Scintillator veto FF state
[15:14]	R/W	--	0	Unassigned

Adr AE ADR_SEQSM Sequencer Machine State

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	stack udf	stack ovf	stack empty	stack full	read sm 4	read sm 3	read sm 2	read sm 1	read sm 0	tmb sm 2	tmb sm 1	tmb sm 0	clct sm 2	clct sm 1	clct sm 0

Bits	Dir	Signal		Description
[02:00]	R	clct_sm[2:0]		CLCT Trigger machine state
[05:03]	R	tmb_sm[2:0]		TMB Match machine state
[10:06]	R	read_sm[4:0]		Readout machine state
[11]	R	stack_full		Readout stack full
[12]	R	stack_empty		Readout stack empty
[13]	R	stack_ovf		Attempt to push new even when stack full
[14]	R	stack_udf		Attepmt to pop stack when empty
[15]	R	--	0	Unassigned

Adr B0 ADR_SEQCLCTM Sequencer CLCT (MSBs)
(Split with Adr 78 ADR_SEQCLCT0 and Adr 7A ADR_SEQCLCT1)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	2nd clct 20	2nd clct 19	2nd clct 18	2nd clct 17	2nd clct 16	1st clct 20	1st clct 19	1st clct 18	1st clct 17	1st clct 16

Bits	Dir	Signal		Description
[04:00]	R	clct_first[20:16]		First CLCT MSBs (see 78 ADR_SEQCLCT0)
[09:05]	R	clct_second[20:16]		Second CLCT MSBs (see 78 ADR_SEQCLCT0)
[15:10]	R	--	0	Unassigned

Adr B2 ADR_TMBTIM TMB Timing for ALCT*CLCT Coincidence

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	clct width 3	clct width 2	clct width 1	clct width 0	alct delay 3	alct delay 2	alct delay 1	alct delay 0

Bits	Dir	Signal	Default	Description
[03:00]	R/W	alct_delay[3:0]	1	Delay ALCT for CLCT match window
[07:04]	R/W	clct_width[3:0]	3	CLCT match window width
[15:08]	R/W	--	0	Unassigned

Adr B4 ADR_LHC_CYCLE LHC Cycle Period, Maximum BXN Count

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	lhc cycle 11	lhc cycle 10	lhc cycle 9	lhc cycle 8	lhc cycle 7	lhc cycle 6	lhc cycle 5	lhc cycle 4	lhc cycle 3	lhc cycle 2	lhc cycle 1	lhc cycle 0

Bits	Dir	Signal	Default	Description
[11:00]	R/W	lhc_cycle[11:0]	3564	Maximum bxn+1 3564(hDEC) for LHC 924(h39C) for beam test
[15:12]	R/W	--	0	Unassigned

Adr B6 ADR_RPC_CFG RPC Configuration

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	read bxn 2	read bxn 1	read bxn 0	read bank 1	read bank 0	bxn offset 3	bxn offset 2	bxn offset 1	bxn offset 0	read enable	rpc3 exists	rpc2 exists	rpc1 exists	rpc0 exists

Bits	Dir	Signal	Default	Description
[03:00]	R/W	rpc_exists[3:0]	F	Bit (n) = 1 = RPC(n) Exists, F=all 4 exist
[04]	R/W	rpc_read_enable	1	1=Include Existing RPCs in DMB Readout
[08:05]	R/W	rpc_bxn_offset[3:0]	0	RPC BXN offset
[10:09]	R/W	rpc_bank[1:0]	0	RPC bank address, for reading rdata sync mode
[13:11]	R	rpc_rbxn[2:0]	-	RPC rdata[18:16] msbs for sync mode, adr 1E
[15:14]	R/W	--	0	Unassigned

Adr B8 ADR_RPC_RDATA RPC Raw Hits Sync Mode Read Data, See Adr 1E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rdata 15	rdata 14	rdata 13	rdata 12	rdata 11	rdata 10	rdata 9	rdata 8	rdata 7	rdata 6	rdata 5	rdata 4	rdata 3	rdata 2	rdata 1	rdata 0

Bits	Dir	Signal	Default	Description
[15:00]	R	rpc_rdata[15:0]	-	RPC RAM read data for sync mode

Adr BA ADR_RPC_RAW_DELAY RPC Raw Hits Data Delay

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rpc3 delay 3	rpc3 delay 2	rpc3 delay 1	rpc3 delay 0	rpc2 delay 3	rpc2 delay 2	rpc2 delay 1	rpc2 delay 0	rpc1 delay 3	rpc1 delay 2	rpc1 delay 1	rpc1 delay 0	rpc0 delay 3	rpc0 delay 2	rpc0 delay 1	rpc0 delay 0

Bits	Dir	Signal	Default	Description
[03:00]	R/W	rpc0_delay[3:0]	1	RPC0 Raw hits data delay
[07:04]	R/W	rpc1_delay[3:0]	1	RPC1 Raw hits data delay
[11:08]	R/W	rpc2_delay[3:0]	1	RPC2 Raw hits data delay
[15:12]	R/W	rpc3_delay[3:0]	1	RPC3 Raw hits data delay

Adr BC ADR_RPC_INJ RPC Injector Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	inj rdata 18	inj rdata 17	inj rdata 16	inj wdata 18	inj wdata 17	inj wdata 16	inj sel	delay rat 3	delay rat 2	delay rat 1	delay rat 0	mask rpc	mask rat	mask all

Bits	Dir	Signal	Default	Description
[00]	R/W	rpc_mask_all	1	1=Enable RPC Inputs from RAT, 0=disable all
[01]	R/W	injector_mask_rat	0	1=Enable RAT for injector fire
[02]	R/W	injector_mask_rpc	1	1=Enable RPC injector RAM for injector fire
[06:03]	R/W	inj_delay_rat[3:0]	0	CFEB/RPC injectors wait for RAT
[07]	R/W	rpc_inj_sel	0	1=Enable injector RAM write
[10:08]	R/W	rpc_inj_wdata[18:16]	0	RPC injector write data MSBs, see adr C0
[13:11]	R	rpc_inj_rdata[18:16]	-	RPC injector read data MSBs, see adr C0
[15:14]	R/W	--	0	Unassigned

Adr BE ADR_RPC_INJ_ADR RPC Injector RAM Addresses

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
inj adr 7	inj adr 6	inj adr 5	inj adr 4	inj adr 3	inj adr 2	inj adr 1	inj adr 0	inj ren 3	inj ren 2	inj ren 1	inj ren 0	inj wen 3	inj wen 2	inj wen 1	inj wen 0

Bits	Dir	Signal	Default	Description
[03:00]	R/W	rpc_inj_wen[3:0]	0	1=Write enable injector RAMn
[07:04]	R/W	rpc_inj_ren[3:0]	0	1=Read enable Injector RAMn
[15:08]	R/W	inj_rwadr[7:0]	0	Injector RAM read/write address

Adr C0 ADR_RPC_INJ_WDATA RPC Injector Write Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
inj wdata 15	inj wdata 14	inj wdata 13	inj wdata 12	inj wdata 11	inj wdata 10	inj wdata 9	inj wdata 8	inj wdata 7	inj wdata 6	inj wdata 5	inj wdata 4	inj wdata 3	inj wdata 2	inj wdata 1	inj wdata 0

Bits	Dir	Signal	Default	Description
[15:00]	R/W	rpc_inj_wdata[15:0]	0	RPC RAM write data LSBs (see adr BC msbs)

Adr C2 ADR_RPC_INJ_RDATA RPC Injector Read Data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
inj rdata 15	inj rdata 14	inj rdata 13	inj rdata 12	inj rdata 11	inj rdata 10	inj rdata 9	inj rdata 8	inj rdata 7	inj rdata 6	inj rdata 5	inj rdata 4	inj rdata 3	inj rdata 2	inj rdata 1	inj rdata 0

Bits	Dir	Signal	Default	Description
[15:00]	R	rpc_inj_rdata[15:0]	-	RPC RAM read data LSBs (see adr BC msbs)

Adr C4 ADR_RPC_BXN_DIFF RPC BXN Differences

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rpc3 bxn diff3	rpc3 bxn diff2	rpc3 bxn diff1	rpc3 bxn diff0	rpc2 bxn diff3	rpc2 bxn diff2	rpc02 bxn diff1	rpc2 bxn diff0	rpc1 bxn diff3	rpc1 bxn diff2	rpc1 bxn diff1	rpc1 bxn diff0	rpc0 bxn diff3	rpc0 bxn diff2	rpc0 bxn diff1	rpc0 bxn diff0

Bits	Dir	Signal	Default	Description
[03:00]	R	rpc0_bxn_diff[3:0]	-	RPC bxn – Offset (in adr B6)
[07:04]	R	rpc1_bxn_diff[3:0]	-	RPC bxn – Offset (in adr B6)
[11:08]	R	rpc2_bxn_diff[3:0]	-	RPC bxn – Offset (in adr B6)
[15:12]	R	rpc3_bxn_diff[3:0]	-	RPC bxn – Offset (in adr B6)

Adr C6 ADR_RPC0_HCM RPC0 Hot Channel Mask

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
enable pad15	enable pad14	enable pad13	enable pad12	enable pad11	enable pad10	enable pad9	enable pad8	enable pad7	enable pad6	enable pad5	enable pad4	enable pad3	enable pad2	enable pad1	enable pad0

Bits	Dir	Signal	Default	Description
[15:00]	R/W	rpc0_hcm[15:0]	FFFF	Bit(n)=1=Enable RPC Pad(n), FFFF=enable all

Adr C8 ADR_RPC1_HCM RPC1 Hot Channel Mask

Bits	Dir	Signal	Default	Description
[15:00]	R/W	rpc1_hcm[15:0]	FFFF	Bit(n)=1=Enable RPC Pad(n), FFFF=enable all

Adr CA ADR_RPC2_HCM RPC2 Hot Channel Mask

Bits	Dir	Signal	Default	Description
[15:00]	R/W	rpc2_hcm[15:0]	FFFF	Bit(n)=1=Enable RPC Pad(n), FFFF=enable all

Adr CC ADR_RPC3_HCM RPC3 Hot Channel Mask

Bits	Dir	Signal	Default	Description
[15:00]	R/W	rpc3_hcm[15:0]	FFFF	Bit(n)=1=Enable RPC Pad(n), FFFF=enable all

TTC Commands:

Fast Control Bus ccb_cmd[5..0] Decoding Scheme

Signal	Code (hex)	Decoded by TMB	Description
BX0 (*)	1	Y	Bunch Crossing Zero
L1 Reset (*)	3	Y	Reset L1 readout buffers and resynchronize optical links
Hard_reset (*)	4		Reload all FPGAs from EPROMs
Start Trigger	6	Y	
Stop Trigger	7	Y	
Test Enable	8		
Private Gap	9		
Private Orbit	A		
Tmb_hard_reset (*)	10		Reload TMB FPGAs from EPROM
Alct_hard_reset (*)	11		Reload ALCT FPGAs from EPROM
Dmb_hard_reset (*)	12		Reload DMB FPGAs from EPROM
Mpc_hard_reset (*)	13		Reload MPC FPGAs from EPROM
Dmb_cfeb_calibrate0 (*)	14		CFEB Calibrate Pre-Amp Gain
Dmb_cfeb_calibrate1 (*)	15		CFEB Trigger Pattern Calibration
Dmb_cfeb_calibrate2 (*)	16		CFEB Pedestal Calibration
Dmb_cfeb_initiate (*)	17		Initiate CFEB calibration (Hold next L1ACC and Pretriggers)
Alct_adb_pulse_sync (*)	18		Pulse Anode Discriminator, synchronous
Alct_adb_pulse_async (*)	19		Pulse Anode Discriminator, asynchronous
Clct_external_trigger (*)	1A		External Trigger All CLCTs
Alct_external_trigger (*)	1B		External Trigger All ALCTs
Soft_reset (*)	1C		Initializes the FPGA on DMB, TMB and MPC boards
DMB_soft_reset (*)	1D		Initializes the FPGA on a DMB
TMB_soft_reset (*)	1E		Initializes the FPGA on a TMB
MPC_soft_reset (*)	1F		Initializes the FPGA on a MPC
Send_bcnt[7..0] (*)	20		Send Bunch_Counter[7..0] to ccb_data[7..0] bus
Send_evcnt[7..0] (*)	21		Send Event_Counter[7..0] to ccb_data[7..0] bus
Send_evcnt[15..8] (*)	22		Send Event_Counter[15..8] to ccb_data[7..0] bus
Send_evcnt[23..16] (*)	23		Send Event_Counter[23..16] to ccb_data[7..0] bus
Inject patterns from TMBs	24	Y	Injects patterns from TMB's internal RAM to MPC
Alct_adb_pulse (*)	25		Generate sync and async anode discriminator pulses
Inject patterns from MPCs	30		Injects patterns from MPC's input FIFO to SP
Inject patterns from MS	31		Injects patterns from MS input FIFO to Global Muon Trigger
tmb_bxreset	32	Y	Reset TMB/ALCT BXN, do not reset L1A counters

(*) – decoded by CCB

Embedded Logic Analyzer Scope Channels:

Embedded Logic Analyzer Scope Channels

Channel	Signal	Description
ch00	sequencer pretrig	
ch01	active_feb_flag	
ch02	any_cfeb_hit	
ch03	any_cfeb_hsds	
ch04	wr_buf_busy	
ch05	wr_buf_ready	
ch06	clct_ext_trig_os	
ch07	alct_active_feb	
ch08	alct_pretrig_win	
ch09	first_really_valid	
ch10	clct_sm==xtmb	
ch11	tmb_discard	
ch12	discard_nobuf	
ch13	discard_invp	
ch14	discard_tmbreject	
ch15	0 (no dmb readout)	
ch16	first_nhit[0]	
ch17	first_nhit[1]	
ch18	first_nhit[2]	
ch19	first_pat[3]hsds	
ch20	second_nhit[0]	
ch21	second_nhit[1	
ch22	second_nhit[2]	
ch23	second_pat[3]hsds	
ch24	latch_clct0	
ch25	latch_clct1	
ch26	alct_1st_valid	
ch27	alct_2nd_valid	
ch28	alct_vpf_tp	
ch29	clct_vpf_tp	
ch30	clct_window_tp	
ch31	0 (no dmb readout)	
ch32	sequencer pretrig	
ch33	mpc_frame_ff	
ch34	mpc_response_ff	
ch35	mpc_accept_tp[0]	
ch36	mpc_accept_tp[1]	
ch37	l1a_pulse_dsp	
ch38	l1a_window_dsp	
ch39	dmb_dav_mux	
ch40	dmb_busy	
ch41	hs_thresh[0]	
ch42	hs_thresh[1]	
ch43	hs_thresh[2]	
ch44	ds_thresh[0]	
ch45	ds_thresh[1]	
ch46	ds_thresh[2]	
ch47	0(no dmb readout)	

ch48	sequencer pretrig	
ch49	valid_clct_required	
ch50	buf_nbusy[0]	
ch51	buf_nbusy[1]	
ch52	buf_nbusy[2]	
ch53	buf_nbusy[3]	
ch54	0	
ch55	0	
ch56	0	
ch57	0	
ch58	0	
ch59	l1a_rx_counter[0]	
ch60	l1a_rx_counter[1]	
ch61	l1a_rx_counter[2]	
ch62	l1a_rx_counter[3]	
ch63	0 (no dmb readout)	
ch64	sequencer pretrig	
ch65	bxn_counter[0]	
ch66	bxn_counter[1]	
ch67	bxn_counter[2]	
ch68	bxn_counter[3]	
ch69	bxn_counter[4]	
ch70	bxn_counter[5]	
ch71	bxn_counter[6]	
ch72	bxn_counter[7]	
ch73	bxn_counter[8]	
ch74	bxn_counter[9]	
ch75	bxn_counter[10]	
ch76	bxn_counter[11]	
ch77	0	
ch78	0	
ch79	0 (no dmb readout)	
ch80	dmb seq_wdata[0]	
ch81	dmb seq_wdata[1]	
ch82	dmb seq_wdata[2]	
ch83	dmb seq_wdata[3]	
ch84	dmb seq_wdata[4]	
ch85	dmb seq_wdata[5]	
ch86	dmb seq_wdata[6]	
ch87	dmb seq_wdata[7]	
ch88	dmb seq_wdata[8]	
ch89	dmb seq_wdata[9]	
ch90	dmb seq_wdata[10]	
ch91	dmb seq_wdata[11]	
ch92	dmb seq_wdata[12]	
ch93	dmb seq_wdata[13]	
ch94	dmb seq_wdata[14]	
ch95	dmb seq_wdata[15]	
ch96	rpc0_bxn[0]	
ch97	rpc0_bxn[1]	
ch98	rpc0_bxn[2]	
ch99	rpc1_bxn[0]	

ch100	rpc1_bxn[1]	
ch101	rpc1_bxn[2]	
ch102	rpc2_bxn[0]	
ch103	rpc2_bxn[1]	
ch104	rpc2_bxn[2]	
ch105	rpc3_bxn[0]	
ch106	rpc3_bxn[1]	
ch107	rpc3_bxn[2]	
ch108	0	
ch109	0	
ch110	0	
ch111	0	
ch112	rpc0_nhits[0]	
ch113	rpc0_nhits[1]	
ch114	rpc0_nhits[2]	
ch115	rpc0_nhits[3]	
ch116	rpc1_nhits[0]	
ch117	rpc1_nhits[1]	
ch118	rpc1_nhits[2]	
ch119	rpc1_nhits[3]	
ch120	rpc2_nhits[0]	
ch121	rpc2_nhits[1]	
ch122	rpc2_nhits[2]	
ch123	rpc2_nhits[3]	
ch124	rpc3_nhits[0]	
ch125	rpc3_nhits[1]	
ch126	rpc3_nhits[2]	
ch127	rpc3_nhits[3]	

TMB Board Status Operations

(documentation incomplete 6/9/2004)

ID Registers

id_slot=15	VME Slot
id_rev =D	Firmware version
id_type=C	Firmware Type
id_date=06/08/2004	Firmware Compile Date
id_rev =38C8=06/08/04xc2v3000	Firmware Revcode

Digital Serial Numbers

```
Digital Serial for TMB CRC=DC DSN=00000A237E7F MFG=01 OK
Digital Serial for Mez CRC=BF DSN=000007E06194 MFG=01 OK
Digital Serial for RAT CRC=52 DSN=00000AB39AAD MFG=01 OK
```

Power Supply ADC

```
TMB2004A Comparators
5.0V  status=OK
3.3V  status=OK
1.8V  status=OK
1.5V  status=OK
Tcrit status=OK

TMB2004A ADC
+5.0 TMB      5.004 V     0.305 A
+3.3 TMB      3.221 V     1.160 A
+1.5 TMBcore  1.488 V     0.795 A
+1.5 GTLtt    1.492 V     0.230 A
+1.0 GTLref   1.004 V     0.000 A
+3.3 RAT      3.221 V     0.250 A
+1.8 RATcore  1.797 V     8.985 A
+vref/2       2.047 V     0.000 A
+vzero        0.000 V     0.000 A
+vref         4.095 V     0.000 A

TMB2004A Temperature IC
T tmb pcb    73.4   F    23.    C  Tcrit=261./127.
T tmb fpga   95.0   F    35.    C  Tcrit=261./127.

RAT2004A Temperature IC
T rat pcb    68.0   F    20.    C  Tcrit=261./127.
T rat xstr   69.8   F    21.    C  Tcrit=261./127.
```

Clock Delays

```
Current 3D3444 Delay Settings
     Ch0   8steps  16ns  ALCT  tx clock
     Ch1   1steps   2ns  ALCT  rx clock
     Ch2   2steps   4ns  DMB   tx clock
     Ch3   9steps  20ns  RPC   tx clock
     Ch4   0steps   0ns  TMB1  rx clock
     Ch5   0steps   0ns  MPC   rx clock
     Ch6   0steps   0ns  DCC   tx clock
     Ch7   7steps  14ns  CFEB0 tx clock
     Ch8   7steps  14ns  CFEB1 tx clock
     Ch9   7steps  14ns  CFEB2 tx clock
     ChA   7steps  14ns  CFEB3 tx clock
     ChB   7steps  14ns  CFEB4 tx clock
```

RAT Module Status

```
RAT FPGA device 0 IDcode=20A10093
RAT PROM device 1 IDcode=05034093
RAT FPGA device 0 USERcode=FFFFFFFF
RAT PROM device 1 USERcode=06032004
RAT USER1=E2A78220040603AB
rs_begin      B
rs_version    A
rs_monthday   0603
rs_year       2004
rs_syncmode   0
rs_posneg     1
rs_loop       0
rs_rpc_clk    0
rs_rpc_en     F
rs_txok       0
rs_rxok       0
rs_locked     1
rs_locklost   0
rs_tcrit      1
rs_rpc_free   2
rs_unassigned 00
rs_end        E
```

JTAG Chains

Chain Select Address (X=don't care)

3210	Base	Function
00XX	0	ALCT
01XX	4	TMB Mezzanine FPGA+PROMs
10xx	8	TMB User PROMs
1100	C	FPGA Monitor (for TMB self-test)
1101	D	RAT Module FPGA+PROM

DMB Readout

Full-Readout and Local-Readout Format:

1	6B0C	header	Beginning Of Cathode Data	
3	event	header	Non-buffered event data	
e	clct	header	Cathode LCTs	
e	tmb	header	TMB match result	
e	mpc	header	MPC frames	
e	buf	header	Buffer status	
e	rpc	header	RPC status	
e	6E0B	header	End of header block	
n	hits		CFEB0 raw hits	
n	hits		CFEB1 raw hits	
n	hits		CFEB2 raw hits	
n	hits		CFEB3 raw hits	
n	hits		CFEB4 raw hits	
1	6B04		Start of RPC raw hits marker	(optional)
m	hits		RPC0 raw hits	(optional)
m	hits		RPC1 raw hits	(optional)
m	hits		RPC2 raw hits	(optional)
m	hits		RPC3 raw hits	(optional)
1	6E04		End of RPC raw hits marker	(optional)
1	6E0C		End of raw hits	
1	2AAA		Make word count x4	(inserted only if needed)
1	5555		Make word count x4	(inserted only if needed)
1	crc0		CRC22[10:0]	
1	crc1		CRC22[21:11]	
1	E0F		End of Frame	
1	wordcount		Total words in transmission	(inclusive)

Word Count = 26(nheaders)
+ 1(E0B)
+ ncfebs*(6*ntbins)
+1(B04) (if RPC readout enabled)
+ nrpcs*(2*ntbins) (if RPC readout enabled)
+1(E04) (if RPC readout enabled)
+1(EOC)
+2(2AAA 5555) (if needed to make word count multiple of 4)
+2(crc)
+1(E0F)
+1(wordcount)

Long Header-only Format:

1	6B0C	header	Beginning Of Cathode Data
3	event	header	Non-buffered event data
e	clct	header	Cathode LCTs
e	tmb	header	TMB match result
e	mpc	header	MPC frames
e	buf	header	Buffer status
e	rpc	header	RPC status
1	6E0B		End of header block
1	6E0C		End of raw hits
1	crc0		CRC22
1	crc1		CRC22
1	E0F		End of Frame
1	wordcount		Total words in transmission (inclusive)

32 words = nheaders(26)+E0B+E0C+2crc+E0F+wdcnt

Short Header-only Format:

1	6B0C	header	Beginning Of Cathode Data
3	event	header	Non-buffered event data
1	crc0		CRC22
1	crc1		CRC22
1	EEF		End of Frame
1	frame wordcount		Total words in transmission (inclusive)

8 words = 4headers+2crc+EEF+wdcnt

Header Word Descriptions:

(documentation incomplete 6/9/2004)

```
header00_[11:0]  =      12'hB0C;                // Begining of Cathode record marker
header00_[14:12]=       3'b110;                 // Marker 6

header01_[4:0]   =      r_fifo_tbins[4:0];      // Number of time bins per CFEB in dump
header01_[11:5]  =      {2'h0,r_febs_read[4:0]}; // CFEBs read out for this event, 2 dummy for ALCT
header01_[14:12]=       fifo_mode[2:0];         // Trigger type and fifo mode

header02_[3:0]   =      pop_l1a_rx_counter[3:0]; // Level 1 accepts received and pushed on L1A stack
header02_[7:4]   =      csc_id[3:0];            // Chamber ID number = (slot/2 or slot/2-1 if slot>12 at pup)
header02_[12:8]  =      board_id[4:0];          // TMB2001 module ID number (= VME slot at power up)
header02_[14:13]=       l1a_type[1:0];          // L1A Pop type code: buffers, no buffers, clct/alct_only

header03_[11:0]  =      pop_bxn_counter[11:0];  // Bxn pushed on L1A stack at L1A arrival
header03_[13:12]=       r_type[1:0];            // Record type: dump,nodump, full header, short header
header03_[14]    =      0;                      // Free

header04_[4:0]   =      r_nheaders[4:0];        // Number of header words
header04_[7:5]   =      r_ncfebs[2:0];          // Number of CFEBs read out
header04_[8]     =      r_has_buf;              // Event has buffer data
header04_[13:9]  =      fifo_pretrig[4:0];      // # Time bins before pretrigger;
header04_[14]    =      0;                      // Free

header05_[3:0]   =      r_l1a_tx_counter[3:0];  // Level 1 accept event number at pretrig or alct_only
header05_[11:4]  =      r_trig_source_vec[7:0]; // Trigger source vector
header05_[12]    =      r_trig_source_hsds;     // Trigger was hs or ds
header05_[14:13]=       0;                      // Free

header06_[4:0]   =      r_active_feb_ff[4:0];   // Active CFEB list sent to DMB
header06_[9:5]   =      cfeb_exists[4:0];       // List of instantiated CFEBs
header06_[13:10]=       run_id[3:0];            // Run info
header06_[14]    =      0;                      // Free

header07_[11:0]  =      r_bxn_counter_ff[11:0]; // Full Bunch Crossing number at pretrig
header07_[12]    =      r_sync_err;             // BXN sync error
header07_[14:13]=       0;                      // Free

header08_[14:0]  =      r_clct0_tmb[14:0];      // CLCT0 after drift lsbs
header09_[14:0]  =      r_clct1_tmb[14:0];      // CLCT1 after drift lsbs

header10_[5:0]   =      r_clct0_tmb[20:15];     // CLCT0 after drift msbs
header10_[11:6]  =      r_clct1_tmb[20:15];     // CLCT1 after drift msbs
header10_[12]    =      r_clct_invp;            // CLCT0 had invalid pattern after drift delay
header10_[14:13]=       0;                      // Free

header11_[0]     =      r_tmb_match;            // ALCT and CLCT matched in time
header11_[1]     =      r_tmb_alct_only;        // Only ALCT triggered
header11_[2]     =      r_tmb_clct_only;        // Only CLCT triggered
header11_[4:3]   =      r_tmb_bxn0_diff[1:0];   // BXN difference for matched LCTs alct-clct
header11_[6:5]   =      r_tmb_bxn1_diff[1:0];   // BXN difference for matched LCTs alct-clct
header11_[10:7]  =      r_tmb_match_win[3:0];   // Location of alct in clct match window
header11_[14:11]=       triad_persist[3:0];     // CLCT Triad persistence

header12_[14:0]  =      r_mpc0_frame0_ff[14:0]; // MPC muon 0 frame 0 LSBs
header13_[14:0]  =      r_mpc0_frame1_ff[14:0]; // MPC muon 0 frame 1 LSBs
header14_[14:0]  =      r_mpc1_frame0_ff[14:0]; // MPC muon 1 frame 0 LSBs
header15_[14:0]  =      r_mpc1_frame1_ff[14:0]; // MPC muon 1 frame 1 LSBs
```

```
header16_[0]     =      r_mpc0_frame0_ff[15];          // MPC muon 0 frame 0 MSB
header16_[1]     =      r_mpc0_frame1_ff[15];          // MPC muon 0 frame 1 MSB
header16_[2]     =      r_mpc1_frame0_ff[15];          // MPC muon 1 frame 0 MSB
header16_[3]     =      r_mpc1_frame1_ff[15];          // MPC muon 1 frame 1 MSB
header16_[5:4]   =      r_mpc_accept[1:0];             // MPC muon accept response
header16_[7:6]   =      r_mpc_reserved[1:0];           // MPC reserved
header16_[10:8]  =      hs_thresh[2:0];                // 1/2-strip pretrigger threshold
header16_[13:11]=       ds_thresh[2:0];                // DiStrip   pretrigger threshold
header16_[14]    =      0;                             // Free

header17_[0]     =      r_wr_buf_ready_ff;             // Write buffer is ready
header17_[5:1]   =      r_wr_tbin_adr_ff[4:0];         // Tbin address at pretrig
header17_[8:6]   =      r_wr_buf_adr_ff[2:0];          // Address of write buffer at pretrig
header17_[9]     =      r_buf_ovf;                     // Pretrig arrived when no buffer was free
header17_[10]    =      r_buf_full;                    // All 8 buffers in use
header17_[11]    =      r_buf_almost_full;             // Almost all buffers in use
header17_[12]    =      r_buf_half_full;               // Half of buffers in use
header17_[13]    =      r_buf_empty;                   // No buffers in use
header17_[14]    =      0;                             // Free

header18_[3:0]   =      r_buf_nbusy[MXBUFB:0];         // Number of buffers busy
header18_[11:4]  =      r_buf_busy[MXBUF-1:0];         // List of busy buffers
header18_[12]    =      pop_free[0:0];                 // Unassigned
header18_[13]    =      stack_ovf_latch;               // L1A stack overflow
header18_[14]    =      0;                             // Free

header19_[0]     =      pop_tmb_trig_pulse;            // TMB response
header19_[1]     =      pop_tmb_alct_only;             // Only ALCT triggered
header19_[2]     =      pop_tmb_clct_only;             // Only CLCT triggered
header19_[3]     =      pop_tmb_match;                 // ALCT*CLCT triggered
header19_[4]     =      pop_wr_buf_ready;              // Write buffer ready at pretrig
header19_[5]     =      pop_wr_buf_avail;              // Write buffer ready or not required at pretrig
header19_[10:6]  =      pop_wr_tbin_adr[4:0];          // Tbin address at pretrig
header19_[13:11]=       pop_wr_buf_adr[2:0];           // Address of write buffer at pretrig
header19_[14]    =      0;                             // Free

header20_[3:0]   =      r_discard_nowbuf_cnt[3:0];     // pretrig but no wbuf available
header20_[7:4]   =      r_discard_invp_cnt[3:0];       // invalid pattern after drift
header20_[11:8]  =      r_discard_tmbreject_cnt[3:0];  // tmb rejected event
header20_[12]    =      r_no_tmb_trig_pulse;           // no tmb_trig_pulse  before timeout
header20_[13]    =      r_no_mpc_frame_ff;             // no mpc_frame_ff    before timeout
header20_[14]    =      r_no_mpc_response_ff;          // no mpc_response_ff before timeout

header21_[3:0]   =      rpc_exists[3:0];               // RPCs connected to this TMB
header21_[7:4]   =      rd_rpc_list[3:0];              // RPC units included in read out
header21_[10:8]  =      rd_nrpcs[2:0];                 // Number of RPCs in readout
header21_[11]    =      rpc_read_enable;               // RPC readout enabled
header21_[14:12]=       0;                             // Free

header22_[14:0]  =      8'h22;                         // Free
header23_[14:0]  =      8'h23;                         // Free
header24_[14:0]  =      8'h24;                         // Free

header25_[13:0]  =      revcode[13:0];                 // Firmware version date code
header25_[14]    =      0;                             // Free
```

Revcode

```
-----------------------------------------------------
`define FIRMWARE_TYPE       04'hC          // C=Normal CLCT/TMB, D=Debug PCB loopback version
`define VERSION             04'hD          // Version ID
`define MONTHDAY            16'h0608       // Version date
`define YEAR                16'h2004       // Version date
`define FPGAID              16'h3000       // FPGA Type XC2Vnnnn

assign revcode_vme[8:0]    = (monthday[15:12]*10 + monthday[11:8])*32+ (monthday[7:4]*10 + monthday[ 3:0]);
assign revcode_vme[11:9]   = year[2:0];
assign revcode_vme[13:12] = fpgaid[15:12];
```

Decoding Revcode:

```
      adr = base_adr+6
      status = vme_read(%ref(adr),%ref(rd_data))
      id_rev                  = rd_data
      id_rev_day        = ishft(id_rev , 0).and.'001F'x
      id_rev_month      = ishft(id_rev, -5).and.'000F'x
      id_rev_year       = ishft(id_rev, -9).and.'0007'x
      id_rev_fpga       = ishft(id_rev,-12).and.'000F'x
```

DMB FIFO Data Format: Short-Header Mode

Frame #	/wr	first	last	15 ddu	14 d14	13 d13	12 d12	11 d11	10 d10	9 d9	8 d8	7 d7	6 d6	5 d5	4 d4	3 d3	2 d2	1 d1	0 d0
	FIFO Control			DDU	TMB Data														
No Write	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	1	0	0	1	1	0	$B0C_{16}$											
1	0	0	0	0	FIFO Mode			CFEBs in Readout							Tbins per CFEB				
2	0	0	0	0	l1a_type			Board ID				CSC ID			L1A Rx Number				
3	0	0	0	0	Res	r_type		BXN Counter at L1A arrival											
4	0	0	0	1	DDU Code 101_2			1 TMB	CRC22[10:0]										
5	0	0	0	1	DDU Code 101_2			1 TMB	CRC22[21:11]										
6	0	0	0	1	DDU Code 101_2			EEF_{16}											
7	0	0	1	1	DDU Code 101_2			1 TMB	Word Count [10:0]										
No Write	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Record Type Codes:

r-type	Raw Hits	Header	
0	No	Full	
1	Full	Full	
2	Local	Full	
3	No	Short	(No buffer was available at pre-trigger)

L1A Type Codes:

l1a-type		
0	Normal CLCT trigger with buffer data and L1A window match	
1	ALCT-only trigger, no data buffers	(not usually read out)
2	L1A-only, no matching TMB trigger, no buffer data	(not usually read out)
3	TMB triggered, no L1A-window match, event has buffer data	(not usually read out)

FIFO Modes:

mode	Raw Hits	Header	
0	No	Full	(If buffer was available at pre-trigger)
1	All 5 CFEBs	Full	(If buffer was available at pre-trigger)
2	Local	Full	(If buffer was available at pre-trigger)
3	No	Short	
4	No	No	

DMB FIFO Data Format: Long Header-Only Mode

Frame #	/wr	first	last	15 ddu	14 d14	13 d13	12 d12	11 d11	10 d10	9 d9	8 d8	7 d7	6 d6	5 d5	4 d4	3 d3	2 d2	1 d1	0 d0
	FIFO Control			DDU	TMB Data														
No Write	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	1	0	0	1	1	0	$B0C_{16}$											
1	0	0	0	0	FIFO Mode			CFEBs in Readout							Tbins per CFEB				
2	0	0	0	0	l1a_type			Board ID				CSC ID			L1A Rx Counter				
3	0	0	0	0	Res	r_type		BXN Counter at L1A arrival											
4	0	0	0	0	Res	# Tbins before pre-trig					has buf	# CFEBs			# Header frames				
5	0	0	0	0	Reserved		hs pretg	Trigger Source Vector							L1A Tx Counter				
6	0	0	0	0	Res	Run ID				CFEBs Instantiated					Active CFEBs				
7	0	0	0	0	Reserved		Sync Err	BXN Counter at Pre-trigger											
8	0	0	0	0	Cathode LCT0[14:0] (lsb)														
9	0	0	0	0	Cathode LCT1[14:0] (lsb)														
10	0	0	0	0	Reserved		Invalid Pattern	Cathode LCT1[20:15]						Cathode LCT0[20:15]					
11	0	0	0	0	Triad Persistence[3:0]			ALCT Match Time				LCT1 BXN Difference		LCT0 BXN Difference		CLCT Only	ALCT Only	TMB Match	
12	0	0	0	0	MPC Muon0 Frame0[14:0] (lsb)														
13	0	0	0	0	MPC Muon0 Frame1[14:0] (lsb)														
14	0	0	0	0	MPC Muon1 Frame0[14:0] (lsb)														
15	0	0	0	0	MPC Muon1 Frame1[14:0] (lsb)														
16	0	0	0	0	Res	ds_thresh[2:0]			hs_thresh[2:0]			mpc reserved		mpc accept[1:0]		Muon1 Fram1 [15]	Muon1 Frame0 [15]	Muon0 Fram1 [15]	Muon0 Frame0 [15]
17	0	0	0	0	Res	Buf empty	Buf ½ful	Buf full-1	Buf full	Buf ovf	Write Buf Adr				Tbin Address at pretrig				Buf ready
18	0	0	0	0	Reserved		Pop free	Busy Buffer List							# Buffers Busy				
19	0	0	0	0	Res	POP Buf Adr			POP Tbin Adr					POP Buf Avai	POP Buf Ready	POP TMB Match	POP CLCT Only	POP ALCT Only	POP TMB Trig
20	0	0	0	0	TMB Mpc rx timeout	TMB Mpc tx timeout	TMB Trig timout	Discard: TMB Reject				Discard: Invalid Pattern			Discard: No buffer avail				
21	0	0	0	0	Reserved			rpc read en	#RPCs			RPC Readout[3:0]			RPC Exits[3:0]				
22	0	0	0	0	22_{16} (future RPC/TMB matching info)														
23	0	0	0	0	23_{16} (future RPC/TMB matching info)														
24	0	0	0	0	24_{16} (future RPC/TMB matching info)														
25	0	0	0	0	Res	Firmware Revcode													
26	0	1	0	0	1	1	0	$E0B_{16}$											
27	0	0	0	0	1	1	0	$E0C_{16}$											
28	0	0	0	1	DDU Code 101_2			1 TMB	CRC22[10:0]										
29	0	0	0	1	DDU Code 101_2			1 TMB	CRC22[21:11]										
30	0	0	0	1	DDU Code 101_2			$E0F_{16}$											
31	0	0	1	1	DDU Code 101_2			1 TMB	Word Count [10:0]										
No Write	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

DMB FIFO Data Format: Full-Readout Mode

Frame #	/wr	first	last	15 ddu	14 d14	13 d13	12 d12	11 d11	10 d10	9 d9	8 d8	7 d7	6 d6	5 d5	4 d4	3 d3	2 d2	1 d1	0 d0
	FIFO Control			DDU	TMB Data														
No Write	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	0	1	0	0	1	1	0	$B0C_{16}$ Begin Cathode Header											
1	0	0	0	0	FIFO Mode			CFEBs in Readout							Tbins per CFEB				
2	0	0	0	0	l1a_type			Board ID				CSC ID				L1A Rx Counter			
3	0	0	0	0	Res	r_type		BXN Counter at L1A arrival											
4	0	0	0	0	Res	# Tbins before pre-trig					has buf	# CFEBs			# Header frames				
5	0	0	0	0	Reserved			Trigger Source Vector								L1A Tx Counter			
6	0	0	0	0	Res	Run ID				CFEBs Instantiated					Active CFEBs				
7	0	0	0	0	Reserved		Sync Err	BXN Counter at Pre-trigger											
8	0	0	0	0	Cathode LCT0[14:0] (lsb)														
9	0	0	0	0	Cathode LCT1[14:0] (lsb)														
10	0	0	0	0	Reserved		Invalid Pattern	Cathode LCT1[20:15]							Cathode LCT0[20:15]				
11	0	0	0	0	Reserved				ALCT Match Time			LCT1 BXN Difference		LCT0 BXN Difference			CLCT Only	ALCT Only	TMB Match
12	0	0	0	0	MPC Muon0 Frame0[14:0] (lsb)														
13	0	0	0	0	MPC Muon0 Frame1[14:0] (lsb)														
14	0	0	0	0	MPC Muon1 Frame0[14:0] (lsb)														
15	0	0	0	0	MPC Muon1 Frame1[14:0] (lsb)														
16	0	0	0	0	Reserved							mpc reserved		mpc accept[1:0]		Muon1 Fram1 [15]	Muon1 Frame0 [15]	Muon0 Fram1 [15]	Muon0 Frame0 [15]
17	0	0	0	0	Res	Buf empty	Buf ½ful	Buf full-1	Buf full	Buf ovf	Write Buf Adr			Tbin Address at pretrig					Buf ready
18	0	0	0	0	Reserved		Pop free	Busy Buffer List								# Buffers Busy			
19	0	0	0	0	Res	POP Buf Adr			POP Tbin Adr					POP Buf Avai	POP Buf Ready	POP TMB Match	POP CLCT Only	POP ALCT Only	POP TMB Trig
20	0	0	0	0	TMB Mpc rx timeout	TMB Mpc tx timeout	TMB Trig timout	Discard: TMB Reject				Discard: Invalid Pattern				Discard: No buffer avail			
21	0	0	0	0	Reserved			rpc read en	#RPCs			RPC Readout[3:0]				RPC Exits[3:0]			
22	0	0	0	0	22_{16} (future RPC/TMB matching info)														
23	0	0	0	0	23_{16} (future RPC/TMB matching info)														
24	0	0	0	0	24_{16} (future RPC/TMB matching info)														
25	0	0	0	0	Res	Firmware Revcode													
26	0	1	0	0	1	1	0	$E0B_{16}$ End Header Block											
27	0	0	0	0	CFEB 0			Tbin 0				Ly0[7:0] Triad bits							
28	0	0	0	0	CFEB 0			Tbin 0				Ly1[7:0]							
29	0	0	0	0	CFEB 0			Tbin 0				Ly2[7:0]							
30	0	0	0	0	CFEB 0			Tbin 0				Ly3[7:0]							
31	0	0	0	0	CFEB 0			Tbin 0				Ly4[7:0]							
32	0	0	0	0	CFEB 0			Tbin 0				Ly5[7:0]							
33	0	0	0	0	CFEB 0			Tbin 1				Ly0[7:0]							
34	0	0	0	0	CFEB 0			Tbin 1				Ly1[7:0]							
35	0	0	0	0	CFEB 0			Tbin 1				Ly2[7:0]							
36	0	0	0	0	CFEB 0			Tbin 1				Ly3[7:0]							
37	0	0	0	0	CFEB 0			Tbin 1				Ly4[7:0]							
38	0	0	0	0	CFEB 0			Tbin 1				Ly5[7:0]							
-	-	-	-	-	-			-				-							

231	0	0	0	0	CFEB 4			Tbin 6				Ly0[7:0]								
232	0	0	0	0	CFEB 4			Tbin 6				Ly1[7:0]								
233	0	0	0	0	CFEB 4			Tbin 6				Ly2[7:0]								
234	0	0	0	0	CFEB 4			Tbin 6				Ly3[7:0]								
235	0	0	0	0	CFEB 4			Tbin 6				Ly4[7:0]								
236	0	0	0	0	CFEB 4			Tbin 6				Ly5[7:0]								
237	0	0	0	0	1	1	0	$B04_{16}$ Begin RPC Raw Hits (if RPC readout enabled)												
238	0	0	0	0	RPC 0			Tbin 0				Pads[7:0] RPC Pads								
239	0	0	0	0	RPC 0				RPC BXN			Pads[15:8]								
240	0	0	0	0	RPC 0			Tbin 1				Pads[7:0]								
241	0	0	0	0	RPC 0				RPC BXN			Pads[15:8]								
242	0	0	0	0	RPC 0			Tbin 2				Pads[7:0]								
243	0	0	0	0	RPC 0				RPC BXN			Pads[15:8]								
244	0	0	0	0	RPC 0			Tbin 3				Pads[7:0]								
245	0	0	0	0	RPC 0				RPC BXN			Pads[15:8]								
246	0	0	0	0	RPC 0			Tbin 4				Pads[7:0]								
247	0	0	0	0	RPC 0				RPC BXN			Pads[15:8]								
248	0	0	0	0	RPC 0			Tbin 5				Pads[7:0]								
249	0	0	0	0	RPC 0				RPC BXN			Pads[15:8]								
250	0	0	0	0	RPC 0			Tbin 6				Pads[7:0]								
251	0	0	0	0	RPC 0				RPC BXN			Pads[15:8]								
-	-	-	-	-	-			-	-			-								
292	0	0	0	0	RPC 3			Tbin 6				Pads[7:0]								
293	0	0	0	0	RPC 3				RPC BXN			Pads[15:8]								
294	0	0	0	0	1	1	0	$E04_{16}$ End RPC Raw Hits												
295	0	0	0	0	1	1	0	$E0C_{16}$ End Cathode Data												
opt	0	0	0	0	0			$2AAA_{16}$ (Optional to make word count multiple of 4)												
opt	0	0	0	0	0			5555_{16} (Optional to make word count multiple of 4)												
296	0	0	0	1	DDU Code 101_2			1 TMB	CRC22[10:0]											
297	0	0	0	1	DDU Code 101_2			1 TMB	CRC22[21:11]											
298	0	0	0	1	DDU Code 101_2			$E0F_{16}$ End TMB Readout												
299	0	0	1	1	DDU Code 101_2			1 TMB	Word Count [10:0]											
No Write	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Sample TMB Raw Hits Dump:

TMB internal pattern injector + RPC internal pattern injector
7-Time bins, full raw hits readout

```
Adr=   0 Data=06B0C      Adr=  75 Data=01100      Adr= 150 Data=02600      Adr= 225 Data=04500
Adr=   1 Data=013E7      Adr=  76 Data=01100      Adr= 151 Data=02600      Adr= 226 Data=04500
Adr=   2 Data=01592      Adr=  77 Data=01100      Adr= 152 Data=02600      Adr= 227 Data=04500
Adr=   3 Data=01CFA      Adr=  78 Data=01100      Adr= 153 Data=03000      Adr= 228 Data=04500
Adr=   4 Data=005BA      Adr=  79 Data=01100      Adr= 154 Data=03000      Adr= 229 Data=04500
Adr=   5 Data=01011      Adr=  80 Data=01100      Adr= 155 Data=03000      Adr= 230 Data=04500
Adr=   6 Data=003FF      Adr=  81 Data=01242      Adr= 156 Data=03000      Adr= 231 Data=04600
Adr=   7 Data=01C7D      Adr=  82 Data=01242      Adr= 157 Data=03000      Adr= 232 Data=04600
Adr=   8 Data=00BFD      Adr=  83 Data=01242      Adr= 158 Data=03000      Adr= 233 Data=04600
Adr=   9 Data=04BFD      Adr=  84 Data=01242      Adr= 159 Data=03100      Adr= 234 Data=04600
Adr=  10 Data=00514      Adr=  85 Data=01242      Adr= 160 Data=03100      Adr= 235 Data=04600
Adr=  11 Data=02881      Adr=  86 Data=01242      Adr= 161 Data=03100      Adr= 236 Data=04600
Adr=  12 Data=07F87      Adr=  87 Data=01300      Adr= 162 Data=03100      Adr= 237 Data=06B04
Adr=  13 Data=01705      Adr=  88 Data=01340      Adr= 163 Data=03100      Adr= 238 Data=00000
Adr=  14 Data=077BD      Adr=  89 Data=01300      Adr= 164 Data=03100      Adr= 239 Data=00000
Adr=  15 Data=01725      Adr=  90 Data=01340      Adr= 165 Data=03242      Adr= 240 Data=00100
Adr=  16 Data=0240F      Adr=  91 Data=01300      Adr= 166 Data=03242      Adr= 241 Data=00000
Adr=  17 Data=00021      Adr=  92 Data=01340      Adr= 167 Data=03242      Adr= 242 Data=002CD
Adr=  18 Data=00011      Adr=  93 Data=01440      Adr= 168 Data=03242      Adr= 243 Data=005AB
Adr=  19 Data=00439      Adr=  94 Data=01402      Adr= 169 Data=03242      Adr= 244 Data=00301
Adr=  20 Data=00000      Adr=  95 Data=01440      Adr= 170 Data=03242      Adr= 245 Data=00100
Adr=  21 Data=00CFF      Adr=  96 Data=01402      Adr= 171 Data=03300      Adr= 246 Data=00402
Adr=  22 Data=00022      Adr=  97 Data=01440      Adr= 172 Data=03340      Adr= 247 Data=00200
Adr=  23 Data=00023      Adr=  98 Data=01402      Adr= 173 Data=03300      Adr= 248 Data=00503
Adr=  24 Data=00024      Adr=  99 Data=01500      Adr= 174 Data=03340      Adr= 249 Data=00300
Adr=  25 Data=038C8      Adr= 100 Data=01500      Adr= 175 Data=03300      Adr= 250 Data=00604
Adr=  26 Data=06E0B      Adr= 101 Data=01500      Adr= 176 Data=03340      Adr= 251 Data=00400
Adr=  27 Data=00000      Adr= 102 Data=01500      Adr= 177 Data=03440      Adr= 252 Data=01000
Adr=  28 Data=00000      Adr= 103 Data=01500      Adr= 178 Data=03402      Adr= 253 Data=01000
Adr=  29 Data=00000      Adr= 104 Data=01500      Adr= 179 Data=03440      Adr= 254 Data=01100
Adr=  30 Data=00000      Adr= 105 Data=01600      Adr= 180 Data=03402      Adr= 255 Data=01000
Adr=  31 Data=00000      Adr= 106 Data=01600      Adr= 181 Data=03440      Adr= 256 Data=012AB
Adr=  32 Data=00000      Adr= 107 Data=01600      Adr= 182 Data=03402      Adr= 257 Data=014EF
Adr=  33 Data=00100      Adr= 108 Data=01600      Adr= 183 Data=03500      Adr= 258 Data=01301
Adr=  34 Data=00100      Adr= 109 Data=01600      Adr= 184 Data=03500      Adr= 259 Data=01200
Adr=  35 Data=00100      Adr= 110 Data=01600      Adr= 185 Data=03500      Adr= 260 Data=01402
Adr=  36 Data=00100      Adr= 111 Data=02000      Adr= 186 Data=03500      Adr= 261 Data=01200
Adr=  37 Data=00100      Adr= 112 Data=02000      Adr= 187 Data=03500      Adr= 262 Data=01503
Adr=  38 Data=00100      Adr= 113 Data=02000      Adr= 188 Data=03500      Adr= 263 Data=01200
Adr=  39 Data=00242      Adr= 114 Data=02000      Adr= 189 Data=03600      Adr= 264 Data=01604
Adr=  40 Data=00242      Adr= 115 Data=02000      Adr= 190 Data=03600      Adr= 265 Data=01200
Adr=  41 Data=00242      Adr= 116 Data=02000      Adr= 191 Data=03600      Adr= 266 Data=02000
Adr=  42 Data=00242      Adr= 117 Data=02100      Adr= 192 Data=03600      Adr= 267 Data=02000
Adr=  43 Data=00242      Adr= 118 Data=02100      Adr= 193 Data=03600      Adr= 268 Data=02100
Adr=  44 Data=00242      Adr= 119 Data=02100      Adr= 194 Data=03600      Adr= 269 Data=02000
Adr=  45 Data=00300      Adr= 120 Data=02100      Adr= 195 Data=04000      Adr= 270 Data=022EF
Adr=  46 Data=00340      Adr= 121 Data=02100      Adr= 196 Data=04000      Adr= 271 Data=023CD
Adr=  47 Data=00300      Adr= 122 Data=02100      Adr= 197 Data=04000      Adr= 272 Data=02301
Adr=  48 Data=00340      Adr= 123 Data=02242      Adr= 198 Data=04000      Adr= 273 Data=02300
Adr=  49 Data=00300      Adr= 124 Data=02242      Adr= 199 Data=04000      Adr= 274 Data=02402
Adr=  50 Data=00340      Adr= 125 Data=02242      Adr= 200 Data=04000      Adr= 275 Data=02300
Adr=  51 Data=00440      Adr= 126 Data=02242      Adr= 201 Data=04100      Adr= 276 Data=02503
Adr=  52 Data=00402      Adr= 127 Data=02242      Adr= 202 Data=04100      Adr= 277 Data=02300
Adr=  53 Data=00440      Adr= 128 Data=02242      Adr= 203 Data=04100      Adr= 278 Data=02604
Adr=  54 Data=00402      Adr= 129 Data=02300      Adr= 204 Data=04100      Adr= 279 Data=02300
Adr=  55 Data=00440      Adr= 130 Data=02340      Adr= 205 Data=04100      Adr= 280 Data=03000
Adr=  56 Data=00402      Adr= 131 Data=02300      Adr= 206 Data=04100      Adr= 281 Data=03000
Adr=  57 Data=00500      Adr= 132 Data=02340      Adr= 207 Data=04242      Adr= 282 Data=03100
Adr=  58 Data=00500      Adr= 133 Data=02300      Adr= 208 Data=04242      Adr= 283 Data=03000
Adr=  59 Data=00500      Adr= 134 Data=02340      Adr= 209 Data=04242      Adr= 284 Data=03223
Adr=  60 Data=00500      Adr= 135 Data=02440      Adr= 210 Data=04242      Adr= 285 Data=03201
Adr=  61 Data=00500      Adr= 136 Data=02402      Adr= 211 Data=04242      Adr= 286 Data=03301
Adr=  62 Data=00500      Adr= 137 Data=02440      Adr= 212 Data=04242      Adr= 287 Data=03400
Adr=  63 Data=00600      Adr= 138 Data=02402      Adr= 213 Data=04300      Adr= 288 Data=03402
Adr=  64 Data=00600      Adr= 139 Data=02440      Adr= 214 Data=04340      Adr= 289 Data=03400
Adr=  65 Data=00600      Adr= 140 Data=02402      Adr= 215 Data=04300      Adr= 290 Data=03503
Adr=  66 Data=00600      Adr= 141 Data=02500      Adr= 216 Data=04340      Adr= 291 Data=03400
Adr=  67 Data=00600      Adr= 142 Data=02500      Adr= 217 Data=04300      Adr= 292 Data=03604
Adr=  68 Data=00600      Adr= 143 Data=02500      Adr= 218 Data=04340      Adr= 293 Data=03400
Adr=  69 Data=01000      Adr= 144 Data=02500      Adr= 219 Data=04440      Adr= 294 Data=06E04
Adr=  70 Data=01000      Adr= 145 Data=02500      Adr= 220 Data=04402      Adr= 295 Data=06E0C
Adr=  71 Data=01000      Adr= 146 Data=02500      Adr= 221 Data=04440      Adr= 296 Data=0DB37
Adr=  72 Data=01000      Adr= 147 Data=02600      Adr= 222 Data=04402      Adr= 297 Data=0DAE7
Adr=  73 Data=01000      Adr= 148 Data=02600      Adr= 223 Data=04440      Adr= 298 Data=0DE0F
Adr=  74 Data=01000      Adr= 149 Data=02600      Adr= 224 Data=04402      Adr= 299 Data=0D92C
```

TMB Signal Summary

CCB

1 Input LVDS 40MHz clock
46 Inputs GTLP at 40MHz
46 Outputs GTLP at 40MHz

Table 1: CCB Signal Summary

Signal	Bits	Dir	Logic	Function
Clock Bus				
ccb_clock40	1	In	LVDS	
Total	1			
Fast Control Bus				
ccb_clock40_enable	1	In	GTLP	
ccb_cmd[5..0]	6	In	GTLP	
ccb_evcntres	1	In	GTLP	
ccb_bcntres	1	In	GTLP	
ccb_cmd_strobe	1	In	GTLP	
ccb_bx0	1	In	GTLP	
ccb_l1accept	1	In	GTLP	
ccb_data[7..0]	8	In	GTLP	
ccb_data_strobe	1	In	GTLP	
ccb_reserved[4..0]	5	In	GTLP	
Total	26			
TMB Reload Bus: ALCT+CLCT+TMB FPGA Reload				
tmb_hard_reset	1	In	GTLP	
tmb_cfg_done[8..0]	9	Out	GTLP	
alct_hard_reset	1	In	GTLP	
alct_cfg_done[8..0]	9	Out	GTLP	
tmb_reserved[1..0]	2	In	GTLP	
Total	22			
DAQ Special Purpose Bus [Used by DMB and TMB]				
dmb_cfeb_calibrate[2..0]	3	In	GTLP	
dmb_l1a_release	1	(In)	GTLP	
dmb_reserved_out[4..0]	5	In	GTLP	
dmb_reserved_in[2..0]	3	(In)	GTLP	
Total	12			
Trigger Special Purpose Bus [Used by TMB only]				
alct_adb_pulse_sync	1	In	GTLP	
alct_adb_pulse_async	1	In	GTLP	
clct_external_trigger	1	In	GTLP	
alct_external_trigger	1	In	GTLP	
clct_status[8..0]	9	Out	GTLP	
alct_status[8..0]	9	Out	GTLP	
tmb_l1a_request	1	Out	GTLP	
tmb_l1a_release	1	Out	GTLP	
tmb_reserved_in[4..0]	5	Out	GTLP	
tmb_reserved_out[2..0]	3	In	GTLP	
Total	32			

ALCT

29 Input s LVDS Multiplexed at 80 MHz
20 Outputs LVDS Multiplexed at 80 MHz
1 Output LVDS 40MHz clock

Table 2: ALCT Signal Summary

Signal	Bits	Pins	Mux	Dir	Logic	Function
first_valid	1	0.5	Yes	In	LVDS	Valid Pattern Flag, best muon
first_quality[1..0]	2	1	Yes	In	LVDS	Pattern Quality, best muon
first_amu	1	0.5	Yes	In	LVDS	Accelerator Muon Flag, best muon
first_key[6..0]	7	3.5	Yes	In	LVDS	Key Wire Group, best muon
second_valid	1	0.5	Yes	In	LVDS	Valid Pattern Flag, 2nd best muon
second_quality[1..0]	2	1	Yes	In	LVDS	Pattern Quality, 2nd best muon
second_amu	1	0.5	Yes	In	LVDS	Accelerator Muon Flag, 2nd best muon
second_key[6..0]	7	3.5	Yes	In	LVDS	Key Wire Group, 2nd best muon
bxn[4..0]	5	2.5	Yes	In	LVDS	Bunch Crossing Number
daq_data[13..0]	14	7	Yes	In	LVDS	DAQ data
/wr_fifo	1	0.5	Yes	In	LVDS	/Write_enable DAQ FIFO
lct_special	1	0.5	Yes	In	LVDS	LCT Special Word Flag
ddu_special	1	0.5	Yes	In	LVDS	DAQ Special Word Flag
first_frame	1	0.5	Yes	In	LVDS	First DAQ Frame
last_frame	1	0.5	Yes	In	LVDS	Last DAQ Frame
seq_status[1..0]	2	1	Yes	In	LVDS	Sequencer Status
seu_status[1..0]	2	1	Yes	In	LVDS	Radiation SEU Status
active_feb_flag	1	0.5	Yes	In	LVDS	Active FEB Flag (ALCT pre-triggered)
cfg_done	1	0.5	Yes	In	LVDS	FPGA configuration done
reserved_out[3..0]	4	2	Yes	In	LVDS	Future use
tdo	1	1	No	In	LVDS	JTAG tdo from ALCT
Total Inputs	57	29				

Signal	Bits	Pins	Mux	Dir	Logic	Function
ccb_brcst[7..0]	8	4	Yes	Out	LVDS	CCB broadcast command
brcst_str	1	0.5	Yes	Out	LVDS	ccb_brcst strobe
dout_str	1	0.5	Yes	Out	LVDS	ccb_dout strobe
subadr_str	1	0.5	Yes	Out	LVDS	ccb_subaddr strobe
bx0	1	0.5	Yes	Out	LVDS	Bunch Crossing Zero
ext_inject	1	0.5	Yes	Out	LVDS	External Test Pattern Inject Command
ext_trig	1	0.5	Yes	Out	LVDS	External Trigger Command
level1_accept	1	0.5	Yes	Out	LVDS	Level 1 Accept
sync_adb_pulse	1	0.5	Yes	Out	LVDS	Synchronous ADB Test Pulse
seq_cmd[2..0]	3	1.5	Yes	Out	LVDS	Sequencer Command
reserved_in[4..0]	5	2.5	Yes	Out	LVDS	Future use
clock	1	1	No	Out	LVDS	40MHz clock
clock_en	1	1	No	Out	LVDS	Clock enable
hard_reset	1	1	No	Out	LVDS	FPGA Reload Command
async_adb_pulse	1	1	No	Out	LVDS	Asynchronous ADB Test Pulse
jtag_select[1..0]	2	2	No	Out	LVDS	JTAG Chain Select
tck	1	1	No	Out	LVDS	JTAG tck to ALCT
tms	1	1	No	Out	LVDS	JTAG tms to ALCT
tdi	1	1	No	Out	LVDS	JTAG tdi to ALCT
Total Outputs	33	21				

DMB

3 Inputs LVTTL at 40 MHz
45 Outputs LVTTL at 40 MHz

Table 3: DMB Signal Summary

Signal	Bits	Dir	Logic	Function
tmb_data[14:0]	15	Out	LVTTL	TMB data[14:0] to DMB FIFO
alct_data[14:0]	15	Out	LVTTL	ALCT data [14:0] to DMB FIFO
tmb_ddu_special	1	Out	LVTTL	TMB DDU Special Word Flag
tmb_last_frame	1	Out	LVTTL	TMB Last FIFO frame
tmb_data_available	1	Out	LVTTL	TMB Data Available
/tmb_write_enable_fifo	1	Out	LVTTL	TMB FIFO /write_enable
tmb_active_feb_flag	1	Out	LVTTL	TMB Active Front-End-Board Flag
tmb_active_feb[4…0]	5	Out	LVTTL	TMB Active FEB indicators[4..0]
fifo_clock	1	Out	LVTTL	40MHz FIFO storage clock [= tmb_clock]
alct_ddu_special	1	Out	LVTTL	ALCT DDU Special Word Flag
alct_last_frame	1	Out	LVTTL	ALCT Last FIFO frame
alct_first_frame(dav)	1	Out	LVTTL	ALCT First FIFO frame, data available
/alct_write_enable_fifo	1	Out	LVTTL	ALCT FIFO /write_enable
reserved_to_dmb	5	Out	LVTTL	Unassigned
Total Outputs	50			

dmb_request_lct	1	In	LVTTL	DMB requests active_feb_flag from TMB
dmb_ext_trig	1	In	LVTTL	DMB external trigger to TMB
dmb_fpga_pgm_done	1	In	LVTTL	DMB FPGA Program Done
reserved_from_dmb	3	In	LVTTL	Unassigned
Total Inputs	6			

CFEB

120 Inputs LVDS data multiplexed at 80 MHz
5 Outputs LVDS 40MHz clock

Table 4: CFEB Signal Summary

Signal	Bits	Pins	Dir	Logic	Function
cfeb0_ly[5..0]_tr[7..0]	48	24	In	LVDS	CFEB0 6 layers x 8 triads, 80MHz
cfeb1_ly[5..0]_tr[7..0]	48	24	In	LVDS	CFEB1 6 layers x 8 triads, 80MHz
cfeb2_ly[5..0]_tr[7..0]	48	24	In	LVDS	CFEB2 6 layers x 8 triads, 80MHz
cfeb3_ly[5..0]_tr[7..0]	48	24	In	LVDS	CFEB3 6 layers x 8 triads, 80MHz
cfeb4_ly[5..0]_tr[7..0]	48	24	In	LVDS	CFEB4 6 layers x 8 triads, 80MHz
Total Inputs	240	120			

Signal	Bits	Pins	Dir	Logic	Function
cfeb0_lct_clock	1	1	Out	LVDS	CFEB 1 40MHz clock
cfeb1_lct_clock	1	1	Out	LVDS	CFEB 2 40MHz clock
cfeb2_lct_clock	1	1	Out	LVDS	CFEB 3 40MHz clock
cfeb3_lct_clock	1	1	Out	LVDS	CFEB 4 40MHz clock
cfeb4_lct_clock	1	1	Out	LVDS	CFEB 5 40MHz clock
Total Outputs	5	5			

MPC

1 Input GTLP at 80MHz
32 Outputs GTLP at 80MHz

Table 5: MPC Signal Summary

	Signal	Bits	Pins	Dir	Logic	Function
First In Time	alct_first_key[6:0]	7	3.5	Out	GTLP	LCT 0 ALCT key wire-group
	clct_first_pat[2:0]	3	1.5	Out	GTLP	LCT 0 CLCT pattern number
	clct_first_hsds	1	0.5	Out	GTLP	LCT 0 CLCT ½-Strip flag
	lct_first_quality[3:0]	4	2	Out	GTLP	LCT 0 Muon quality
	first_vpf	1	0.5	Out	GTLP	LCT 0 Valid pattern flag
	alct_second_key[6:0]	7	3.5	Out	GTLP	LCT 1 ALCT key wire-group
	clct_second_pat[2:0]	3	1.5	Out	GTLP	LCT 1 CLCT pattern number
	clct_second_hsds	1	0.5	Out	GTLP	LCT 1 CLCT ½-Strip flag
	lct_second_quality[3:0]	4	2	Out	GTLP	LCT 1 Muon quality
	second_vpf	1	0.5	Out	GTLP	LCT 1 Valid pattern flag
Second In Time	clct_first_key[7:0]	8	4	Out	GTLP	LCT 0 CLCT key ½-strip
	clct_first_bend	1	0.5	Out	GTLP	LCT 0 CLCT bend direction
	lct 0 sync_err	1	0.5	Out	GTLP	LCT 0 BXN does not match at BX0
	alct_first_bxn[0]	1	0.5	Out	GTLP	LCT 0 ALCT bunch crossing number
	clct_first_bx0_local	1	0.5	Out	GTLP	LCT 0 local BXN from CLCT
	csc_id[3:0]	4	2	Out	GTLP	CSC chamber ID
	clct_second_key[7:0]	8	4	Out	GTLP	LCT 1 CLCT key ½-strip
	clct_second_bend	1	0.5	Out	GTLP	LCT 1 CLCT bend direction
	lct 1 sync_err	1	0.5	Out	GTLP	LCT 1 BXN does not match at BX0
	alct_second_bxn[0]	1	0.5	Out	GTLP	LCT 1 ALCT bunch crossing number
	clct_second_bx0_local	1	0.5	Out	GTLP	LCT 1 local BXN from CLCT
	csc_id[3:0]	4	2	Out	GTLP	CSC chamber ID
	Total Input Signals	64	32			2:1 Multiplexing at 80 MHz

Time	Signal	Bits	Pins	Dir	Logic	Function
1st	lct0_accept	1	0.5	In	GTLP	LCT 0 Accepted by MPC best 3 of 18 sort
2nd	lct1_accept	1	0.5	In	GTLP	LCT 1 Accepted by MPC best 3 of 18 sort
	Total Input Signals	2	1			2:1 Multiplexing at 80 MHz

RPC

80 Inputs 40MHz LVTTL [from receivers on transition module]
0 Outputs

Table 6: RPC Signal Summary

Signal	Bits	Dir	Logic	Function
rpc0_seg[15..0]	16	In	LVTTL	RPC Segment[15..0]
rpc0_bxn[2..0]	3	In	LVTTL	Bunch Crossing Number [2..0]
rpc0_clock	1	In	LVTTL	Clock from RPC Link Board
rpc1_seg[15..0]	16	In	LVTTL	RPC Segment[15..0]
rpc1_bxn[2..0]	3	In	LVTTL	Bunch Crossing Number [2..0]
rpc1_clock	1	In	LVTTL	Clock from RPC Link Board
rpc2_seg[15..0]	16	In	LVTTL	RPC Segment[15..0]
rpc2_bxn[2..0]	3	In	LVTTL	Bunch Crossing Number [2..0]
rpc2_clock	1	In	LVTTL	Clock from RPC Link Board
rpc3_seg[15..0]	16	In	LVTTL	RPC Segment[15..0]
rpc3_bxn[2..0]	3	In	LVTTL	Bunch Crossing Number [2..0]
rpc3_clock	1	In	LVTTL	Clock from RPC Link Board
Total data bits	80			

VME

24 Inputs TTL Address
16 BiDir TTL Data

Table 7: VME Signal Summary

Signal	Bits	Dir	Logic	Function
address	24	In	TTL	VME Address[23..0]
data	16	BiDir	TTL	VME Data[15..0]
control in		In	TTL	VME Control Inputs
control out		Out	TTL	VME Control Outputs

JTAG

5 Inputs LVDS
1 Outputs LVDS

Table 8: JTAG Signal Summary

Signal	Bits	Dir	Logic	Function
tck	1	In	LVDS	JTAG TCK
tms	1	In	LVDS	JTAG TMS
tdi	1	In	LVDS	JTAG TDI
chain_select	2	In	LVDS	Chain Select Address
tdo	1	Out	LVDS	JTAG TDO

LEDs

Table 9: TMB Front Panel LEDs

LED	Color	Function
LCT	Blue	ALCT vpf and CLCT vpf match within the 75ns ALCT window (see note[1] below)
ALCT	Green	ALCT active FEB flag (may not always be the same as ALCT valid pattern flag)
CLCT	Green	CLCT active FEB flag Or any external trigger except ALCT
L1A	Green	Level 1 Accept arrived in L1A window
INVP	Amber	Invalid CLCT pattern after drift delay Pattern dropped below threshold, probably triggered on noise
NMAT	Amber	ALCT vpf or CLCT vpf arrived but did not match in ALCT window
NL1A	Red	No Level 1 Accept arrived in L1A window after TMB triggered Constant flash rate = buffers full
VME	Green	ON = TMB FPGA loaded successfully from PROM Flashes OFF when module addressed by VME

[1] NB: All external triggers (including scintillator and ALCT active FEB) create a dummy CLCT to force the TMB to read out raw hits. ALCT triggers can produce an LCT match if the ALCT active FEB is followed by an ALCT valid pattern flag.

TMB Total I/O Count

Table 10: TMB Total I/O Count

Bits	Pins	Dir	Logic	Connect To	Function
1	2	In	LVDS	CCB	Clock Bus
26	26	In	GTLP	CCB	Fast Control Bus
4	4	In	GTLP	CCB	TMB Reload Bus
12	12	In	GTLP	CCB + 9 DMB + 9 TMB	DAQ Special Purpose Bus
7	7	In	GTLP	CCB + 9 TMB	Trigger Special Purpose Bus
240	120	In	LVDS	5 CFEBs	CFEB Comparators
57	29	In	LVDS	ALCT	ALCT Module
6	6	In	LVTTL	1 DMB	DMB commands
2	1	In	GTLP	MPC	MPC winner
80	40	In	LVTTL	RPC	RPC Inputs
24	24	In	TTL	VME	VME Address
16	16	BiDir	TTL	VME	VME Data
5	5	In	LVTTL	JTAG	JTAG
480	292				Totals

Bits	Pins	Dir	Logic	Connect To	Function
0	0	Out	LVDS	CCB	Clock Bus
0	0	Out	GTLP	CCB	Fast Control Bus
18	18	Out	GTLP	CCB	TMB Reload Bus
0	0	Out	GTLP	CCB + 9 DMB + 9 TMB	DAQ Special Purpose Bus
25	25	Out	GTLP	CCB + 9 TMB	Trigger Special Purpose Bus
5	5	Out	LVDS	5 CFEBs	CFEB Comparators
33	21	Out	LVDS	ALCT	ALCT Module
50	50	Out	LVTTL	1 DMB	DMB data
64	32	Out	GTLP	MPC	MPC winner
0	0	Out	LVTTL	RPC	RPC Inputs
0	0	Out	TTL	VME	VME data is BiDir
1	1	Out	LVTTL	JTAG	JTAG
196	152				Totals

FPGA I/O Estimate: 392 in – 7 clock + 152 out = 537

TMB2001 Connectors

TMB Connector Summary

Table 11: TMB2001 Connector Summary

ID	Pins	Type	Function
J0	50	SCSI-II	CFEB0 Inputs + Clock Out
J1	50	SCSI-II	CFEB1 Inputs + Clock Out
J2	50	SCSI-II	CFEB2 Inputs + Clock Out
J3	50	SCSI-II	CFEB3 Inputs + Clock Out
J4	50	SCSI-II	CFEB4 Inputs + Clock Out
J5	50	SCSI-II	ALCT Cable 1 Inputs
J6	50	SCSI-II	ALCT Cable 2 I/O
J7	10	Header	Xilinx LVDS X-Blaster I/O
P1	160	VME64x	VME J1/P1 Bus I/O
P2A	125	Z-Pack 25x5	CCB + DMB I/O
P2B	55	Z-Pack 11x5	DMB I/O
P3A	55	Z-Pack 11x5	MPC I/O
P3B	125	Z-Pack 25x5	RPC Inputs + ALCT alternate I/O

J0-J4 CFEB0-CFEB4 Connectors

Function: Receives 80MHz data from CFEBs. Transmits 40MHz clock.

Connector Type: PCB: AMP 787190-5
Cable: AMP 749111-4
Shell: AMP 749889-3 [with latches]

Table 12: J0-J4 CFEB0/4-to-TMB Connectors

(This table uses Layer numbers Ly0-to-Ly5, Triad numbers Tr0-to-Tr7)

Pair	Pin		Dir	Logic	Multiplexed Signals	
1	1+	2-	In	LVDS	Ly0Tr0	Ly3Tr0
2	3+	4-	In	LVDS	Ly0Tr2	Ly3Tr2
3	5+	6-	In	LVDS	Ly5Tr0	Ly4Tr0
4	7+	8-	In	LVDS	Ly5Tr2	Ly4Tr2
5	9+	10-	In	LVDS	Ly1Tr0	Ly2Tr0
6	11+	12-	In	LVDS	Ly1Tr2	Ly2Tr2
7	13+	14-	In	LVDS	Ly0Tr4	Ly3Tr4
8	15+	16-	In	LVDS	Ly0Tr6	Ly3Tr6
9	17+	18-	In	LVDS	Ly5Tr4	Ly4Tr4
10	19+	20-	In	LVDS	Ly5Tr6	Ly4Tr6
11	21+	22-	In	LVDS	Ly1Tr4	Ly2Tr4
12	23+	24-	In	LVDS	Ly1Tr6	Ly2Tr6
13	25+	26-	Out	LVDS	LCT_Clock	
14	27+	28-	In	LVDS	Ly1Tr7	Ly2Tr7
15	29+	30-	In	LVDS	Ly1Tr5	Ly2Tr5
16	31+	32-	In	LVDS	Ly5Tr7	Ly4Tr7
17	33+	34-	In	LVDS	Ly5Tr5	Ly4Tr5
18	35+	36-	In	LVDS	Ly0Tr7	Ly3Tr7
19	37+	38-	In	LVDS	Ly0Tr5	Ly3Tr5
20	39+	40-	In	LVDS	Ly1Tr3	Ly2Tr3
21	41+	42-	In	LVDS	Ly1Tr1	Ly2Tr1
22	43+	44-	In	LVDS	Ly5Tr3	Ly4Tr3
23	45+	46-	In	LVDS	Ly5Tr1	Ly4Tr1
24	47+	48-	In	LVDS	Ly0Tr3	Ly3Tr3
25	49+	50-	In	LVDS	Ly0Tr1	Ly3Tr1

J5 ALCT Cable1 Connector (Receiver)

Function: Receives 80MHz data from ALCT.

Connector Type: PCB: AMP 787190-5
Cable: AMP 749111-4
Shell: AMP 749889-3 [with latches]

Table 13: J5 ALCT Cable1 Connector [J10 on ALCT board]

Modified 4/12/01 to match ALCT2001 PCB. Stinking bad signal inversion = ☹

Pair	Inverted	Pin		Dir	Logic	Multiplexed Signals	
		+	-			First in Time	Second in Time
1	☹	1+	2-	In	LVDS	first_valid	second_valid
2		49+	50-	In	LVDS	first_amu	second_amu
3	☹	3+	4-	In	LVDS	first_quality0	second_quality0
4		47+	48-	In	LVDS	first_quality1	second_quality1
5	☹	5+	6-	In	LVDS	first_key0	second_key0
6		45+	46-	In	LVDS	first_key1	second_key1
7	☹	7+	8-	In	LVDS	first_key2	second_key2
8		43+	44-	In	LVDS	first_key3	second_key3
9	☹	9+	10-	In	LVDS	first_key4	second_key4
10		41+	42-	In	LVDS	first_key5	second_key5
11	☹	11+	12-	In	LVDS	first_key6	second_key6
12		39+	40-	In	LVDS	bxn0	bxn3
13	☹	13+	14-	In	LVDS	bxn1	bxn4
14		37+	38-	In	LVDS	bxn2	/wr_fifo
15	☹	15+	16-	In	LVDS	daq_data0	daq_data7
16		35+	36-	In	LVDS	daq_data1	daq_data8
17	☹	17+	18-	In	LVDS	daq_data2	daq_data9
18		33+	34-	In	LVDS	daq_data3	daq_data10
19	☹	19+	20-	In	LVDS	daq_data4	daq_data11
20		31+	32-	In	LVDS	daq_data5	daq_data12
21	☹	21+	22-	In	LVDS	daq_data6	daq_data13
22		29+	30-	In	LVDS	lct_special	first_frame
23	☹	23+	24-	In	LVDS	seq_status0	seu_status0
24		27+	28-	In	LVDS	seq_status1	seu_status1
25	☹	25+	26-	In	LVDS	ddu_special	last_frame

J6 ALCT Cable2 Connector (Transmitter)

Function: Sends/Receives 80MHz data to/from ALCT.

Connector Type: PCB: AMP 787190-5
Cable: AMP 749111-4
Shell: AMP 749889-3 [with latches]

Table 14: J6 ALCT Cable2 Connector [J11 on ALCT board]

Modified 4/12/01 to match ALCT2001 PCB. Stinking bad signal inversion ☹

Pair	Inverted	Pin		Dir	Logic	Multiplexed Signals	
		+	-			First in Time	Second in Time
1		1+	2-	Out	LVDS	tdi	
2	☹	49+	50-	Out	LVDS	tms	
3		3+	4-	Out	LVDS	tck	
4	☹	47+	48-	Out	LVDS	jtag_select0	
5		5+	6-	Out	LVDS	jtag_select1	
6	☹	45+	46-	Out	LVDS	ccb_brcst0	ccb_brcst4
7		7+	8-	Out	LVDS	ccb_brcst1	ccb_brcst5
8	☹	43+	44-	Out	LVDS	ccb_brcst2	ccb_brcst6
9		9+	10-	Out	LVDS	ccb_brcst3	ccb_brcst7
10	☹	41+	42-	Out	LVDS	brcst_str1	subaddr_str
11		11+	12-	Out	LVDS	dout_str	bx0
12	☹	39+	40-	Out	LVDS	ext_inject	ext_trig
13		13+	14-	Out	LVDS	level1_accept	sync_adb_pulse
14	☹	37+	38-	Out	LVDS	seq_cmd0	seq_cmd2
15		15+	16-	Out	LVDS	seq_cmd1	reserved_in4
16	☹	35+	36-	Out	LVDS	reserved_in0[2]	reserved_in2
17		17+	18-	Out	LVDS	reserved_in1	reserved_in3
18	☹	33+	34-	Out	LVDS	async_adb_pulse	
19		19+	20-	Out	LVDS	/hard_reset	
20	☹	31+	32-	Out	LVDS	clock_en	
21		21+	22-	Out	LVDS	clock	
22		29+	30-	In	LVDS	tdo	
23	☹	23+	24-	In	LVDS	reserved_out0	reserved_out2
24		27+	28-	In	LVDS	reserved_out1	reserved_out3
25	☹	25+	26-	In	LVDS	active_feb_flag	cfg_done

[2] Reserved cable input signals connect to ALCT FPGA user input pins

J1-J6 SCSI-II 50-Pin Connector Pin Convention

Figure 2: 50-Pin PCB Connector (Female)[3]

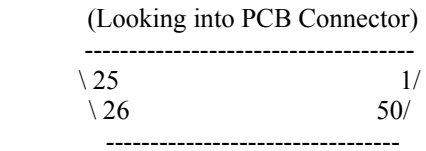


Figure 3: 50 Pin Cable Connector (Male)

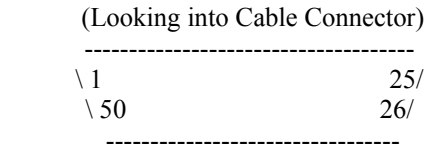
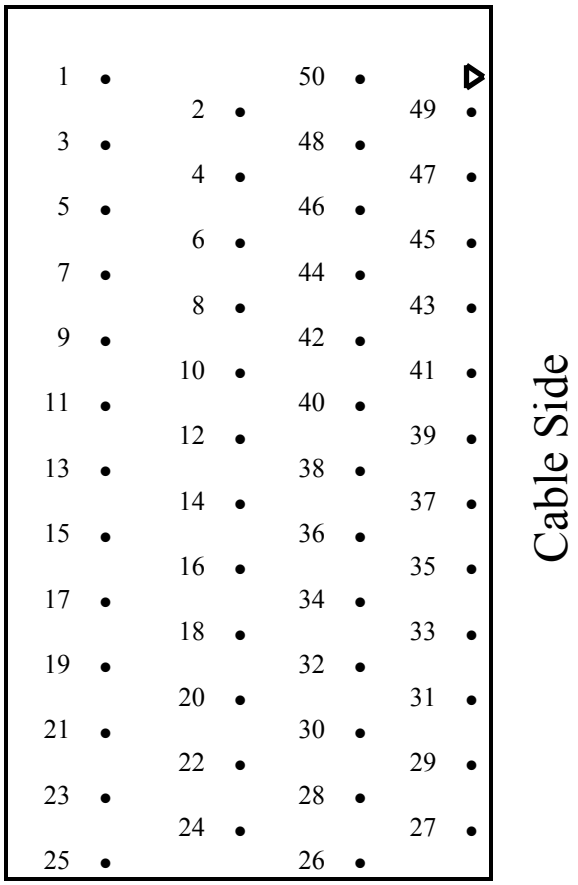


Figure 4: 50 Pin PCB Connector Pin Convention



[3] Copied from CFEB design: http://www.physics.ohio-state.edu/~gujh/works/cmpdata.html

J7 Xilinx LVDS Xilinx X-Blaster Connector

Function: Connects TMB2001 to LVDS x-Blaster for programming FPGAs and PROMs. The LVDS signals and voltage sources on this connector are not directly compatible with the standard Xilinx programming cable.
JTAG chain select signals SEL[3:0] are TTL ☹.

Connector Type: PCB: 3M 3316-5002 16-pin right angle center key
Cable: 3M 3452-6600 16-pin center bump

Table 15: J8 Xilinx LVDS X-Blaster Connector

+TCK	In	1	△	2	In	-TCK
+TDO	Out	3		4	Out	-TDO
+TMS	In	5		6	In	-TMS
+3.3V	Out	7		8	-	GND
+TDI	In	9		10	In	-TDI
+3.3V	In	11		12	In	JTAG_EN(TTL)
SEL0 (TTL)	Out	13		14	In	SEL1 (TTL)
SEL2 (TTL)	In	15		16	In	SEL3 (TTL)

P1 Backplane VME64x J1/P1 Connector

Function: VME interface.

Connector Type: PCB: Harting 02-02-160-2101 Male Right-Angle
Backplane: Harting 02-01-160-2201 Female
Address bits: 24
Data bits: 16
Geographic Address bits: 5

Table 16: P1 VME64x Connector

Pin	Row z	Row a	Row b	Row c	Row d
1	MPR	D00	BBSY*	D08	VPC
2	GND	D01	BCLR*	D09	GND
3	MCLK	D02	ACFAIL*	D10	+V1
4	GND	D03	BG0IN*	D11	+V2
5	MSD	D04	BG0OUT*	D12	RsvU
6	GND	D05	BG1IN*	D13	-V1
7	MMD	D06	BG1OUT*	D14	-V2
8	GND	D07	BG2IN*	D15	RsvU
9	MCTL	GND	BG2OUT*	GND	GAP*
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0*
11	RESP*	GND	BG3OUT*	BERR*	GA1*
12	GND	DS1*	BR0*	SYSRESET*	+3.3V
13	RsvBus1	DS0*	BR1*	LWORD*	GA2*
14	GND	WRITE*	BR2*	AM5	+3.3V
15	RsvBus2	GND	BR3*	A23	GA3*
16	GND	DTACK*	AM0	A22	+3.3V
17	RsvBus3	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	+3.3V
19	RsvBus4	GND	AM3	A19	RsvBus11
20	GND	IACK*	GND	A18	+3.3V
21	RsvBus5	IACKIN*	SERCLK	A17	RsvBus12
22	GND	IACKOUT*	SERDAT	A16	+3.3V
23	RsvBus6	AM4	GND	A15	RsvBus13
24	GND	A07	IRQ7*	A14	+3.3V
25	RsvBus7	A06	IRQ6*	A13	RsvBus14
26	GND	A05	IRQ5*	A12	+3.3V
27	RsvBus8	A04	IRQ4*	A11	LI/I*
28	GND	A03	IRQ3*	A10	+3.3V
29	RsvBus9	A02	IRQ2*	A09	LI/O*
30	GND	A01	IRQ1*	A08	+3.3V
31	RsvBus10	-12V	+5VSTDBY	+12V	GND
32	GND	+5V	+5V	+5V	VPC

P2A Backplane CCB+DMB Connector

Function: Sends and receives data to/from CCB, and carries some DMB signals.

Connector Type: PCB: AMP Z-Pack 125 (25 rows of 5 pins) female AMP 100145-1
Backplane: AMP Z-Pack 125 (25 rows of 5 pins) male AMP ?

Table 17: P2A Backplane CCB+DMB Connector

Pin	Dir	Logic	Signal
A1	In	LVDS	ccb_clock40+
A2	In	GTLP	ccb_clock40_enable
A3	In	GTLP	ccb_cmd0
A4	In	GTLP	ccb_cmb4
A5	In	GTLP	ccb_cmd_strobe
A6	In	GTLP	ccb_data0
A7	In	GTLP	ccb_data4
A8	In	GTLP	ccb_reserved0
A9	In	GTLP	tmb_hard_reset
A10	In	GTLP	alct_adb_pulse_sync
A11	Out	GTLP	clct_status0
A12	Out	GTLP	clct_status4
A13	Out	GTLP	clct_status6
A14	Out	GTLP	alct_status3
A15	Out	GTLP	alct_status7
A16	Out	GTLP	tmb_reserved_in0
A17	Out	GTLP	tmb_reserved_in4
A18			
A19	In	GTLP	dmb_cfeb_calibrate0
A20	In	GTLP	dmb_reserved_out0
A21	In	GTLP	dmb_reserved_out4
A22			
A23	Out	LVTTL	tmb_data0
A24	Out	LVTTL	tmb_data4
A25	Out	LVTTL	tmb_data8

Pin	Dir	Logic	Signal
B1	In	LVDS	ccb_clock40-
B2	In	GTLP	ccb_reserved4
B3	In	GTLP	ccb_cmd1
B4	In	GTLP	ccb_cmb5
B5	In	GTLP	ccb_bx0
B6	In	GTLP	ccb_data1
B7	In	GTLP	ccb_data5
B8	In	GTLP	ccb_reserved1
B9	In	GTLP	alct_hard_reset
B10	In	GTLP	alct_adb_pulse_async
B11	Out	GTLP	clct_status1
B12	Out	GTLP	clct_status5
B13	Out	GTLP	alct_status0
B14	Out	GTLP	alct_status4
B15	Out	GTLP	alct_status8
B16	Out	GTLP	tmb_reserved_in1
B17	In	GTLP	tmb_reserved_out0
B18			
B19	In	GTLP	dmb_cfeb_calibrate1
B20	In	GTLP	dmb_reserved_out1
B21	(In)[1]	GTLP	dmb_reserved_in0
B22			
B23	Out	LVTTL	tmb_data1
B24	Out	LVTTL	tmb_data5
B25	Out	LVTTL	tmb_data9

Pins C1 through C25 are connected to Backplane Ground

Notes:
1) TMB can monitor signals to/from DMB, but can not assert them.

P2A Backplane CCB+DMB Connector Continued

Table 17: P2A Backplane CCB Connector Continued

Pin	Dir	Logic	Signal
D1	Out	GTLP	tmb_config_done
D2			
D3	In	GTLP	ccb_cmd2
D4	In	GTLP	ccb_evcntres
D5	In	GTLP	ccb_l1accept
D6	In	GTLP	ccb_data2
D7	In	GTLP	ccb_data6
D8	In	GTLP	ccb_reserved2
D9	In	GTLP	tmb_reserved0
D10	In	GTLP	clct_external_trigger
D11	Out	GTLP	clct_status2
D12	Out	GTLP	clct_status6
D13	Out	GTLP	clct_status1
D14	Out	GTLP	alct_status5
D15	Out	GTLP	tmb_l1a_request
D16	Out	GTLP	tmb_reserved_in2
D17	In	GTLP	tmb_reserved_out1
D18			
D19	In	GTLP	dmb_cfeb_calibrate2
D20	In	GTLP	dmb_reserved_out2
D21	(In)[1]	GTLP	dmb_reserved_in1
D22			
D23	Out	LVTTL	tmb_data2
D24	Out	LVTTL	tmb_data7
D25	Out	LVTTL	tmb_data11

Pin	Dir	Logic	Signal
E1	Out	GTLP	alct_config_done
E2			
E3	In	GTLP	ccb_cmd3
E4	In	GTLP	ccb_bcntres
E5	In	GTLP	ccb_data_strobe
E6	In	GTLP	ccb_data3
E7	In	GTLP	ccb_data7
E8	In	GTLP	ccb_reserved3
E9	In	GTLP	tmb_reserved1
E10	In	GTLP	alct_external_trigger
E11	Out	GTLP	clct_status3
E12	Out	GTLP	clct_status7
E13	Out	GTLP	alct_status2
E14	Out	GTLP	alct_status6
E15	Out	GTLP	tmb_l1a_release
E16	Out	GTLP	tmb_reserved_in3
E17	In	GTLP	tmb_reserved_out2
E18			
E19	(In)[1]	GTLP	dmb_l1a_release
E20	In	GTLP	dmb_reserved_out3
E21	(In)[1]	GTLP	dmb_reserved_in2
E22			
E23	Out	LVTTL	tmb_data3
E24	Out	LVTTL	tmb_data7
E25	Out	LVTTL	tmb_data11

Notes:
1) TMB can monitor signals to/from DMB, but can not assert them.

P2B Backplane DMB Connector

Function: Sends and receives data to/from DMB.

Connector Type: PCB: AMP Z-Pack 55 (11 rows of 5 pins) female AMP 100161-1
Backplane: AMP Z-Pack 55 (11 rows of 5 pins) male AMP ?

Table 18: P2B Backplane DMB Connector

Pin	Dir	Logic	Signal
A1	Out	LVTTL	tmb_data12
A2	Out	LVTTL	alct_data1
A3	Out	LVTTL	alct_data5
A4	Out	LVTTL	alct_data9
A5	Out	LVTTL	alct_data13
A6	Out	LVTTL	tmb_data_available
A7	Out	LVTTL	tmb_active_feb1
A8	Out	LVTTL	fifo_clock
A9	Out	LVTTL	alct_last_frame
A10	In	LVTTL	res_from_dmb2
A11	Out	LVTTL	res_to_dmb2

Pin	Dir	Logic	Signal
B1	Out	LVTTL	tmb_data13
B2	Out	LVTTL	alct_data2
B3	Out	LVTTL	alct_data6
B4	Out	LVTTL	alct_data10
B5	Out	LVTTL	alct_data14
B6	Out	LVTTL	/tmb_write_enable_fifo
B7	Out	LVTTL	tmb_active_feb2
B8	In	LVTTL	dmb_request_lct
B9	In	LVTTL	dmb_ext_trig
B10	In	LVTTL	res_from_dmb3
B11	Out	LVTTL	res_to_dmb3

Pin	Dir	Logic	Signal
D1	Out	LVTTL	tmb_data14
D2	Out	LVTTL	alct_data3
D3	Out	LVTTL	alct_data7
D4	Out	LVTTL	alct_data11
D5	Out	LVTTL	tmb_ddu_special
D6	Out	LVTTL	tmb_active_feb_flag
D7	Out	LVTTL	tmb_active_feb3
D8	Out	LVTTL	/alct_write_enable_fifo
D9	In	LVTTL	res_from_dmb1
D10	Out	LVTTL	res_to_dmb5
D11	Out	LVTTL	res_to_dmb4

Pin	Dir	Logic	Signal
E1	Out	LVTTL	alct_data0
E2	Out	LVTTL	alct_data4
E3	Out	LVTTL	alct_data8
E4	Out	LVTTL	alct_data12
E5	Out	LVTTL	tmb_last_frame
E6	Out	LVTTL	tmb_active_feb0
E7	Out	LVTTL	tmb_active_feb4
E8	Out	LVTTL	alct_ddu_special
E9	Out	LVTTL	alct_data_available
E10	Out	LVTTL	res_to_dmb1
E11	In	LVTTL	dmb_fpga_pgm_done

Pin	Dir	Logic	Signal
C1	In	Pwr	Gnd
C2	In	Pwr	V_{TT} (+1.5V)
C3	In	Pwr	Gnd
C4	In	Pwr	V_{TT}
C5	In	Pwr	Gnd
C6	In	Pwr	V_{TT}
C7	In	Pwr	Gnd
C8	In	Pwr	V_{TT}
C9	In	Pwr	Gnd
C10	In	Pwr	V_{TT}
C11	In	Pwr	Gnd

P3A Backplane MPC Connector

Function: Sends and receives data to/from MPC.

Connector Type: PCB: AMP Z-Pack 55 (11 rows of 5 pins) female AMP 100161-1
Backplane: AMP Z-Pack 55 (11 rows of 5 pins) male AMP ?

Table 19: P3A Backplane MPC Connector

See ADR_MPCx_FRAMEx on page 34 for signal assigments

Pin	Dir	Logic	Signal
A1	Out	GTLP	/mpc_out0
A2	Out	GTLP	/mpc_out4
A3	Out	GTLP	/mpc_out8
A4	Out	GTLP	/mpc_out12
A5	Out	GTLP	/mpc_out16
A6	Out	GTLP	/mpc_out20
A7	Out	GTLP	/mpc_out24
A8	Out	GTLP	/mpc_out28
A9	In	GTLP	lct_winner
A10			
A11			

Pin	Dir	Logic	Signal
B1	Out	GTLP	/mpc_out1
B2	Out	GTLP	/mpc_out5
B3	Out	GTLP	/mpc_out9
B4	Out	GTLP	/mpc_out13
B5	Out	GTLP	/mpc_out17
B6	Out	GTLP	/mpc_out21
B7	Out	GTLP	/mpc_out25
B8	Out	GTLP	/mpc_out29
B9			
B10			
B11			

Pin	Dir	Logic	Signal
D1	Out	GTLP	/mpc_out2
D2	Out	GTLP	/mpc_out6
D3	Out	GTLP	/mpc_out10
D4	Out	GTLP	/mpc_out14
D5	Out	GTLP	/mpc_out18
D6	Out	GTLP	/mpc_out22
D7	Out	GTLP	/mpc_out26
D8	Out	GTLP	/mpc_out30
D9			
D10			
D11			

Pin	Dir	Logic	Signal
E1	Out	GTLP	/mpc_out3
E2	Out	GTLP	/mpc_out7
E3	Out	GTLP	/mpc_out11
E4	Out	GTLP	/mpc_out15
E5	Out	GTLP	/mpc_out19
E6	Out	GTLP	/mpc_out23
E7	Out	GTLP	/mpc_out27
E8	Out	GTLP	/mpc_out31
E9			
E10			
E11			

Pins C1 through C11 are connected to Backplane Ground

P3B Backplane RPC+ALCT Connector

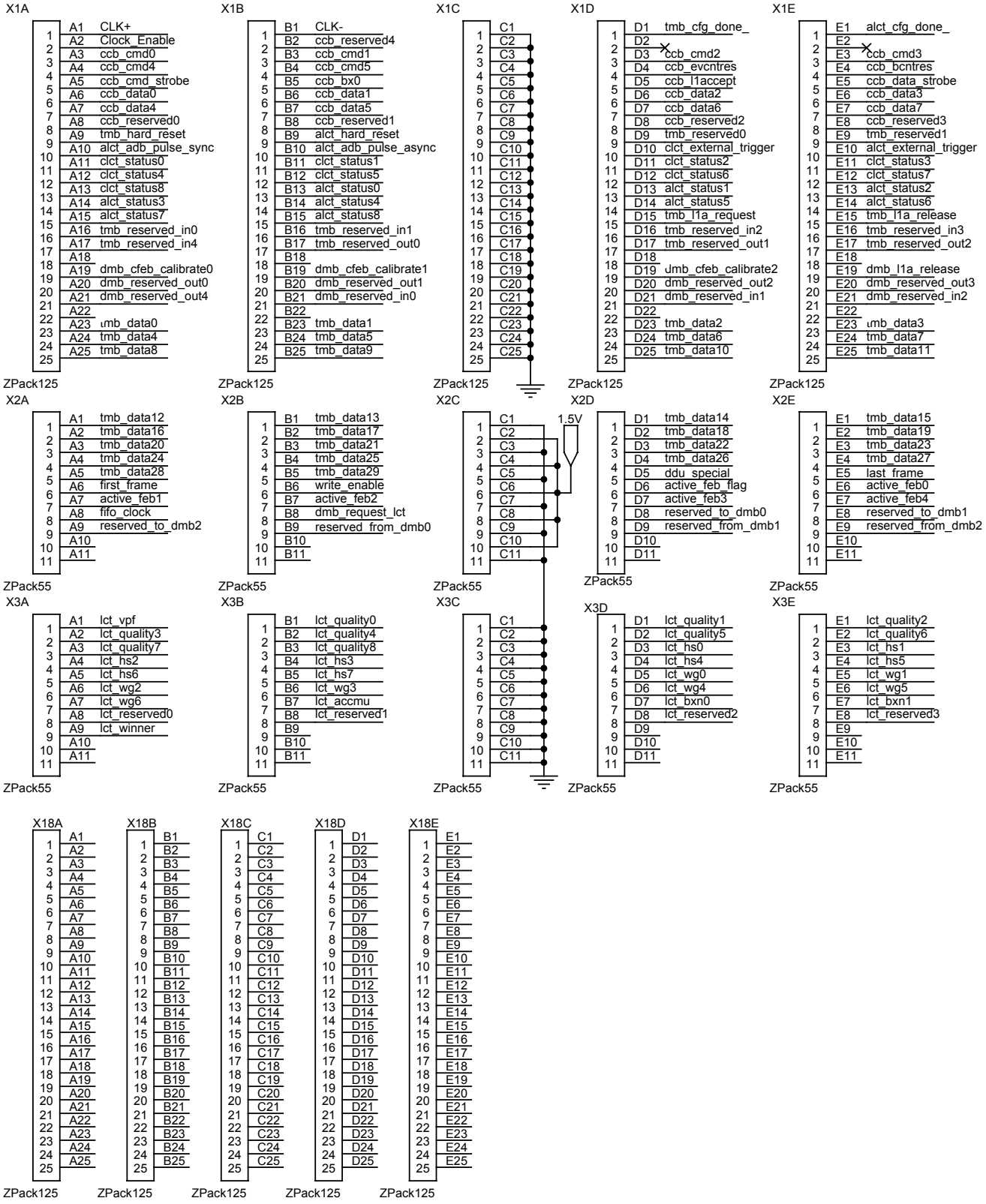
Function: Sends and receives data to/from ALCT, and receives from RPC.

Connector Type: PCB: AMP Z-Pack 125 (25 rows of 5 pins) female AMP 100145-1
Backplane: AMP Z-Pack 125 (25 rows of 5 pins) male AMP ?

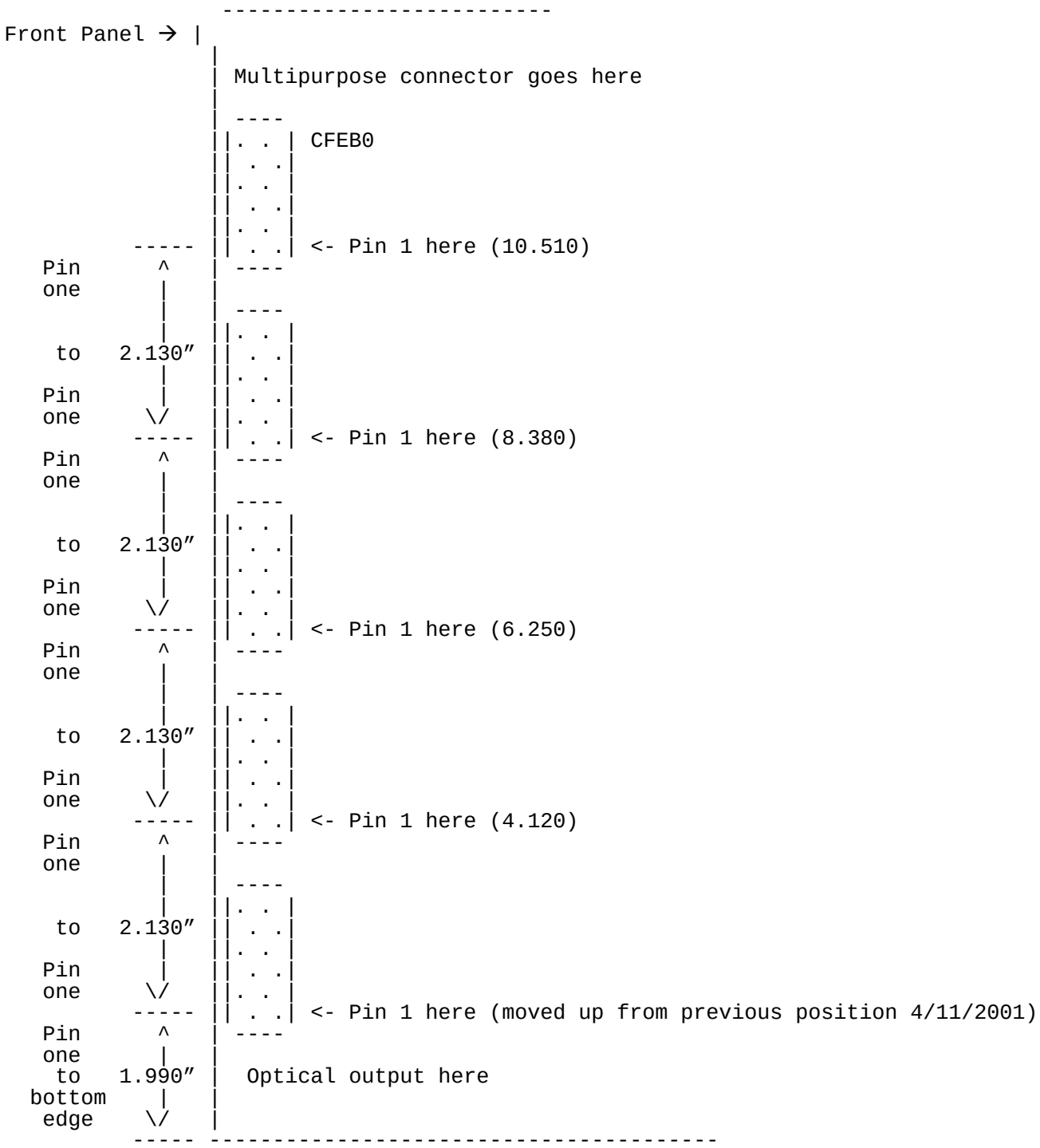
Table 20: P3B Backplane RPC+ALCT Connector

Pin	Signal		Pin	Signal		Pin	Signal		Pin	Signal		Pin	Signal
A1	rpc_rx31		B1	rpc_rx30		C1	rpc_rx29		D1	rpc_rx28		E1	rpc_rx27
A2	rpc_rx26		B2	rpc_rx25		C2	rpc_rx24		D2	rpc_rx23		E2	rpc_rx22
A3	rpc_rx21		B3	rpc_rx20		C3	rpc_rx19		D3	rpc_rx18		E3	rpc_rx17
A4	rpc_rx16		B4	rpc_rx15		C4	rpc_rx14		D4	rpc_rx13		E4	rpc_rx12
A5	rpc_rx11		B5	rpc_rx10		C5	rpc_rx9		D5	rpc_rx8		E5	rpc_rx7
A6	rpc_rx6		B6	rpc_rx5		C6	rpc_rx4		D6	rpc_rx3		E6	rpc_rx2
A7	rpc_rx1		B7	rpc_rx0		C7	rpc_clock		D7	smb_clk		E7	tck
A8	tms		B8	tdi		C8	rpc_loop		D8	posneg		E8	sync
A9	tdo		B9	smbrx		C9	rpc_in37		D9	rpc_in36		E9	rpc_in35
A10	rpc_in34		B10	rpc_in33		C10	rpc_in32		D10			E10	+3.3V
A11	+3.3V		B11	+3.3V		C11	GND		D11	GND		E11	GND
A12	alct_rx31		B12	alct_rx30		C12	alct_rx29		D12	alct_rx28		E12	alct_rx27
A13	alct_rx26		B13	alct_rx25		C13	alct_rx24		D13	alct_rx23		E13	alct_rx22
A14	alct_rx21		B14	alct_rx20		C14	alct_rx19		D14	alct_rx18		E14	alct_rx17
A15	alct_rx16		B15	alct_rx15		C15	alct_rx14		D15	alct_rx13		E15	alct_rx12
A16	alct_rx11		B16	alct_rx10		C16	alct_rx9		D16	alct_rx8		E16	alct_rx7
A17	alct_rx6		B17	alct_rx5		C17	alct_rx4		D17	alct_rx3		E17	alct_rx2
A18	alct_rx1		B18	alct_rx0		C18	smbtx		D18	hrst_rpc		E18	free_tx0
A19	alct_oe		B19	alct_clock		C19	alct_clk_en		D19	txoe		E19	alct_loop
A20	alct_tx23		B20	alct_tx22		C20	alct_tx21		D20	alct_tx20		E20	alct_tx19
A21	alct_tx18		B21	alct_tx17		C21	alct_tx16		D21	alct_tx15		E21	alct_tx14
A22	alct_tx13		B22	alct_tx12		C22	alct_tx11		D22	alct_tx10		E22	alct_tx9
A23	alct_tx8		B23	alct_tx7		C23	alct_tx6		D23	alct_tx5		E23	alct_tx4
A24	alct_tx3		B24	alct_tx2		C24	alct_tx1		D24	alct_tx0		E24	+1.8V
A25	+1.8V		B25	+1.8V		C25	GND		D25	GND		E25	GND

Backplane Pin Diagram



Front Panel Connector Locations



PCB Shunts

Table 20: PCB Shunts

Shunt	Module	1-2 Normal Operation Position	2-3 Special Operations
SH50	Clock	Select CCB 40MHz clock	Select 40MHz on-board crystal
SH55	VME	Enable bootstrap global address SW1 SW2	Disable
SH56	VME	Enable bootstrap geographic address	Disable
SH57	VME	Enable bootstrap VME logic	Disable
SH62	VME	Select backplane as geographic address	Select SW1-SW2 as geographic address
SH74	JTAG	JTAG chain select comes from X-blaster	JTAG chain select comes from SW3
SH95	VME	Enable CCB hard reset to clear bootstrap register	Disable
SH99	Power	Select +3.3Vcc for U99+U101 delay chips	Select +5Vcc
SH104	VME	Enable VME hard reset for TMB and ALCT	Disable
SH105	VME	Enable CCB hard reset for TMB and ALCT	Disable
SH106	VME	Enable ALCT hard reset by FPGA	Disable
SH107	VME	Enable TMB hard reset by FPGA (self reset)	Disable
SH69-1	Power	Disconnect +3.3V from U69 1.5Vregulator input	Connect +3.3V to U69 1.5Vregulator input
SH69-2	Power	Select backplane as source of +1.5V	Select U69 as source of +1.5V
SH1081	VME	TMB hard reset pulse width set by CCB	TMB hard reset pulse width 400ns one-shot
SH1082	VME	ALCT hard reset pulse width set by CCB	ALCT hard reset pulse width 400ns one-shot

CCB Front Panel

CCB Input connector P10

Pin (+)	Pin (-)	Signal
1	2	external_clock40
3	4	external_clock40_enable
5	6	external_l1accept
7	8	dmb_cfeb_calibrate[0]
9	10	dmb_cfeb_calibrate[1]
11	12	dmb_cfeb_calibrate[2]
13	14	alct_adb_pulse_sync
15	16	alct_adb_pulse_async
17	18	clct_external_trigger
19	20	alct_external_trigger
21	22	tmb_l1a_request
23	24	ccb_fp_reserved_in[0]
25	26	ccb_fp_reserved_in[1]
27	28	
29	30	
31	32	
33	34	

CCB Output connector P11

Pin (+)	Pin (-)	Signal	Test Point	TMB Assignment	Description
1	2	clct_status[0]	391-1	pretrig	Sequencer pre-triggered
3	4	clct_status[1]	391-2	seq_busy	Sequencer busy
5	6	clct_status[2]	391-3	invpat	Invalid pattern after drift delay
7	8	clct_status[3]	391-4	daqmb	Dump to DMB in progress
9	10	clct_status[4]	391-5	l1a_window	L1A window
11	12	clct_status[5]	391-6	l1a	L1A (should be in L1A window)
13	14	clct_status[6]	391-7	tmb	CLCT sent for TMB match
15	16	clct_status[7]	391-8	tmb_flush	TMB found no match or rejected trigger
17	18	clct_status[8]	391-9	nol1a_flush	No L1A, Sequencer flushing event
19	20	ccb_clock40			
21	22	ccb_bx0			
23	24	ccb_l1accept			
25	26	ccb_cmdstr			
27	28	ccb_fp_reserved_out[0]			
29	30				
31	32				
33	34				

CCB Output connector P12

Pin (+)	Pin (-)	Signal	Test Point	TMB Assignment	Description
1	2	alct_status[0]	392-1	alct_active_feb	ALCT fast active AFEB
3	4	alct_status[1]	392-2	first_valid	First muon valid pattern flag
5	6	alct_status[2]	392-3	second_valid	Second muon valid pattern flag
7	8	alct_status[3]	392-4	first_amu	First accelerator muon flag
9	10	alct_status[4]	392-5	second_amu	Second accelerator muon flag
11	12	alct_status[5]	392-6	/wr_fifo(alct)	ALCT /write enable raw-hit FIFO
13	14	alct_status[6]	392-7	alct_vpf	ALCT 1st Valid Pattern (TMB pipe)
15	16	alct_status[7]	392-8	clct_vpf	CLCT 1st Valid Pattern (TMB pipe)
17	18	alct_status[8]	392-9	scint_veto	Scintillator Veto (clears via VME)
19	20				
21	22				
23	24				
25	26				
27	28				
29	30				
31	32				
33	34				

Revision History

Version	Date	Action
1.00	07/12/03	Initial, copied from TMB2001
1.01	10/29/03	Replaced PHOS4 registers with DDD, update shunts table, rat signals updated
1.02	03/15/04	Update 3D3444 registers, add RAT/RPC registers
1.03	03/16/04	Move RAT register addy to match bdtest.v
1.04	04/15/04	Copy from TMB2003
2.01	05/19/04	Add RPC Readout
2.01	06/09/04	New registers B6-CC, 4 new header words, new raw hits format, started logic docs