



Pin assignment for the boards in the peripheral crate

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- Zpack125 on schematics is AMP part number 100145-1 (female 25 rows by 5 pins).
- Zpack55 on schematics is AMP part number 100161-1 (female 11 rows by 5 pins).
- The guiding pins will be implemented on the backplane-strengthening bars. The corresponding guiding modules are shown on the mechanical drawings (AMP partnumber 223957-1). These modules are used also for keying the boards.
- All signal names match those in Jonathan's document (EMU Peripheral Crate Specification, version 3.2).
- All bussed signals must NOT be terminated on boards, the tracks from the connector to GTLP transceivers should be done as short as possible.
- All 40 MHz point-to-point signals must be terminated on receiving boards: 100 OHM to 1.5 V for GTLP, 100 OHM between the complementary signals for LVDS (clock), as close to the receiver as possible.
- All 80 MHz signals must be terminated on receiving boards: 50 OHM to 1.5 V for GTLP, as close to the receiver as possible.
- 1.5 V power from the backplane is provided for GTLP termination. The board designer should provide bypassing for it. MPC is powered from two regulators, so there are two 1.5V inputs. The load must be distributed so that each of the regulators provides exactly one half of the total power necessary to terminate all GTLP signals.
- TMB RPC feed-thru connector (X18) pin assignment is not defined, all pins are left unconnected on the backplane.
- Mechanical drawings for connector placement are available here:

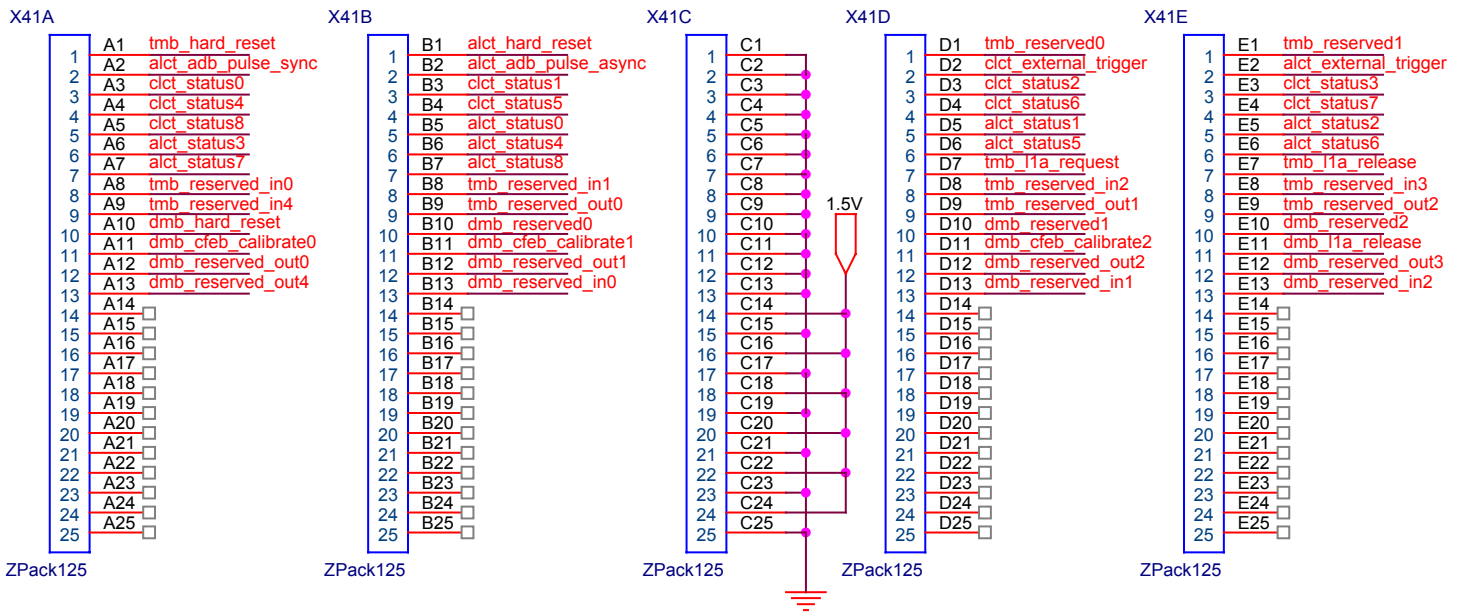
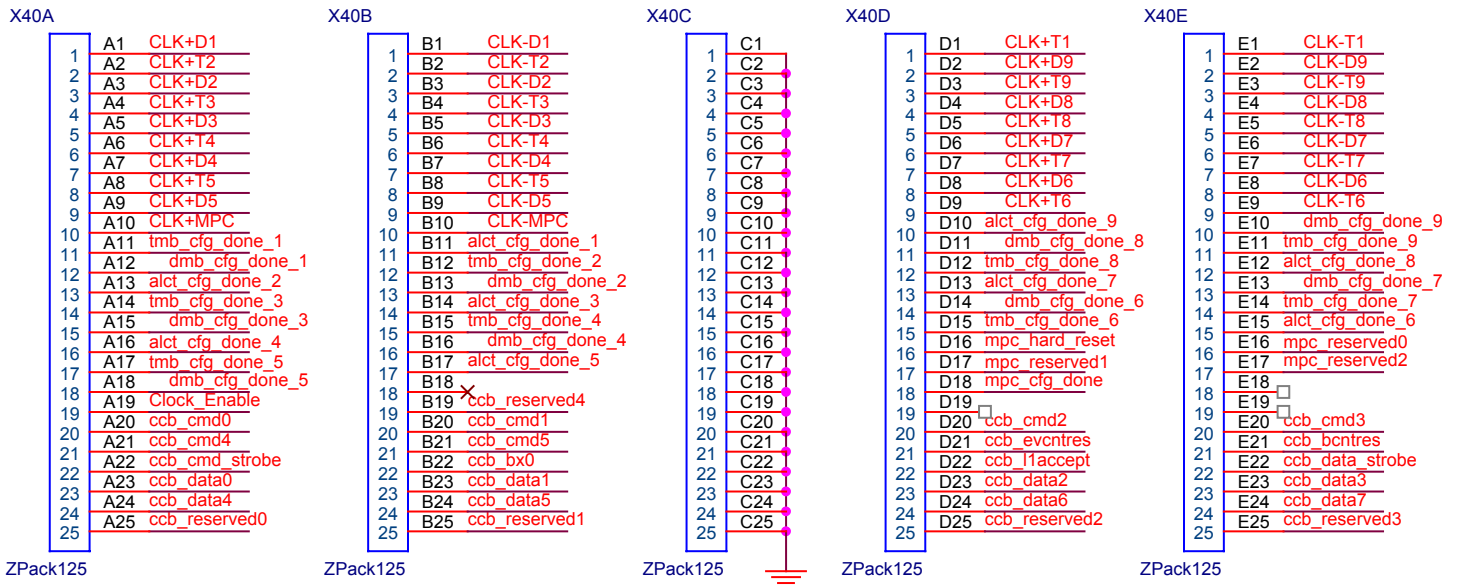
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<http://www.phys.ufl.edu/~madorsky/backplane/dmb.dxf>

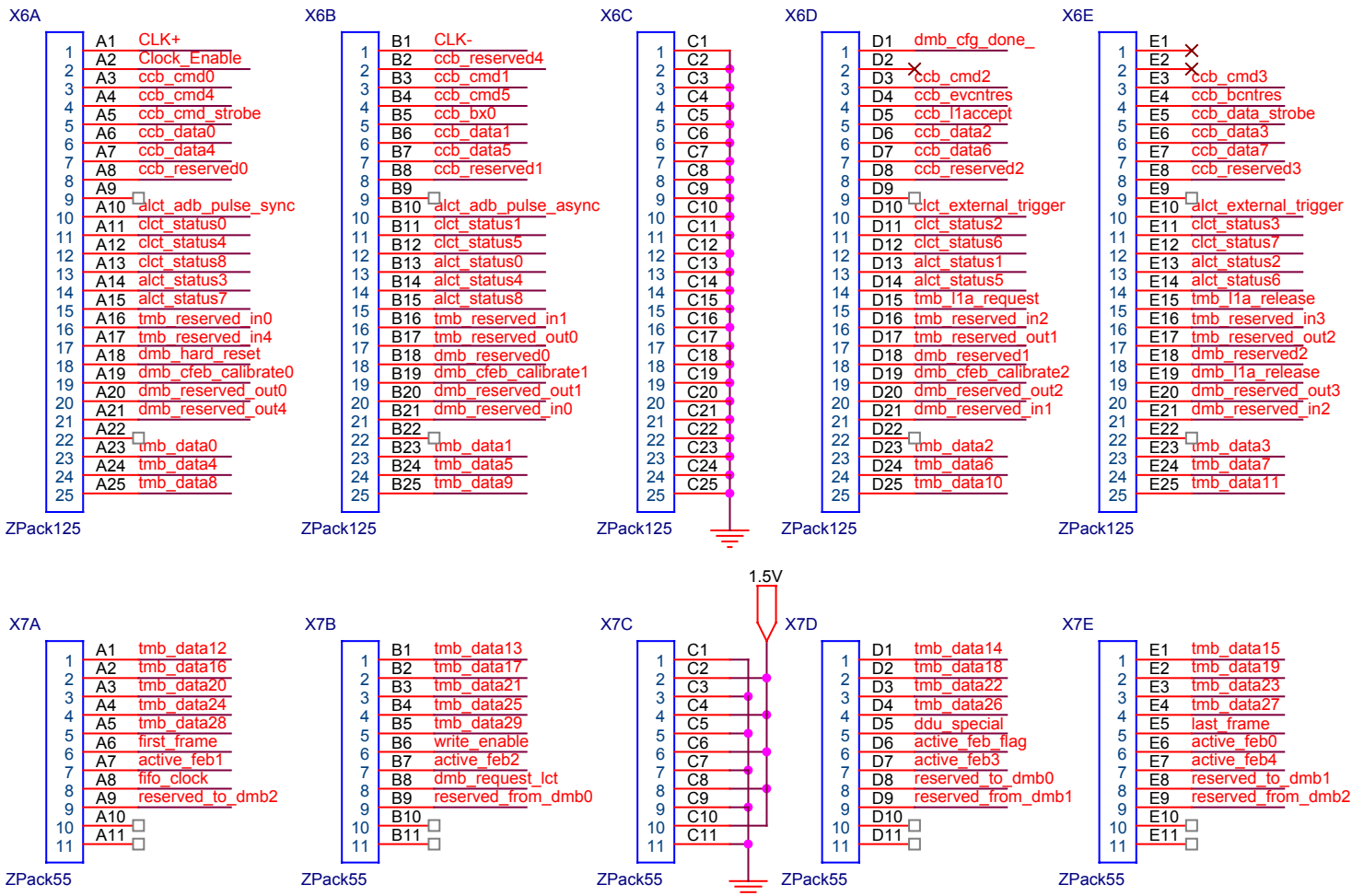
<http://www.phys.ufl.edu/~madorsky/backplane/mpc.dxf>

<http://www.phys.ufl.edu/~madorsky/backplane/tmb.dxf>

Download these files to your local disk and then open by the application supporting DXF – OrCAD (use VisualCAD tool), AutoCAD, Volo View (available for free from <http://www.download.com/>), and by many other applications.



CCB



DMB

X36A

1	A1	CLK+
2	A2	
3	A3	
4	A4	
5	A5	Clock_Enable
6	A6	ccb_cmd0
7	A7	ccb_cmd4
8	A8	ccb_cmd_strobe
9	A9	ccb_data0
10	A10	ccb_data4
11	A11	ccb_reserved0
12	A12	lct8_vpf
13	A13	lct8_quality3
14	A14	lct8_quality7
15	A15	lct8_hs2
16	A16	lct8_hs6
17	A17	lct8_wg2
18	A18	lct8_wg6
19	A19	lct8_reserved0
20	A20	lct2_vpf
21	A21	lct2_quality3
22	A22	lct2_quality7
23	A23	lct2_hs2
24	A24	lct2_hs6
25	A25	lct2_wg2

X37A

1	A1	lct2_wg6
2	A2	lct2_reserved0
3	A3	lct2_winner
4	A4	lct6_vpf
5	A5	lct6_quality3
6	A6	lct6_quality7
7	A7	lct6_hs2
8	A8	lct6_hs6
9	A9	lct6_wg2
10	A10	lct6_wg6
11	A11	lct6_reserved0

X38A

1	A1	lct4_vpf
2	A2	lct4_quality3
3	A3	lct4_quality7
4	A4	lct4_hs2
5	A5	lct4_hs6
6	A6	lct4_wg2
7	A7	lct4_wg6
8	A8	lct4_reserved0
9	A9	lct5_vpf
10	A10	lct5_quality3
11	A11	lct5_quality7
12	A12	lct5_hs2
13	A13	lct5_hs6
14	A14	lct5_wg2
15	A15	lct5_wg6
16	A16	lct5_reserved0
17	A17	lct3_vpf
18	A18	lct3_quality3
19	A19	lct3_quality7
20	A20	lct3_hs2
21	A21	lct3_hs6
22	A22	lct3_wg2
23	A23	lct3_wg6
24	A24	lct3_reserved0
25	A25	lct1_winner

X39A

1	A1	lct7_vpf
2	A2	lct7_quality3
3	A3	lct7_quality7
4	A4	lct7_hs2
5	A5	lct7_hs6
6	A6	lct7_wg2
7	A7	lct7_wg6
8	A8	lct7_reserved0
9	A9	lct1_vpf
10	A10	lct1_quality3
11	A11	lct1_quality7
12	A12	lct1_hs2
13	A13	lct1_hs6
14	A14	lct1_wg2
15	A15	lct1_wg6
16	A16	lct1_reserved0
17	A17	lct9_vpf
18	A18	lct9_quality3
19	A19	lct9_quality7
20	A20	lct9_hs2
21	A21	lct9_hs6
22	A22	lct9_wg2
23	A23	lct9_wg6
24	A24	lct9_reserved0
25	A25	lct9_winner

ZPack125

X36B

1	B1	CLK-
2	B2	
3	B3	
4	B4	
5	B5	ccb_reserved4
6	B6	ccb_cmd1
7	B7	ccb_cmd5
8	B8	ccb_bx0
9	B9	ccb_data1
10	B10	ccb_data5
11	B11	ccb_reserved1
12	B12	lct8_quality0
13	B13	lct8_quality4
14	B14	lct8_quality8
15	B15	lct8_hs3
16	B16	lct8_hs7
17	B17	lct8_wg3
18	B18	lct8_accmu
19	B19	lct8_reserved1
20	B20	lct2_quality0
21	B21	lct2_quality4
22	B22	lct2_quality8
23	B23	lct2_hs3
24	B24	lct2_hs7
25	B25	lct2_wg3

X37B

1	B1	lct2_accmu
2	B2	lct2_reserved1
3	B3	lct4_winner
4	B4	lct6_quality0
5	B5	lct6_quality4
6	B6	lct6_quality8
7	B7	lct6_hs3
8	B8	lct6_hs7
9	B9	lct6_wg3
10	B10	lct6_accmu
11	B11	lct6_reserved1

X38B

1	B1	lct4_quality0
2	B2	lct4_quality4
3	B3	lct4_quality8
4	B4	lct4_hs3
5	B5	lct4_hs7
6	B6	lct4_wg3
7	B7	lct4_accmu
8	B8	lct4_reserved1
9	B9	lct5_quality0
10	B10	lct5_quality4
11	B11	lct5_quality8
12	B12	lct5_hs3
13	B13	lct5_hs7
14	B14	lct5_wg3
15	B15	lct5_accmu
16	B16	lct5_reserved1
17	B17	lct3_quality0
18	B18	lct3_quality4
19	B19	lct3_quality8
20	B20	lct3_hs3
21	B21	lct3_hs7
22	B22	lct3_wg3
23	B23	lct3_accmu
24	B24	lct3_reserved1
25	B25	lct3_winner

X39B

1	B1	lct7_quality0
2	B2	lct7_quality4
3	B3	lct7_quality8
4	B4	lct7_hs3
5	B5	lct7_hs7
6	B6	lct7_wg3
7	B7	lct7_accmu
8	B8	lct7_reserved1
9	B9	lct1_quality0
10	B10	lct1_quality4
11	B11	lct1_quality8
12	B12	lct1_hs3
13	B13	lct1_hs7
14	B14	lct1_wg3
15	B15	lct1_accmu
16	B16	lct1_reserved1
17	B17	lct9_quality0
18	B18	lct9_quality4
19	B19	lct9_quality8
20	B20	lct9_hs3
21	B21	lct9_hs7
22	B22	lct9_wg3
23	B23	lct9_accmu
24	B24	lct9_reserved1
25	B25	

ZPack125

X36C

1	C1	
2	C2	
3	C3	
4	C4	
5	C5	
6	C6	
7	C7	
8	C8	
9	C9	
10	C10	
11	C11	
12	C12	
13	C13	
14	C14	
15	C15	
16	C16	
17	C17	
18	C18	
19	C19	
20	C20	
21	C21	
22	C22	
23	C23	
24	C24	
25	C25	

X37C

1	C1	
2	C2	
3	C3	
4	C4	
5	C5	
6	C6	
7	C7	
8	C8	
9	C9	
10	C10	
11	C11	

X38C

1	C1	
2	C2	
3	C3	
4	C4	
5	C5	
6	C6	
7	C7	
8	C8	
9	C9	
10	C10	
11	C11	
12	C12	
13	C13	
14	C14	
15	C15	
16	C16	
17	C17	
18	C18	
19	C19	
20	C20	
21	C21	
22	C22	
23	C23	
24	C24	
25	C25	

X39C

1	C1	
2	C2	
3	C3	
4	C4	
5	C5	
6	C6	
7	C7	
8	C8	
9	C9	
10	C10	
11	C11	
12	C12	
13	C13	
14	C14	
15	C15	
16	C16	
17	C17	
18	C18	
19	C19	
20	C20	
21	C21	
22	C22	
23	C23	
24	C24	
25	C25	

ZPack125

X36D

1	D1	mpc_hard_reset
2	D2	mpc_reserved1
3	D3	
4	D4	
5	D5	
6	D6	ccb_cmd2
7	D7	ccb_evtntres
8	D8	ccb_data_strobe
9	D9	ccb_data2
10	D10	ccb_data6
11	D11	ccb_reserved2
12	D12	lct8_quality1
13	D13	lct8_quality5
14	D14	lct8_hs0
15	D15	lct8_hs4
16	D16	lct8_wg0
17	D17	lct8_wg4
18	D18	lct8_bxn0
19	D19	lct8_reserved2
20	D20	lct2_quality1
21	D21	lct2_quality5
22	D22	lct2_hs0
23	D23	lct2_hs4
24	D24	lct2_wg0
25	D25	lct2_wg4

X37D

1	D1	lct2_bxn0
2	D2	lct2_reserved2
3	D3	lct6_winner
4	D4	lct6_quality1
5	D5	lct6_quality5
6	D6	lct6_hs0
7	D7	lct6_hs4
8	D8	lct6_wg0
9	D9	lct6_wg4
10	D10	lct6_bxn0
11	D11	lct6_reserved2

X38D

1	D1	lct4_quality1
2	D2	lct4_quality5
3	D3	lct4_hs0
4	D4	lct4_hs4
5	D5	lct4_wg0
6	D6	lct4_wg4
7	D7	lct4_bxn0
8	D8	lct4_reserved2
9	D9	lct5_quality1
10	D10	lct5_quality5
11	D11	lct5_hs0
12	D12	lct5_hs4
13	D13	lct5_wg0
14	D14	lct5_wg4
15	D15	lct5_bxn0
16	D16	lct5_reserved2
17	D17	lct3_quality1
18	D18	lct3_quality5
19	D19	lct3_hs0
20	D20	lct3_hs4
21	D21	lct3_wg0
22	D22	lct3_wg4
23	D23	lct3_bxn0
24	D24	lct3_reserved2
25	D25	lct5_winner

X39D

1	D1	lct7_quality1
2	D2	lct7_quality5
3	D3	lct7_hs0
4	D4	lct7_hs4
5	D5	lct7_wg0
6	D6	lct7_wg4
7	D7	lct7_bxn0
8	D8	lct7_reserved2
9	D9	lct1_quality1
10	D10	lct1_quality5
11	D11	lct1_hs0
12	D12	lct1_hs4
13	D13	lct1_wg0
14	D14	lct1_wg4
15	D15	lct1_bxn0
16	D16	lct1_reserved2
17	D17	lct9_quality1
18	D18	lct9_quality5
19	D19	lct9_hs0
20	D20	lct9_hs4
21	D21	lct9_wg0
22	D22	lct9_wg4
23	D23	lct9_bxn0
24	D24	lct9_reserved2
25	D25	

ZPack125

X36E

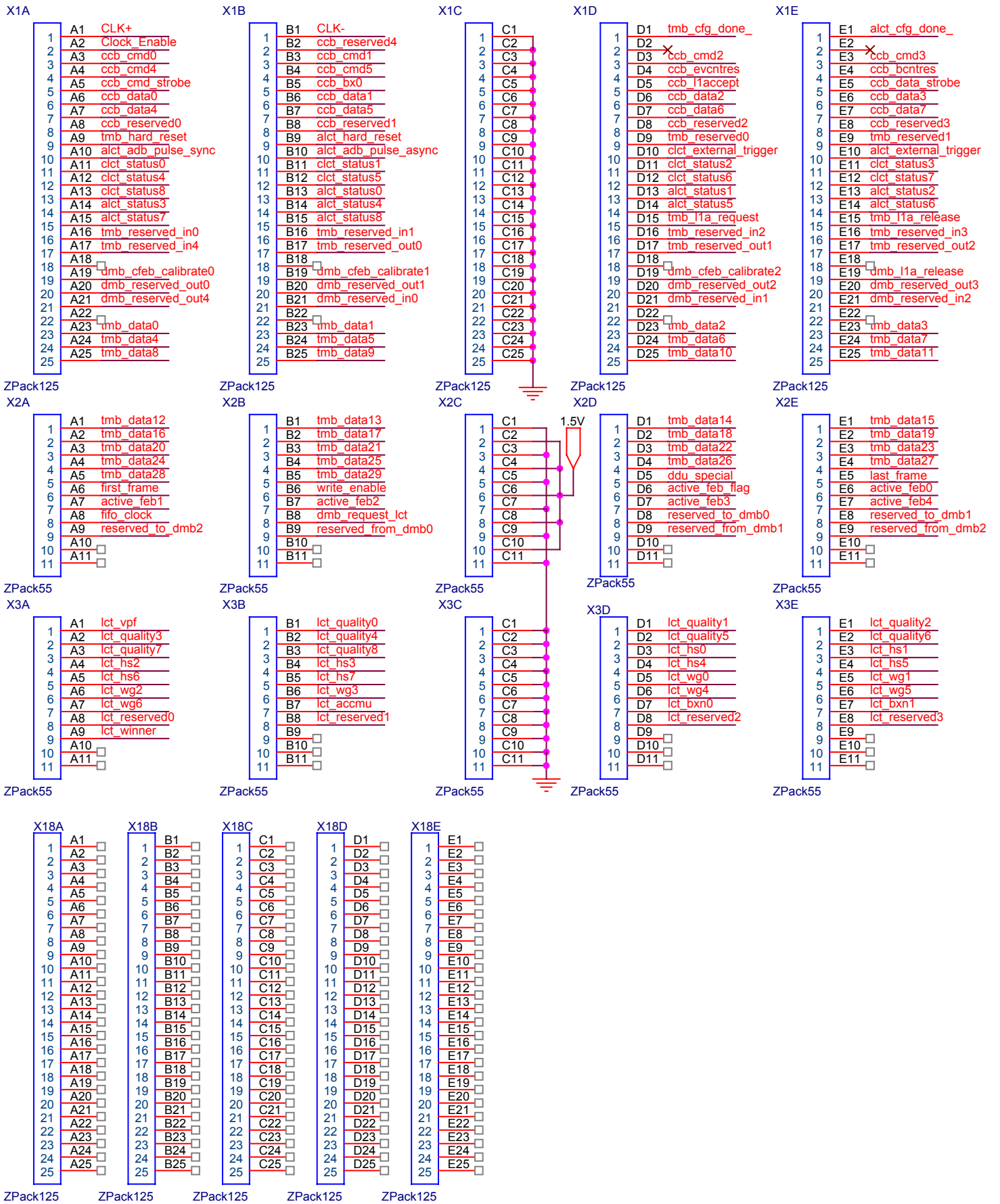
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2	E2	mpc_reserved2
3	E3	mpc_cfg_done
4	E4	
5	E5	
6	E6	ccb_cmd3
7	E7	ccb_bcntres
8	E8	ccb_data_strobe
9	E9	ccb_data3
10	E10	ccb_data7
11	E11	ccb_reserved3
12	E12	lct8_quality2
13	E13	lct8_quality6
14	E14	lct8_hs1
15	E15	lct8_hs5
16	E16	lct8_wg1
17	E17	lct8_wg5
18	E18	lct8_bxn1
19	E19	lct8_reserved3
20	E20	lct2_quality2
21	E21	lct2_quality6
22	E22	lct2_hs1
23	E23	lct2_hs5
24	E24	lct2_wg1
25	E25	lct2_wg5

X37E

1	E1	lct2_bxn1
2	E2	lct2_reserved3
3	E3	lct8_winner
4	E4	lct6_quality2
5	E5	lct6_quality6
6	E6	lct6_hs1
7	E7	lct6_hs5
8	E8	lct6_wg1
9	E9	lct6_wg5
10	E10	lct6_bxn1
11	E11	lct6_reserved3

X38E

1	E1	lct4_quality2
2	E2	lct4_quality6
3	E3	lct4_hs1
4	E4	lct4_hs5
5	E5	lct4_wg1
6	E6	lct4_wg5
7	E7	lct4_bxn1
8	E8	lct4_reserved3
9	E9	lct5_quality2
10	E10	lct5_quality6
11	E11	lct5_hs1
12	E12	lct5_hs5
13	E13	lct5_wg1
14	E14	lct5_wg5
15	E15	lct5_bxn1
16	E16	lct5_reserved3
17	E17	lct3_quality2
18	E18	lct3_quality6
19	E19	lct3_hs1
20	E20	lct3_hs5
21	E21	lct3_wg1
22	E22	lct3_wg5
23	E23	lct3_bxn1
24	E24	lct3_reserved3



Revision history:

- 02/05/01 – Creation
- 02/06/01 – Title changed to reflect better the purpose of this document
- 02/12/01 – Clock_Enable+ renamed to Clock_Enable, Clock_Enable- renamed to ccb_reserved4
- 02/22/01 – Universal Power Modules added to TMB, DMB, CCB. MPC 1.5 V power is split in two halves.
- 02/26/01 – Mechanical drawings links added.
- 03/02/01 – Universal Power Modules excluded, all board's connectors are changed to female type, guiding hardware added. Mechanical drawings updated.