

Sector Processor Core Logic Interface

Virtex-5 upgrade

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Inputs

me1a, me1b, me1c, me1d, me1e, me1f

bit width: 28

Six track stub inputs from station 1

Table 1. ME1 input bit fields.

Bits	Name	Description
11:0	Phi	Phi of the track stub
18:12	Eta	Eta of the track stub
22:19	Q	Quality of the track stub
26:23	CSCid	Chamber number this track stub belongs to
27	Valid	1 if this track stub is valid

me2a, me2b, me2c
me3a, me3b, me3c
me4a, me4b, me4c

bit width: 24

Track stub inputs from stations 2,3,4, three stubs from each.

Table 2. ME2,3,4 input bit fields.

Bits	Name	Description
11:0	Phi	Phi of the track stub
18:12	Eta	Eta of the track stub
22:19	Q	Quality of the track stub
23	Valid	1 if this track stub is valid

mb1a, mb1b

bit width: 16

Two track stub inputs from drift tube trigger system. Data on these inputs can be serialized by DT trigger system (see FL flag in Table 3).

Table 3. MB input bit field.

Bits	Name	Description
11:0	Phi	Phi of the track stub
14:12	Q	Quality of the track stub
15	FL	FL is set to 1 if this track stub belongs to the previous BX

mnetas0, mnetas1, mnetas2, mnetas3, mnetas4, mnetas5, mnetas6, mnetas7

bit width: 7

Minimum eta for collision extrapolation units, see Table 4 for details.

mxetas0, mxetas1, mxetas2, mxetas3, mxetas4, mxetas5, mxetas6, mxetas7

bit width: 7

Maximum eta for collision extrapolation units, see Table 4 for details.

etawn0, etawn1, etawn2, etawn3, etawn4, etawn5, etawn7

bit width: 8

Eta windows for collision extrapolation units, see Table 4 for details.

Table 4. Control parameters for collision extrapolation units.

Extrapolation unit	Minimum Eta		Maximum Eta		Eta Window	
	Index	Default (dec)	Index	Default (dec)	Index	Default (dec)
1-2	0	22	0	127	0	4
1-3	1	22	1	127	1	4
2-3	2	14	2	127	2	4
2-4	3	14	3	127	3	4
3-4	4	14	4	127	4	4
1-2 overlap	5	14	5	24	5	4
2-DT 1	6	10	6	24	N/A	N/A
1-4	7	22	7	127	7	4

mindphi

bit width: 12

Minimum phi difference for track cancellation logic, default = 128

mindeta

bit width: 5

Minimum eta difference for track cancellation logic, default = 8

emindeta_acc0, emindeta_acc1

bit width: 7

Minimum eta difference for halo tracks, see Table 5 for details.

emaxdeta_acc0, emaxdeta_acc1

bit width: 7

Maximum eta difference for halo tracks, see Table 5 for details.

maxdphi_acc0, maxdphi_acc1

bit width: 10

Maximum phi difference for halo tracks, see Table 5 for details.

Table 5. Control parameters for halo extrapolation units.

Extrapolation unit	Minimum Deta		Maximum Deta		Maximum Dphi	
	Index	Default (dec)	Index	Default (dec)	Index	Default (dec)
1-2	0	4	0	16	0	64
1-3	1	4	1	16	1	64

straight

bit width: 12

Parameter for the correction of misaligned 1-2-3-4 tracks, default = 60.

curved

bit width: 12

Parameter for the correction of misaligned 1-2-3-4 tracks, default = 200.

control

bit width: 16

Control input. Used to turn on/off various features in the core.

Table 6. Control input.

Bits	Name	Description	Default	Range
0	wide_phi	enable wider phi extrapolations	0	
3:1	BXA_depth	Depth of BXA history	2	0-2
6:4	reserved		0	
8:7	Pretrigger	Number of track segments to pre-trigger	2	1-3
15:9	reserved		0	

clk

Clock input, 40.08 MHz.

Outputs

pHp, pMp, pLp

bit width: 29

Parameters of the tracks found by the track finder on each clock cycle. pHp is the highest quality track, pLp is the lowest.

Table 7. pHp, pMp, pLp bit fields.

Bits	Name	Description
4:0	eta	Eta of the track that was found
8:5	mode	Mode parameter
9	charge	Charge of the particle
21:10	dphi	Delta Phi
22	sign	Sign
27:23	phi	Phi of the track that was found
28	FR	Front/rear flag – tells if ME1 chamber is in front of rear

PT assignment lookup memory address should be constructed as shown below:

Addr = {FR, sign, mode, eta[4:1], dphi};

idHp, idMp, idLp

bit width: 22

Numbers of the track stubs which resulted into track found by the logic. idHp shows the track stubs for pHp output, idMp for pMp, and idLp for pLp. All numbers start from 1. 0 means that no track stub from this station participated in the decision.

Table 8. idHp, idMp, idLp bit fields.

Bits	Name	Description	Range
2:0	Id1	Number of track stub from station 1	1-6
4:3	Bxd1	Track stub from station 1 delay by BXA	0-2
6:5	Id2	Number of track stub from station 2	1-3
8:7	Bxd2	Track stub from station 2 delay by BXA	0-2
10:9	Id3	Number of track stub from station 3	1-3
12:11	Bxd3	Track stub from station 3 delay by BXA	0-2
14:13	Id4	Number of track stub from station 4	1-3
16:15	Bxd4	Track stub from station 4 delay by BXA	0-2
19:17	Idb1	Number of track stub from DT station 1	1-4
21:20	Bxdb1	Track stub from DT station 1 delay by BXA	0-2

date

bit width: 16

Shows the date when this version of the core was generated from VPP model.

Table 9. Date bit fields.

Bits	Name	Description
0:6	Year	Year – 2000
11:7	Day	Day
15:12	Month	Month

Revision history (started 2008-09-09, even though this document is way older than that)

Date	Modifications
2008-09-09	<ul style="list-style-type: none">• added halo_delay field to control register• added wide_phi field to control register• added new but unused parameters for future implementation of Rick's corrections to 1-2-3-4 tracks:<ul style="list-style-type: none">○ straight○ curved
2008-12-19	modifications for 2008 upgrade <ul style="list-style-type: none">• halo:<ul style="list-style-type: none">○ extrapolations 1-2 and 1-3 added○ halo reports eta and phi○ halo track may be reported on any output○ eta and phi cancellation• 12-bit phi cancellation• Eta cancellation• Rick's corrections for 1-2-3-4 tracks• 1-4 extrapolations for collisions• removed unused mneta, mxeta inputs (left from barrel station 2)• removed halo_delay from control input, implemented in wrapper• Unused bits removed from:<ul style="list-style-type: none">○ ME2,3,4 inputs○ idHp, idMp, idLp outputs