

Sector Processor Core Logic

Virtex-5 upgrade

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Inputs

me1a, me1b, me1c, me1d, me1e, me1f

bit width: 28

Six track stub inputs from station 1

Table 1. ME1 input bit fields.

Bits	Name	Description
11:0	Phi	Phi of the track stub
18:12	Eta	Eta of the track stub
22:19	Q	Quality of the track stub
26:23	CSCid	Chamber number this track stub belongs to
27	Valid	1 if this track stub is valid

me2a, me2b, me2c
me3a, me3b, me3c
me4a, me4b, me4c

bit width: 24

Track stub inputs from stations 2,3,4, three stubs from each.

Table 2. ME2,3,4 input bit fields.

Bits	Name	Description
11:0	Phi	Phi of the track stub
18:12	Eta	Eta of the track stub
22:19	Q	Quality of the track stub
23	Valid	1 if this track stub is valid

mb1a, mb1b

bit width: 16

Two track stub inputs from drift tube trigger system. Data on these inputs can be serialized by DT trigger system (see FL flag in Table 3).

Table 3. MB input bit field.

Bits	Name	Description
11:0	Phi	Phi of the track stub
14:12	Q	Quality of the track stub
15	FL	FL is set to 1 if this track stub belongs to the previous BX

mnet12, mnet13, mnet23, mnet24, mnet34, mnet12ov, mnet2dt, mnet14

bit width: 7

Minimum eta for collision extrapolation units, see Table 4 for details.

mxeta12, mxeta13, mxeta23, mxeta24, mxeta34, mxeta12ov, mxeta2dt, mxeta14

bit width: 7

Maximum eta for collision extrapolation units, see Table 4 for details.

etawn12, etawn13, etawn23, etawn24, etawn34, etawn12ov, etawn14

bit width: 8

Eta windows for collision extrapolation units, see Table 4 for details.

Table 4. Control parameters for collision extrapolation units.

Extrapolation unit	Minimum Eta		Maximum Eta		Eta Window	
	Index	Default (dec)	Index	Default (dec)	Index	Default (dec)
ME1 - ME2	12	22	12	127	12	4
ME1 - ME3	13	22	13	127	13	4
ME2 - ME3	23	14	23	127	23	4
ME2 - ME4	24	14	24	127	24	4
ME3 - ME4	34	14	34	127	34	4
ME1 - ME2 overlap	12ov	14	12ov	24	12ov	4
ME2 - DT1	2dt	10	2dt	24	N/A	N/A
ME1 - ME4	14	22	14	127	14	4

mindphi

bit width: 12

Minimum phi difference for track cancellation logic, default = 128

mindeta

bit width: 5

Minimum eta difference for track cancellation logic, default = 8

mndeta_halo12, mndeta_halo13, mndeta_halo112, mndeta_halo113

bit width: 7

Minimum eta difference for halo tracks, see Table 5 for details.

mxdata_halo12, mxdata_halo13, mxdata_halo112, mxdata_halo113

bit width: 7

Maximum eta difference for halo tracks, see Table 5 for details.

mxdphi_halo12, mxdphi_halo13, mxdphi_halo112, mxdphi_halo113

bit width: 10

Maximum phi difference for halo tracks, see Table 5 for details.

Table 5. Control parameters for halo extrapolation units.

Extrapolation unit	Minimum Deta		Maximum Deta		Maximum Dphi	
	Index	Default (dec)	Index	Default (dec)	Index	Default (dec)
ME1 - ME2 (except ME1/1)	12	8	12	14	12	64
ME1 - ME3 (except ME1/1)	13	19	13	25	13	64
ME1/1 - ME2	112	19	112	25	112	64
ME1/1 - ME3	113	30	113	36	113	64

mindphi_halo

bit width: 12

Minimum phi difference for halo track cancellation logic, default = 128

mindeta_halo

bit width: 5

Minimum eta difference for halo track cancellation logic, default = 8

straight

bit width: 12

Parameter for the correction of misaligned 1-2-3-4 tracks, default = 60.

curved

bit width: 12

Parameter for the correction of misaligned 1-2-3-4 tracks, default = 200.

control

bit width: 16

Control input. Used to turn on/off various features in the core.

Table 6. Control input.

Bits	Name	Description	Default	Range
0	wide_phi	enable wider phi extrapolations	0	
3:1	BXA_depth	Depth of BXA history	2	0-2
6:4	reserved		0	
8:7	Pretrigger	Number of track segments to pre-trigger	2	1-3
15:9	reserved		0	

clk

Clock input, 40.08 MHz.

Outputs

pHp, pMp, pLp

bit width: 29

Parameters of the tracks found by the track finder on each clock cycle. pHp is the highest quality track, pLp is the lowest.

Table 7. pHp, pMp, pLp bit fields.

Bits	Name	Description
4:0	eta	Eta of the track that was found
8:5	mode	Mode parameter
9	charge	Charge of the particle
21:10	dphi	Delta Phi
22	sign	Sign
27:23	phi	Phi of the track that was found
28	FR	Front/rear flag – tells if ME1 chamber is in front of rear

PT assignment lookup memory address should be constructed as shown below:

Addr = {FR, sign, mode, eta[4:1], dphi};

idHp, idMp, idLp

bit width: 22

Numbers of the track stubs which resulted into track found by the logic. idHp shows the track stubs for pHp output, idMp for pMp, and idLp for pLp. All numbers start from 1. 0 means that no track stub from this station participated in the decision.

Table 8. idHp, idMp, idLp bit fields.

Bits	Name	Description	Range
2:0	Id1	Number of track stub from station 1	1-6
4:3	Bxd1	Track stub from station 1 delay by BXA	0-2
6:5	Id2	Number of track stub from station 2	1-3
8:7	Bxd2	Track stub from station 2 delay by BXA	0-2
10:9	Id3	Number of track stub from station 3	1-3
12:11	Bxd3	Track stub from station 3 delay by BXA	0-2
14:13	Id4	Number of track stub from station 4	1-3
16:15	Bxd4	Track stub from station 4 delay by BXA	0-2
19:17	Idb1	Number of track stub from DT station 1	1-4
21:20	Bxdb1	Track stub from DT station 1 delay by BXA	0-2

date

bit width: 16

Shows the date when this version of the core was generated from VPP model.

Table 9. Date bit fields.

Bits	Name	Description
0:6	Year	Year – 2000
11:7	Day	Day
15:12	Month	Month

MINDPHI, MINDETA

STRAIGHT, CURVED

MNDETA_HALO*, MXDETA_HALO*, MXDPHI_HALO*

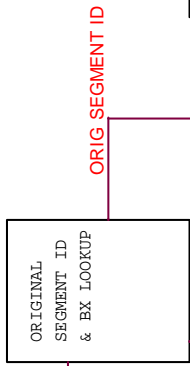
SEGMENT NUMBERS & BX

MNETA*, MXETA*, ETAWIN*

ENDCAP TRACK SEGMENT PARAMETERS: CSCID, Q, ETA, PHI

DT TRACK SEGMENT PARAMETERS: Q, PHI, FL

MINDPHI_HALO, MINDETA_HALO



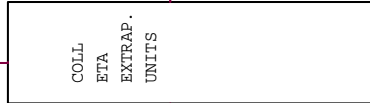
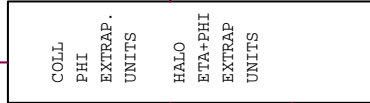
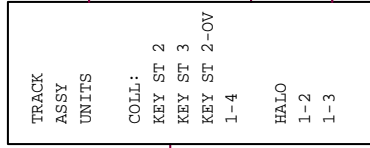
ORIG_SEGMENT ID

STUB ID

STUB ID

COLL RANK[12]

HALO RANK[6]



ETA & PHI EXTRAP. RESULTS

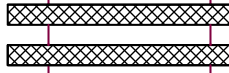
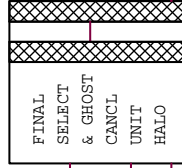
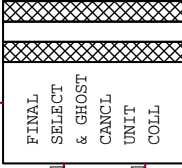
COLL ETA EXTRAP. RESULTS

TRACK SEGMENT PARAMETERS: CSCID, Q, ETA, PHI



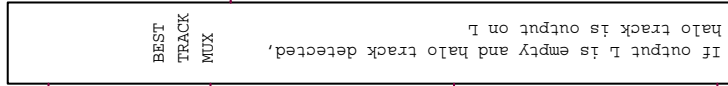
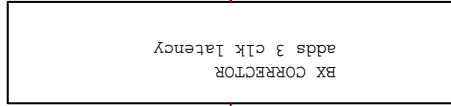
ORIG_SEGMENT ID

TRACK PARAMS PT, SIGN, MODE ETA, FR, PHI (12 COLL+6 HALO TRACKS)



BEST COLL TRACK NUM[3]

BEST HALO TRACK NUM



3 BEST TRACKS
ORIG STUB ID
ETA, FR, PHI
PT, SIGN, MODE
TRACK PARAMETERS

University of Florida
Title = SP firmware core
Schematic Name = SP_core - 2009-04-09
Page Size = A
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Schematic Path =



Mode and rank definition

Mode	Rank	Track assembler key station 2	Track assembler key station 3	Track assembler key station 4	Track assembler key station 2 to DT
0		no track			
1		bad phi road			
2	1f	1(1)-2-3-4	1(1)-2-3-4		
	12	1(1)-2-3	1(1)-2-3		
	21	1(2)-2-3-4	1(2)-2-3-4		
	17	1(2)-2-3	1(2)-2-3		
	23	1(3)-2-3-4	1(3)-2-3-4		
	1c	1(3)-2-3	1(3)-2-3		
3	11	1(1)-2---4			
	16	1(2)-2---4			
	1b	1(3)-2---4			
4	10		1(1)---3-4		
	15		1(2)---3-4		
	1a		1(3)---3-4		
5	4	2-3-4	2-3-4		
6	6	1(1)-2			1-2
	b	1(2)-2			
	e	1(3)-2			
7	5		1(1)---3		
	a		1(2)---3		
	d		1(3)---3		
8	3	2-3	2-3		
9	2	2-4			
a	1		3-4		
b		trigger on singles, impl. in wrapper			
c	13				1-2-b1(1)
	18				1-2-b1(2)
	1d				1-2-b1(3)
d	7			1(1)-----4	
	8			1(2)-----4	
	14			1(3)-----4	
e	9				2-b1(1)
	c				2-b1(2)
	f				2-b1(3)
f		halo trigger			

Explanation:

Track assembler columns show which extrapolations are used in a track.

Notation:

- numbers 1,2,3,4 mean ME stations 1,2,3,4

- b1 means DT station 1
- 1(2) means extrapolation quality to station 1 is 2.

Example:

if "1(2)-2-3-4" appears in "Track assembler key station 2" column, it means a track was built from the following extrapolations:

- ME1 to ME2 (quality 2)
- ME2 to ME3
- ME2 to ME4

Track-finding algorithm notes (see diagram)

Drift tube data deserializer

- Receives data from Drift Tube (DT) interface, analyzes FL bit.
- If FL bit is not set, delays the data by one clock.
- If FL is set, passes data without delay.

Thus, on the output, the data from the same bunch crossing are re-aligned as they should be.

Bunch Crossing Analyzer

- Receives CSC and DT track segments
- Keeps history of the segments received one and two clocks in the past
- Sorts the segments from each station based on their quality, including the segments from history (9 segments from each station total)
- Selects the segments with best quality on each BX, routes them to the outputs

Collision Eta Extrapolation Units

- Make the following Eta extrapolations: 1-2, 1-2 (DT overlap region), 1-3, 1-4
- Check that Eta is in the specified range (between min and max)
- Check that Etas from 2 analyzed stations are close to each other (within Eta window)
- Output one-bit result (true if the extrapolation was successful)

Collision Phi Extrapolation Units

- Make the following Phi extrapolations: 1-2, 1-3, 1-4, 1-2 (DT overlap region), 2-3, 2-4, 3-4, 2-DT
- Check that Phi is in the specified range (between min and max)
- Check that Phis from 2 analyzed stations are close to each other (within Phi window)
- Take Eta extrapolation results into account
- Output extrapolation quality results (2-bit for station 1 extrapolations, 1-bit for all others)

Halo Eta+Phi Extrapolation Units

- Make the following extrapolations: 1-2, 1-3 in Eta and Phi
- Check that Phi and Eta is in the specified range (between min and max)
- Check that Phis from 2 analyzed stations are close to each other (within windows)
- Check that Etas from 2 analyzed stations have difference in the specified ranges
- Output one-bit results

To be continued...

Revision history (started 2008-09-09, even though this document is way older than that)

Date	Modifications
2008-09-09	<ul style="list-style-type: none"> • added halo_delay field to control register • added wide_phi field to control register • added new but unused parameters for future implementation of Rick's corrections to 1-2-3-4 tracks: <ul style="list-style-type: none"> ○ straight

	<ul style="list-style-type: none"> ○ curved
2008-12-19	<p>modifications for 2008 upgrade</p> <ul style="list-style-type: none"> • halo: <ul style="list-style-type: none"> ○ extrapolations 1-2 and 1-3 added ○ halo reports eta and phi ○ halo track may be reported on any output ○ eta and phi cancellation • 12-bit phi cancellation • Eta cancellation • Rick's corrections for 1-2-3-4 tracks • 1-4 extrapolations for collisions • removed unused mmeta, mxeta inputs (left from barrel station 2) • removed halo_delay from control input, implemented in wrapper • Unused bits removed from: <ul style="list-style-type: none"> ○ ME2,3,4 inputs ○ idHp, idMp, idLp outputs
2009-03-25	<ul style="list-style-type: none"> • mmeta, mxeta, etawn parameters renamed to reflect better their purpose • similar parameters for halo muons also renamed • added separate halo parameters (mndeta, mxdeta, mxdphi) for ME1/1 extrapolations
2009-04-09	<ul style="list-style-type: none"> • Added descriptions of mindphi_halo, mindeta_halo parameters. • Added block-schematics
2009-07-28	<ul style="list-style-type: none"> • Added mode and rank definition table • Added partial algorithm notes