Modular Track Finder

Base board specification (Draft)

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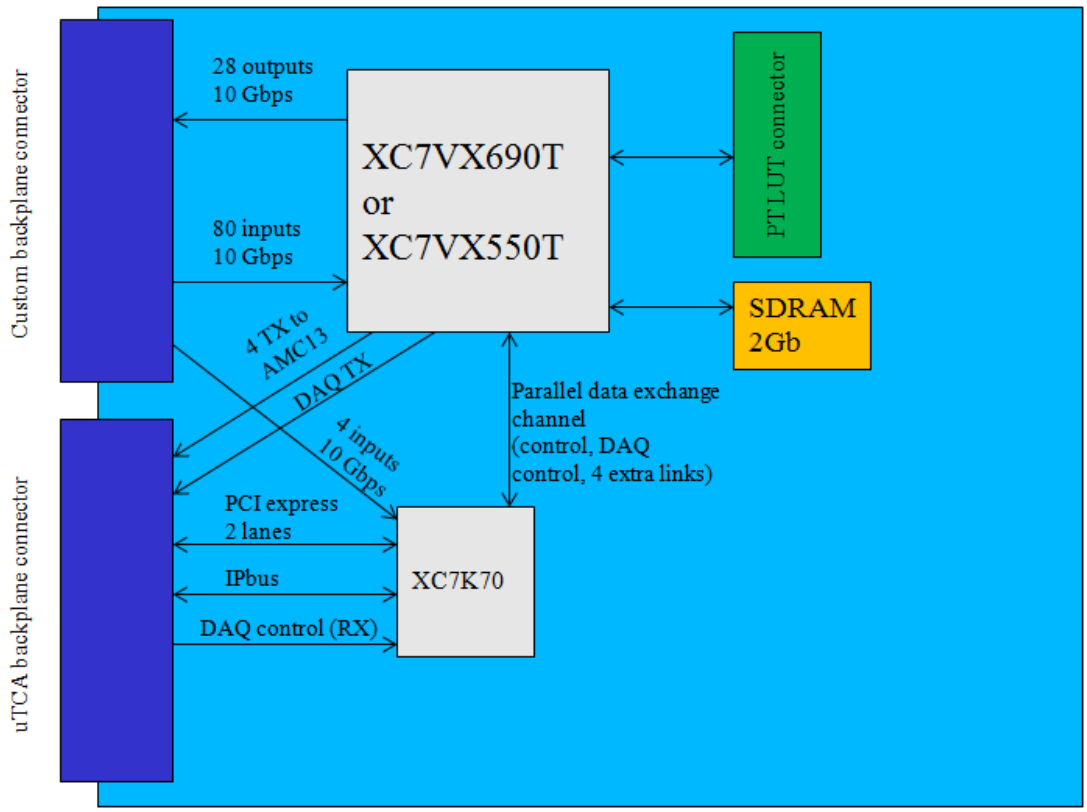


Figure 1 Simplified block structure of MTF7 base board

Multi-Gigabit Serial communications

Description	Link count	From	To	Max rate, Gbps
Trigger data inputs	80	Optical board	Core Logic FPGA	10
Trigger data inputs	4	Optical board	Control FPGA	10
Trigger data outputs	28	Core Logic FPGA	Optical board	10
General purpose outputs	4	Core Logic FPGA	AMC13	10
DAQ	1	Core Logic FPGA	AMC13	10
DAQ	1	AMC13	Control FPGA	10
PCI express	2	MCH	Control FPGA	5

PCI express	2	Control FPGA	MCH	5
IP bus	1	MCH	Control FPGA	1
IP bus	1	Control FPGA	MCH	1

Table 1 Multi-Gigabit Serial communications

Connection between Core Logic and Control FPGAs

Wire count	Bank voltage	Suggested signaling standard
100	1.2V	Bidirectional LVCMOS, source termination

Table 2 Core Logic to Control FPGA connection

Connection between Core Logic FPGA and Pt LUT

Wire count	Bank voltage	Suggested signaling standard
168	1.2V	Bidirectional LVCMOS, source termination

Table 3 Core Logic FPGA to Pt LUT connection

On board SDRAM

Partnumber	MT41K256M8DA
Capacity	2Gb
Organization	256 M x 8 bits
FPGA pin assignment verified	Xilinx Memory Interface Generator v1.9

Table 4 SDRAM

Clocking

Input bank/pin	Synchronous to LHC clock	Frequency	Derived from	Purpose	Dejittered
GTH bank 110, clk 1	Yes	641.28 MHz	LHC clock	Trigger data RX/TX	Yes
GTH bank 113, clk 1	Yes	641.28 MHz	LHC clock	Trigger data RX	Yes
GTH bank 116, clk 1	Yes	641.28 MHz	LHC clock	Trigger data RX/TX	Yes
GTH bank 118, clk 1	Yes	641.28 MHz	LHC clock	Trigger data RX/TX	Yes
GTH bank 211, clk 1	Yes	641.28 MHz	LHC clock	Trigger data RX	Yes
GTH bank 213, clk 1	Yes	641.28 MHz	LHC clock	Trigger data RX	Yes
GTH bank 216, clk 1	Yes	641.28 MHz	LHC clock	Trigger data RX	Yes
GTH bank 218, clk 1	Yes	641.28 MHz	LHC clock	Trigger data RX	Yes
GTH bank 111, clk 0	No	250 MHz	Oscillator	Trigger data RX/TX	Yes
GTH bank 113, clk 0	No	250 MHz	Oscillator	Trigger data RX	Yes
GTH bank 116, clk 0	No	250 MHz	Oscillator	Trigger data RX/TX	Yes
GTH bank 118, clk 0	No	250 MHz	Oscillator	Trigger data RX/TX	Yes
GTH bank 211, clk 0	No	250 MHz	Oscillator	Trigger data RX	Yes
GTH bank 213, clk 0	No	250 MHz	Oscillator	Trigger data RX	Yes

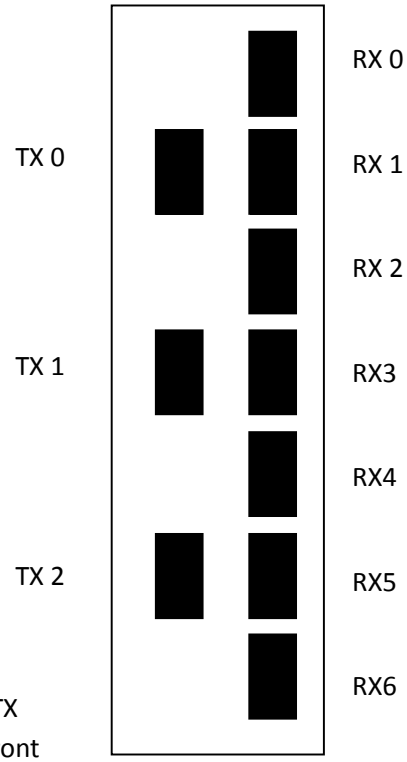
GTH bank 216, clk 0	No	250 MHz	Oscillator	Trigger data RX	Yes
GTH bank 218, clk 0	No	250 MHz	Oscillator	Trigger data RX	Yes
I/O bank 24, pin AU18, LVCMOS12	Yes	40.08 MHz	LHC clock	Trigger logic clocking	Yes

Table 5 Core Logic FPGA clocks

Input bank/pin	Synchronous to LHC	Frequency	Derived from	Purpose	Dejittered
GTX bank 116, clk 0	No	250 MHz	Oscillator	PCIe, DAQ RX	Yes
GTX bank 115, clk 0	Yes	641.28 MHz	LCH clock	Trigger data RX	Yes
I/O bank 34, pins AB2, AC2	No	Depends on system	TCLKA	Telecom clock A	No
I/O bank 34, pins AC4, AC3, LVDS	No	Depends on system	TCLKC	Telecom clock C	No
I/O bank 34, pins AA4, AB4, LVDS	Yes	40.08 MHz	LHC clock	LHC clock	No
I/O bank 15, pins F17, E17, LVDS	Yes	40.08 MHz	LHC clock	LHC clock	Yes

Table 6 Control FPGA clocks

GTH RX, TX mapping and inversion



Mapping of the RX and TX units on Optical board front panel

GTH Quad	GTH Quad Channel	Optical RX unit	Optical RX channel	RX inversion	Optical TX unit	Optical TX channel	TX inversion	Async clock quad	Async clock input	Sync clock quad	Sync clock input
110	0	6	4					111	0	110	1
110	1	6	5					111	0	110	1
110	2	6	0	x				111	0	110	1
110	3	6	1	x				111	0	110	1
111	0	5	8	x				111	0	110	1
111	1	5	9	x				111	0	110	1
111	2	5	5					111	0	110	1
111	3	5	4	x				111	0	110	1
112	0	5	1	x				113	0	113	1
112	1	5	0	x				113	0	113	1
112	2	4	8	x				113	0	113	1
112	3	4	9	x				113	0	113	1
113	0	4	4					113	0	113	1
113	1	4	5					113	0	113	1
113	2	4	0	x				113	0	113	1
113	3	4	1	x				113	0	113	1
114	0	3	8	x				113	0	113	1
114	1	3	9	x				113	0	113	1
114	2	3	5					113	0	113	1
114	3	3	4					113	0	113	1
115	0	3	1	x				116	0	116	1
115	1	3	0					116	0	116	1
115	2	2	9	x				116	0	116	1
115	3	2	8	x				116	0	116	1
116	0	2	5		2	10	x	116	0	116	1
116	1	2	4		2	11		116	0	116	1
116	2	2	1	x	2	6	x	116	0	116	1
116	3	2	0		2	7		116	0	116	1
117	0	1	9	x	2	2		116	0	116	1
117	1	1	8	x	2	3	x	116	0	116	1
117	2	1	5		1	7	x	116	0	116	1
117	3	1	4		1	9	x	116	0	116	1
118	0	1	1	x	2	8	x	118	0	118	1
118	1	1	0		2	9	x	118	0	118	1
118	2	0	9	x	2	4		118	0	118	1
118	3	0	8	x	2	5		118	0	118	1
119	0	0	5	x	2	0	x	118	0	118	1
119	1	0	1		2	1		118	0	118	1
119	2	0	4		1	5	x	118	0	118	1
119	3	0	0		1	2		118	0	118	1

GTH Quad	GTH Quad Channel	Optical RX unit	Optical RX channel	RX inversion	Optical TX unit	Optical TX channel	TX inversion	Async clock quad	Async clock input	Sync clock quad	Sync clock input
210	0	6	7					211	0	211	1
210	1	6	6	x				211	0	211	1
210	2	6	2					211	0	211	1
210	3	6	3					211	0	211	1
211	0	5	11					211	0	211	1
211	1	5	10	x				211	0	211	1
211	2	5	6	x				211	0	211	1
211	3	5	7	x				211	0	211	1
212	0	5	2					211	0	211	1
212	1	4	11					211	0	211	1
212	2	5	3					211	0	211	1
212	3	4	10	x				211	0	211	1
213	0	4	7					213	0	213	1
213	1	4	6	x				213	0	213	1
213	2	4	2					213	0	213	1
213	3	4	3					213	0	213	1
214	0	3	11					213	0	213	1
214	1	3	7					213	0	213	1
214	2	3	10	x				213	0	213	1
214	3	3	3	x				213	0	213	1
215	0	3	6	x				216	0	216	1
215	1	2	11					216	0	216	1
215	2	3	2					216	0	216	1
215	3	2	7					216	0	216	1
216	0	2	10	x				216	0	216	1
216	1	2	3	x				216	0	216	1
216	2	2	6	x				216	0	216	1
216	3	1	11					216	0	216	1
217	0	2	2		0	3	x	218	0	218	1
217	1	1	7		0	2	x	218	0	218	1
217	2	1	10	x	0	1		218	0	218	1
217	3	1	3	x	0	0	x	218	0	218	1
218	0	1	6	x	0	5	x	218	0	218	1
218	1	0	11		0	4		218	0	218	1
218	2	1	2		0	9		218	0	218	1
218	3	0	7		0	8	x	218	0	218	1
219	0	0	10		0	7	x	218	0	218	1
219	1	0	6		0	6	x	218	0	218	1
219	2	0	3	x	0	10	x	218	0	218	1
219	3	0	2	x	0	11	x	218	0	218	1

Table 7. GTH RX, TX mapping and inversion

JTAG

Input 1	Front panel connector, compatible with Xilinx Platform cable
Input 2	uTCA backplane
Input selection	Automatic: uTCA by default, cable is activated when connected and used.
Devices in chain	Control FPGA Core Logic FPGA (with bypass switch) Pt LUT module (with bypass switch)
Cable power voltage	3.3V
Internal JTAG chain signaling voltage	1.8V

Table 8 JTAG chain 1

Input	Front panel connector, compatible with Atmel ICE3 cable
Devices in chain	MMC CPU
Cable and JTAG chain voltage	3.3V

Table 9 JTAG chain 2

FPGA configuration

Memory type	PC28F00AP30TFA
Memory size	1Gb
Memory connected to	Control FPGA
Memory writable from	PCI express Xilinx JTAG cable uTCA JTAG
Core Logic FPGA configuration	By Control FPGA, via dedicated bus.
Core Logic FPGA bitstream storage	1. PC28F00AP30TFA memory (same chip that holds Control FPGA bitstream) 2. Micro-SD card (on front panel)

Table 10 FPGA configuration details

Revision history

Date	Comment
2014-05-20	Initial creation
2014-07-07	Added GTH mapping to optical links, reworked clocking table according to

	modifications on prototype