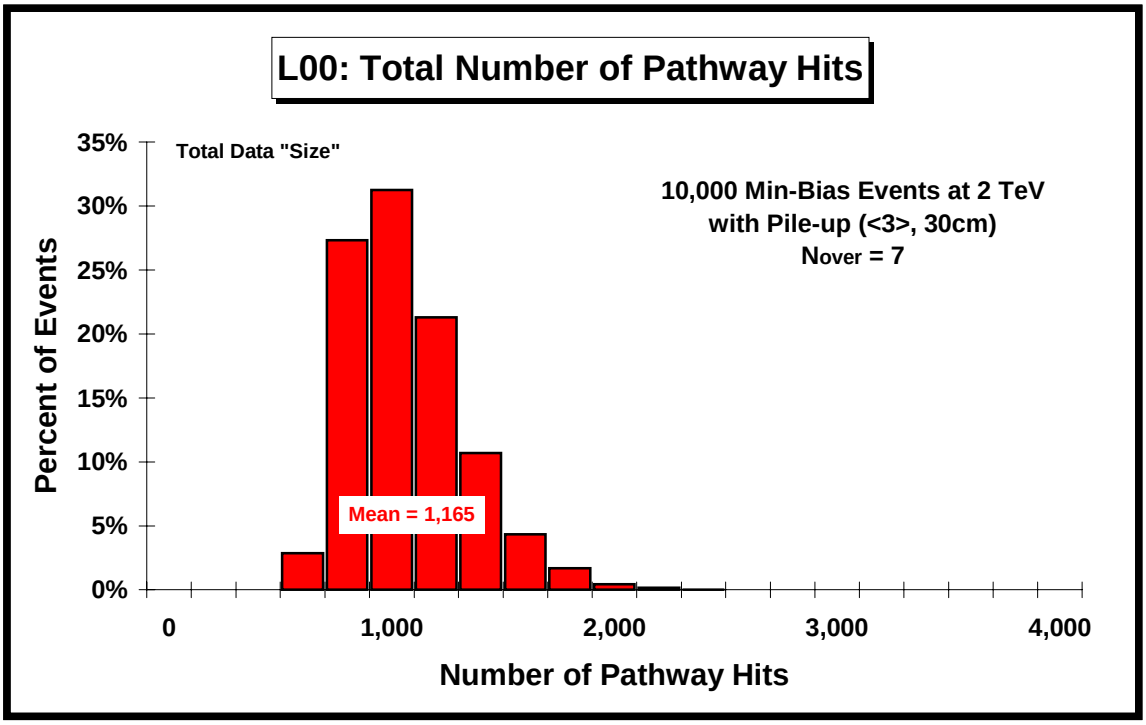
Min-Bias Occupancy Study of Layer 00

Average total chip hits and average hits per chip for the six distinct chip types for 10,000 min-bias events with pile-up (<3> min-bias, σ_z= 30cm) assuming 1.6% noise (N_{over} = 7).

Layer 00: Average Total Chip Hits						<3> Min-Bias	
Radius	Forward	Middle	Central	Central	Middle	Forward	sum
inner	60	67	73	73	68	60	**401**
outer	116	128	137	138	129	116	**764**
sum	**176**	**196**	**210**	**211**	**197**	**176**	**1,165**
Layer 00: Average Hits/Chip							
Radius	Forward	Middle	Central	Central	Middle	Forward	all
inner	10	11	12	12	11	10	**11**
outer	10	11	11	11	11	10	**11**
all	**10**	**11**	**12**	**12**	**11**	**10**	**11**

Distribution of the total number of readout pathway (HDI) hits in layer 00 for min-bias events at 2 TeV with pile-up (<3> min-bias, σ_z= 30cm) assuming 1.6% noise (N_{over} = 7).



Min-Bias Occupancy Study of Layer 00

Average maximum chip hits for the six distinct chip types for 10,000 min-bias events with pile-up (<3> min-bias, σ_z= 30cm) assuming 1.6% noise (N_{over} = 7).

	Layer 00: Average Maximum Chip Hits					<3> Min-Bias	
	Forward	Middle	Central	Central	Middle	Forward	all
inner	14	16	18	18	17	14	
outer	16	18	19	20	18	16	
all							29

Distribution of the number of "hits" in layer 00 chip with maximum hits per event for min-bias events at 2 TeV with pile-up (<3> min-bias, σ_z= 30cm) assuming 1.6% noise (N_{over} = 7).