Components for Generating and Phase Locking 390-GHz Signal in 45-nm CMOS*

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Abstract

Components for generating and phase locking 390-GHz signal are demonstrated using low leakage transistors in 45-nm CMOS. An integrated chain of circuits composed of an 195-GHz oscillator with frequency doubled output at ~390 GHz followed by two cascaded ÷2 injection locked frequency dividers with output frequency of ~49 GHz is demonstrated. The peak power radiated at ~390 GHz by an on-chip antenna is ~2 µW. The oscillator and frequency divider consumes 21 and 6 mW, respectively.

Keywords: CMOS, sub-millimeter wave, phase locking, oscillator, injection locked frequency divider, on-chip antenna

Introduction

Improvements in high frequency capability of CMOS have made it possible to consider CMOS as an alternate means for implementing sub-millimeter wave systems [1]. A signal generation circuit is a key component for sub-millimeter wave systems and several CMOS oscillators that generate signals in the frequency range have been demonstrated [1]-[3]. The free-running oscillators should be phase-locked to generate stable and high spectral purity signals essential in many sub-millimeter wave applications. One of the most challenging blocks for phase locking in this frequency range is implementing the first frequency divider stage. An injection locked frequency divider (ILFD) operating around 200 GHz has been reported as a stand-alone component driven by an external signal source [4]. This paper reports for the first time an integrated chain of oscillator with frequency doubled output at ~390 GHz and two cascaded injection locked frequency divide-by-two circuit stages with an output around 49 GHz (Fig. 1). Quasi-optical measurements using an on-chip antenna demonstrated that the oscillator generates a signal near 390 GHz with the power level of ~2.2 µW. The circuit is implemented using low leakage transistors in a 45-nm logic CMOS technology.

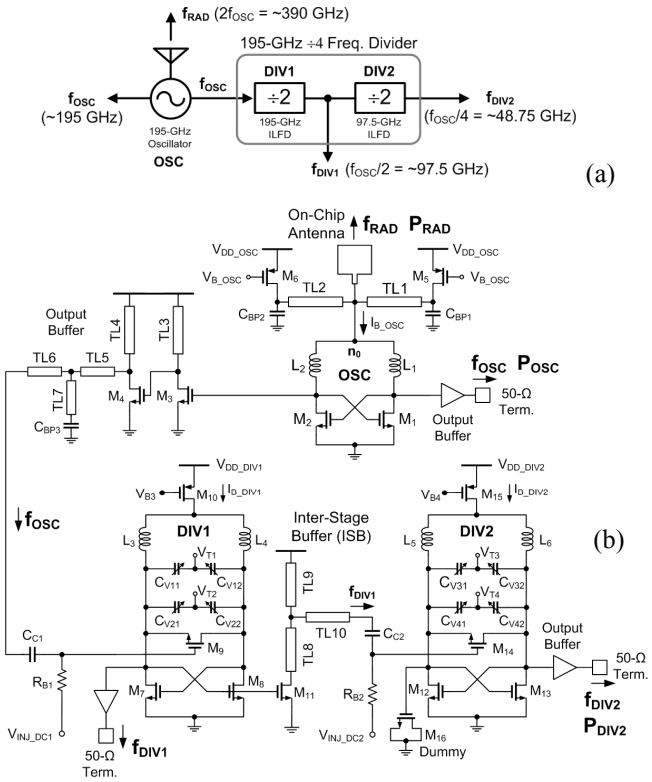

Fig. 1 Block diagram (a) and circuit schematic (b) of component chain for 390-GHz phase locked loop.

Circuit Design

Fig. 1 shows a block diagram (a) and schematic of oscillator and frequency divider chain (b). The oscillator (OSC) consists of an LC tank with a cross coupled NMOS transistor pair operating around 195 GHz with a push-push output [1] around 390 GHz. The core transistor width is 9.5 µm. An output of OSC is buffered and ac coupled to the input of the following ÷2 frequency divider (DIV1). An LC-based direct ILFD is employed due to its high-frequency capability and wide locking range at low power consumption [5]. The simulated voltage gain between the OSC output and input of DIV1 is ~0.7. The width of buffer transistors, M_3 and M_4, is 3 and 9 µm, respectively. The transmission lines are implemented using grounded coplanar wave guides (GCPW) [1]. The free-running oscillation frequency of DIV1 is around 97.5 GHz. The input signal to DIV1 drives the gate of switch transistor (M_9) to inject signal directly into the LC tank [5]. The width of inter-stage buffer transistor (M_{11}) is 3 µm. The circuit configuration of DIV2 is the same as DIV1 with free-running oscillation frequency of ~49 GHz.

The inductors are implemented as a single loop using the top copper layer (Metal 7). The dividers include two binary

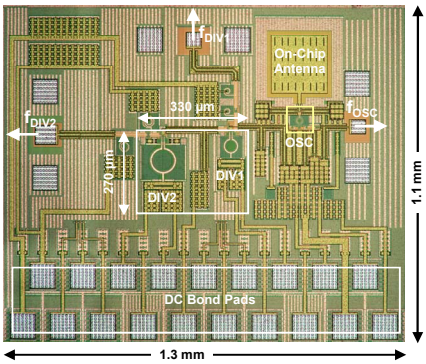

Fig. 2 Die photograph.

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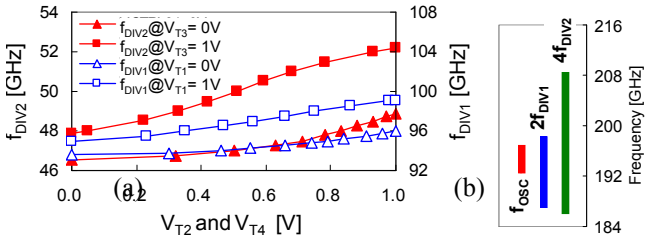

Fig. 3 (a) Free-running oscillation frequency range of injection locked frequency dividers. (b) Comparison of tuning range of OSC and self-oscillation frequency range of the dividers referred to the input frequency of divider chain.

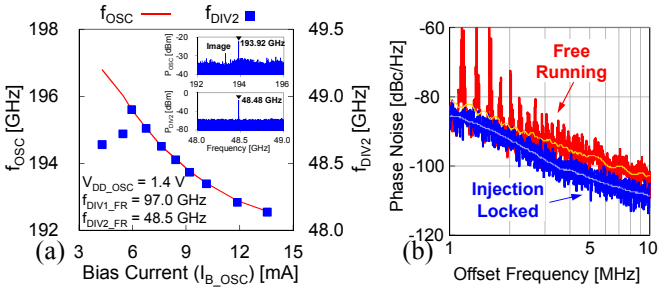

Fig. 4 (a) Output frequency of DIV2 and OSC (f_{DIV2} and f_{OSC}) versus bias current (I_{B_OSC}). (Inset) Output spectra at the output of OSC and divider chain. (b) Phase noise of output of DIV2 with and without input signal to the divider chain.

weighted MOS varactors (CV_{11}–CV_{42}) for frequency tuning/ alignment. The varactors are formed with 110-nm long and 0.7-µm wide fingers. The on-chip microstrip patch antenna was formed using an aluminum bond pad layer [1]. The patch size is 185x180 µm^2. Fig. 2 shows the die photograph of chain. The circuit occupies 1.1x1.3 mm^2 including the areas for bond pads. The thickness of top copper and pad layer is ~2 and ~1 µm, respectively. The total dielectric layer thickness under the top metal layer is ~2.5 µm.

Measurement Results

Fig. 3(a) shows the free-running frequency range of dividers as function of control voltage for C_{V21}, C_{V22}, C_{V41}, and C_{V42} when the control voltage for the other varactors is zero and one. Fig. 3(b) compares the fundamental frequency tuning range of OSC, and free-running oscillation frequency range of DIV1 and DIV2 referred to the input of divider chain. f_{OSC} is varied by changing the OSC bias current, I_{B_OSC}. The figure demonstrates that the frequency dividers should be able to divide the output of OSC assuming that the signal levels at the divider inputs are sufficient. Harmonic mixers and millimeter-wave probes were used for the measurements. The locking range of frequency divider in Fig. 4(a) is measured by changing f_{OSC}. The free-running oscillation frequency of DIV1 and DIV2 (f_{DIV1_FR} and f_{DIV2_FR}) is set at 97.0 and 48.5 GHz by appropriately biasing the varactors. The bias voltages of injection transistors (M_9 and M_{14}), V_{INJ_DC1} and V_{INJ_DC2}, are 1.0 V. As I_{B_OSC} is increased from 4.3 to 13.5 mA, f_{OSC} is tuned from 196.8 to 192.5 GHz. Insets in the figure show the output spectrum of OSC and DIV2. The integrated chain is locked from 192.6 to 195.6 GHz. For frequencies above, the dividers fail to divide-by-four. The locking range is limited by the reduced output power at the high end, and the lower frequency limit of oscillator at the low end.

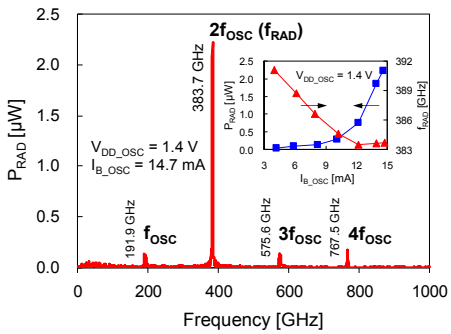

Fig. 5 Measured spectrum of frequency doubled output near 390 GHz. (Inset) Measured radiated power (P_{RAD}) and radiation frequency (f_{RAD}) versus bias current (I_{B_OSC}).

Fig. 4(b) shows the measured output phase noise of divider chain with and without the input signal to the chain. The phase noise improves by ~4–7 dB when the divider locks. The phase noise of frequency divider chain output is –86 and –109 dBc/Hz at 1 MHz and 10 MHz offset, respectively. This means the phase noise at 390 GHz should be lower than –68 and –91 dBc/Hz at the offset frequencies. Fig. 5 plots the spectrum of frequency doubled output measured using a Fourier Transform Infrared Spectrometer and a silicon bolometer [1]. The radiated power through the on-chip antenna connected to the oscillator is 2.2 µW at 383.7 GHz. This is more than 100X higher than that of 410-GHz signal generation circuit fabricated in the same process [1]. This is due to better tuning of the antenna to the radiation frequency (f_{RAD}), ~30% higher bias current (I_{B_OSC}), and use of metal-oxide-metal bypass capacitors instead of MOS ones [1]. The unwanted harmonics are suppressed to more than 10 dB below the intended 2nd order harmonic output. The inset shows the measured radiated power and frequency versus bias current. The output frequency of oscillator at given bias is shifted down because the measurement temperature inside the FTIR is ~8 °C higher than the room temperature at which the entire chain has been characterized. The frequency dividers including the inter-stage buffer (ISB) consumes 6 mW from a 1-V supply, while the OSC core consumes 21 mW from a 1.4-V supply.

Based on the performance of 60-GHz static divider fabricated using low leakage transistors of a 65-nm CMOS process [6], it should be straight forward to realize a 50-GHz buffer and a static frequency divider in the 45-nm process, and cascaded with the dividers from this paper to lock the 390-GHz signal. This will be ~4X the highest signal phase locked in silicon IC's. Furthermore, it should be possible to lock ~553-GHz signal generated using a quadruple-push oscillator with fundamental oscillation frequency of ~138 GHz [3].

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