

## SP02 Backplane Interfaces

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This doc matches `vm_fa_dd_040601.evf` and `sp_040601.evf` configuration files.

### CCB Interface

The CCB interface provides the SP02 with timing and trigger control signals distributed by the Clock and Control Board (CCB) over the backplane [i]. The backplane counts as many as 34 signal lines coming in and going out of the SP02. Table 1 arranges backplane signals into four Groups. All GTLP lines are active LOW (negative bus logic).

**Table 1: SP02 CCB Interface Signals.**

Signal	Lines	Direction	Type	Logic	Duration	Usage
<b>Clock Group</b>						
CCB_CLK	2	IN	Point-to-point	LVDS	40MHz	Used
CCB_CLK_EN	1	IN	Bussed	GTLP	Pulse, n counts	Not used
<b>Subtotal</b>	<b>3</b>					
<b>Fast Control Group</b>						
CCB_CMD [5..0]	6	IN	Bussed	GTLP	Level	Used
CCB_ECRES	1	IN	Bussed	GTLP	25ns	Used
CCB_BCRES	1	IN	Bussed	GTLP	25ns	Used
CCB_CMD_STR	1	IN	Bussed	GTLP	25ns	Used
CCB_BX0	1	IN	Bussed	GTLP	25ns+ECL FP	Not Used
CCB_LIACC	1	IN	Bussed	GTLP	25ns+ECL FP	Used
CCB_DAT [7..0]	8	IN	Bussed	GTLP	Level	Used
CCB_DAT_STR	1	IN	Bussed	GTLP	25ns	Used
CCB_RDY	1	IN	Bussed	GTLP	Static level	Used
<b>Subtotal</b>	<b>21</b>					
<b>Reload Group</b>						
CCB_SP_HRES	1	IN	Bussed	GTLP	400ns	Used
SP_CFG_DONE	1	OUT	Point-to-Point	GTLP	Level	Used
<b>Subtotal</b>	<b>2</b>					
<b>Reserved Group</b>						
CCB_RSVD [3..0] <sup>1</sup>	4	IN	Bussed	GTLP	25ns	Used
SP_RSVD [3..0] <sup>2</sup>	4	OUT	Bussed	GTLP	25ns	Used
<b>Subtotal</b>	<b>8</b>					
<b>Total</b>	<b>34</b>					

The Clock Group includes differential clock and clock enable lines. The SP02 uses the CCB\_CLK signal as a reference for its on-board QPLL. The 40 MHz QPLL output after de-

<sup>1</sup> CCB\_RSVD3 is assigned for CCB\_L1RES – L1 Reset signal resets L1 buffers and resynchronizes optical links.

<sup>2</sup> SP\_RSVD3 is assigned for SP\_L1REQ – L1 request, local trigger generated by the SP\_FPGA logic.

skewing drives each of the SP02 FPGA. The 80 MHz QPLL output delivers a reference clock to GTX\_CLK pins of the TLK2501 serializers / deserializers. The SP02 never uses the CCB\_CLK\_EN signal.

The Fast Control Group includes a CCB\_RDY status line, TTCrx command and data busses with strobes, and a few TTCrx signals, decoded by the CCB. The Fast Control Group signals are valid when and only when the CCB\_RDY is LOW. The SP02 does not use any of the decoded TTCrx signals.

The Reload Group includes a CCB\_SP\_HRES (Hard Reset) signal for reconfiguration of the SP02 FPGAs and a SP\_CFG\_DONE (Configuration Done) status line the SP02 returns to the CCB.

The Reserved Group is only partially specified at the moment, see footnotes to Table 1.

The VME\_FPGA delivers fast control signals to every SP02 FPGA via a 6-bit Fast Control (FC) bus<sup>3</sup>. Table 2 sets correspondence between the FC and CCB signals.

**Table 2: Correspondence between the backplane and SP02 Internal Fast Control Bus Signals**

CCB Command Description	CCB Backplane Signal or Command Code	TTCvi Broadcast command data	Internal Condition	Fast Control Bus Command Code
<b>Dedicated Lines</b>				
L1 Accept	ccb_llacc		L1A_FSM in L1A_RUN state and not WOF	fc_cmd[5] or FC_L1STR
L1 Accept	ccb_llacc		L1A_FSM in L1A_RUN state	fc_cmd[4] or FC_L1ACC
L1 Accept	ccb_llacc		If enabled by VM/MA/CSR_SFC	fc_cmd[3] or FC_SFRUN
Inject Test Pattern into TMB	ccb_cmd[5:0]=0x24 or CCB_TPTMB	0x90	If enabled by VM/MA/CSR_SFC	fc_cmd[3] or FC_SFRUN
Inject Test Pattern into MPC	ccb_cmd[5:0]=0x30 or CCB_TPMPC	0xC0	If enabled by VM/MA/CSR_SFC	fc_cmd[3] or FC_SFRUN
Inject Test Pattern into SP	ccb_cmd[5:0]=0x2F or CCB_TPSP	0xBC	If enabled by VM/MA/CSR_SFC	fc_cmd[3] or FC_SFRUN
<b>Encoded Commands</b>				
No command / Idle state	ccb_cmd[5:0]=0x00 or CCB_NOCMD	0x00	Unconditional	fc_cmd[2:0]=0x0 or FC_NOCMD
Bunch Counter Reset	ccb_cmd[5:0]=0x32 or CCB_BXRES	0xC8	Unconditional	fc_cmd[2:0]=0x1 or FC_BXRES
Event Counter Reset	CCB_ECRES or CCB_BERES	0x02 0x03	Unconditional	fc_cmd[2:0]=0x2 or FC_ECRES
L1 Reset – Resets L1 Buffers and Resynchronizes Optical Links	ccb_cmd[5:0]=0x03 or CCB_L1RES	0x0C	Unconditional	fc_cmd[2:0]=0x3 or FC_L1RES
Bunch Crossing Zero Mark	ccb_cmd[5:0]=0x01 or CCB_BC0	0x04	Unconditional	fc_cmd[2:0]=0x4 or FC_BC0
Start Data Taking	ccb_cmd[5:0]=0x06 or CCB_L1STT	0x18	Unconditional	fc_cmd[2:0]=0x5 or FC_L1STT
Stop Data Taking	ccb_cmd[5:0]=0x07 or CCB_L1STP	0x1C	Unconditional	fc_cmd[2:0]=0x6 or FC_L1STP
Inject Test Pattern into SP	ccb_cmd[5:0]=0x2F or CCB_TPSP	0xBC	Unconditional	fc_cmd[2:0]=0x7 or FC_TFRUN

The FC bus consists of three dedicated lines and three lines for encoded fast control commands. Three dedicated lines are: L1 Accept (FC\_L1ACC), L1 Strobe (FC\_L1STR) and one

<sup>3</sup> The fc\_cmd[5] line of the Fast Control bus is a former clk\_en signal.

line for triggering Spy FIFOs (FC\_SFRUN). Signals on dedicated lines may coincide with encoded commands, while encoded commands are mutually exclusive.

Note, that data taking is stopped on power-up, so backplane CCB\_L1ACC signals don't pass to the FC\_L1ACC line. A sequence of CCB\_L1STT and CCB\_BC0 commands should be issued to let L1 Accepts pass to the internal FC bus, see Figure 1 for details on the L1Accept Finite State Machine (L1A\_FSM). A CCB\_L1STP command returns the L1A\_FSM from L1A\_RUN state into default L1A\_STOP state. Besides, CCB\_L1RES or CCB\_BXRES commands return it into L1A\_STOP state unconditionally.

A CCB\_L1ACC signal is passed to the FC\_L1ACC line if the L1A\_FSM is in L1A\_RUN state. The FC\_L1ACC signal is used to increment event counter.

A CCB\_L1ACC signal is passed to the FC\_L1STR line if the L1A\_FSM is in L1A\_RUN state and warning of overflow is false. Coincidence of FC\_L1STR and FC\_L1ACC initiates a data readout process.

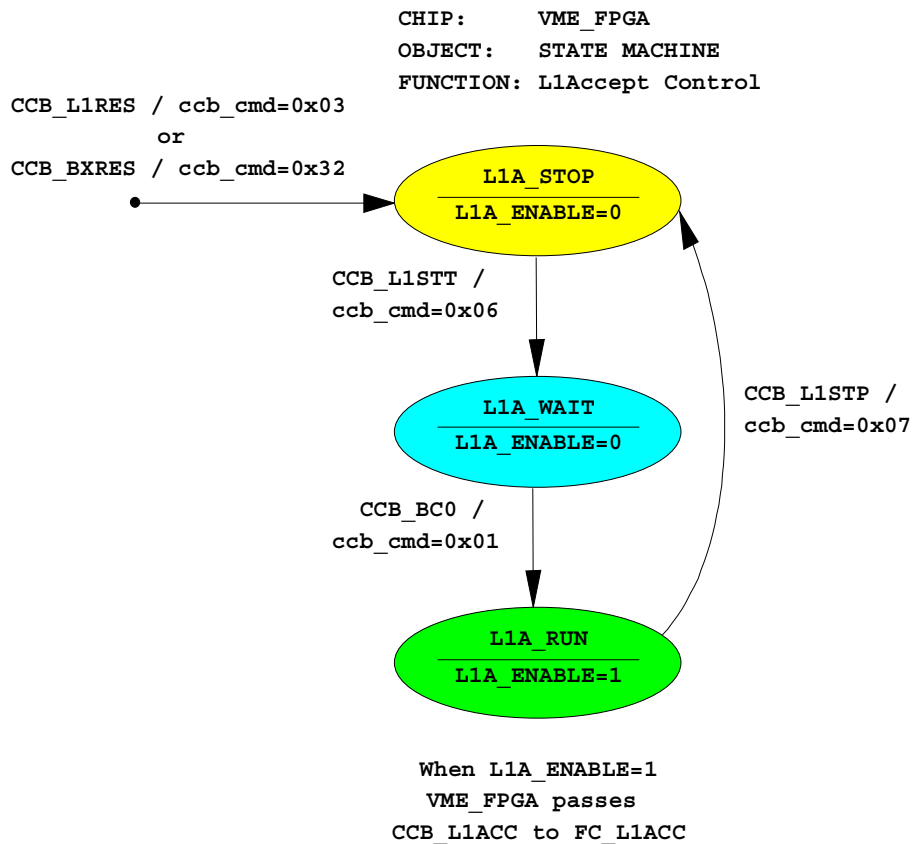


Figure 1: Finite State Machine for L1Accept Control

A FC\_SFRUN internal command requests storing data into the Spy FIFO(s). For a list of events that trigger the FC\_SFRUN command see the CSR\_SFC register description.

Summary of run control fast control commands:

- CCB\_ECRES and CCB\_BERES – resets Event counter and Valid Pattern Counters (see the DAT\_VPC register description for detail) ;
- CCB\_L1RES – returns the L1A\_FSM into L1A\_STOP state, resets Bunch counters into 0xFFE = 4094, resynchronizes optical links, resets readout buffers, resets Event counter and Valid Pattern Counters;
- CCB\_BXRES – returns the L1A\_FSM into L1A\_STOP state and resets Bunch counters to 0xFFE = 4094;
- CCB\_L1STT – pushes the L1A\_FSM into L1\_WAIT state, if it is in L1\_STOP state;
- CCB\_L1STP – returns the L1A\_FSM into L1A\_STOP state;
- CCB\_BC0 – pushes the L1A\_FSM into L1\_RUN state, if it is in L1\_WAIT state.

L1\_RUN state serves as a gate signal for Valid Pattern Counters in the FRONT\_FPGA and SP\_FPGA, see the DAT\_VPC register description for detail.

L1\_STOP state serves as a gate signal for training pattern generation to facilitate timing in the MS receive clock versus SP02 data.

The current state of the SP02 logic can be monitored with four fast monitoring status signals: busy (FM\_BSY), ready (FM\_RDY), warning-of-overflow (FM\_WOF), and out-of-synch (FM\_OSY). Each SP02 FPGA reports its 4-bit status to the VME\_FPGA. The VME\_FPGA is capable of masking individual statuses when providing the SP02 overall status to the RJ45 connector and front panel indicators (LEDs). See the following registers description on fast monitoring status detail: CSR\_BSY – Busy Control / Status, CSR\_RDY – Ready Control / Status, CSR\_WOF – Warning-of-OverFlow Control / Status, and CSR\_OSY – Out-of-Synch Control / Status.

**Table 3: SP02 LED Panel**

Description	Left LED Name	Left LED Color	Right LED Color	Right LED Name	Description
Busy	BSY	Red	Green	5.0V_OK	5.0V power is OK
Ready	RDY	Green	Green	3.3V_OK	3.3V power is OK
Warning-of-OverFlow	WOF	Red	Green	2.5V_OK	2.5V power is OK
Out-of-Synch	OSY	Red	Green	1.5V_OK	1.5V power is OK
Local Charged Trigger	LCT	Yellow	Yellow	L1ACC	L1 Accept

The LED indicators are located above the F5 link transceivers. The BSY, RDY, WOF, and OSY indicators display status of the corresponding signal lines. The L1ACC LED blinks for 25 ms on every CCB\_L1ACC. The LCT LED blinks for 25 ms on every LCT found by the SP\_FPGA.

Former Power\_OK indicators have changed their assignment and now visualize the L1A\_FSM states and lock condition of the on-board QPLL.

- 5.0V\_OK => FSM is in L1\_RUN state;
- 3.3V\_OK => FSM is in L1\_WAIT state;
- 2.5V\_OK => FSM is in L1\_STOP state;
- 1.5V\_OK => On-board QPLL locked to the backplane clock.

## VME Interface

The SP02 card includes two A24D16 Slave interfaces [ii] implemented in the VME\_FPGA and CPLD\_FPGA accordingly. Table 4 shows all address modifiers, the SP02 responds to during the VME Data Transfer Bus (DTB) cycles.

**Table 4: SP02 Address Modifier Codes.**

AM	AM Description	Access Description	Interface Chip
39	A24 non privileged data access	Access to all locations, except the BLT Mapping Registers	VME_FPGA
3A	A24 non privileged program access	Access to the BLT Mapping Registers	
3B	A24 non privileged block transfer (BLT)	BLT access using the BLT Mapping Registers	
3D	A24 supervisory data access		VME_CPLD
3E	A24 supervisory program access		
3F	A24 supervisory block transfer (BLT)		

## Auxiliary VME Interface

The auxiliary VME\_CPLD interface is intended for board configuration and provides access solely for the Bus Scan Controller (BSC). The BSC drives three chains of JTAG-compatible devices, see Table 5:

- Chain 0 consists of the SP\_FPGA and its EEPROMs;
- Chain 1 includes the VME\_FPGA with EEPROM, the FRONT\_FPGAs with EEPROMs, and the DDU\_FPGA with EEPROM;
- Chain 2 connects 45 SRAMs.

**Table 5: SP02 Configuration Chains.**

Chain No	Device No	Device Name	Device Type	Device ID Code	Bypass Switch
0	1	SP_EEPROM_1	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW2
0	2	SP_EEPROM_2	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW3
0	3	SP_EEPROM_3	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW4
0	4	SP_EEPROM_4	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW5
0	5	SP_EEPROM_5	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW6
0	6	SP_FPGA	XC2V4000-5FF1152C	VVVV 0001 0000 0101 0000 0000 1001 0011	MC_SW1

Chain No	Device No	Device Name	Device Type	Device ID Code	Bypass Switch
1	1	VME_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW4
1	2	VME_FPGA	XC2V1000-5FG456C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW5
1	3	FF5_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW2
1	4	FRONT_FPGA_5	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW3
1	5	FF4_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW14
1	6	FRONT_FPGA_4	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW15
1	7	FF3_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW19
1	8	FRONT_FPGA_3	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW20
1	9	DDU_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW10
1	10	DDU_FPGA	XC2V1000-5FG456C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW11
1	11	FF2_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW12
1	12	FRONT_FPGA_2	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW13
1	13	FF1_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW17
1	14	FRONT_FPGA_1	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW18
2	1	ME4C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW7
2	2	ME4C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	3	ME4C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	4	ME4B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	5	ME4B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	6	ME4B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	7	ME4A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	8	ME4A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	9	ME4A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	10	ME3C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	11	ME3C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW9
2	12	ME3C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	13	ME3B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	14	ME3B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	15	ME3B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	16	ME3A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	17	ME3A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	18	ME3A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	19	ME2C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	20	ME2C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	21	ME2C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW8
2	22	ME2B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	23	ME2B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	24	ME2B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	25	ME2A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	26	ME2A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	27	ME2A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	28	ME1F_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	29	ME1F_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	30	ME1F_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	31	ME1E_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW6
2	32	ME1E_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	33	ME1E_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	34	ME1D_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	35	ME1D_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	36	ME1D_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	37	ME1C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	38	ME1C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	39	ME1C_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	40	ME1B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	41	ME1B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW16
2	42	ME1B_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	43	ME1A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	44	ME1A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	45	ME1A_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	

Alex M. is to determine the VME address mapping for the auxiliary VME interface.

## Main VME Interface

### A24 Non Privileged Data Access

An A24 non privileged data access (AM=0x39) to the main VME\_FPGA interface utilizes a 5-bit geographical addressing scheme [ii] and provides for the VME Data Transfer Bus (DTB) multicast *write* cycles by partitioning the address space into the following fields, see Table 6.

**Table 6: Address Format for Non Privileged Data Access**

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA				CA								0	MA		RA						0	0	

Here:

- 0 – Zero value address line;
- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- CA – Chip Address. Positional coding provides simultaneous write access to any combination of SP02 FPGAs (except VME\_FPGA), see Table 7;
- MA – Muon Address. Each FRONT\_FPGA processes data for 3 muons, and the SP\_FPGA services 3 PT LUTs. A 2-bit MA field provides write access either to a single muon-related register or to all three such registers simultaneously, see Table 8 for details.
- RA – Register Address inside FPGA(s). There are 4 groups of registers in total, see Table 9 for details:
  - Action Register Group. Writing to these write-only registers causes pulses, like reset or test pulse, to be generated and/or operations, like start or stop L1ACC processing, to be performed.
  - Control/Status Register Group. These registers carry 2 groups of bits: read-only status bits to monitor, and read/write bits to control behavior of the SP02 logic.
  - Address Register Group. These registers provide access to SRAM and Register File address counters.
  - Data Register Group. The group provides access to SRAM, FIFO and Register File data.

Full Address (FA) of the register is defined as:

$$FA = (SA \ll 19) + (CA \ll 12) + (MA \ll 9) + (RA \ll 2).$$

**Table 7: Chip Address Field Format for Non Privileged Data Access**

Chip	CA, binary	Description
VM	000_0000	VME_FPGA Access
F1	000_0001	FRONT FPGA 1 Access
F2	000_0010	FRONT FPGA 2 Access
F3	000_0100	FRONT FPGA 3 Access
F4	000_1000	FRONT FPGA 4 Access
F5	001_0000	FRONT FPGA 5 Access
DD	010_0000	DDU_FPGA Access
SP	100_0000	SP_FPGA Access

**Table 8: Muon Address Field Format for Non Privileged Data Access**

Label	Muon in FPGA	MA, binary	Description
MA	ALL	00	Access to all three muon-related registers
M1	A/D/1	01	Access to a First (A or D or 1) muon-related register
M2	B/F/2	10	Access to a Second (B or E or 2) muon-related register
M3	C/E/3	11	Access to a Third (C or F or 3) muon-related register

Note, that only *write* access is defined for a group of registers, while *read* access may only be executed to a single register.

**Table 9: Register Address Field Format for Non Privileged Data Access**

RA, hex	Register Label	Description	Valid CA / Valid MA				Page
			SP	DD	Fx	VM	
<b>Action Register Group</b>							
0x00	<a href="#">ACT HR</a>	Hard Resets	-	-	-	MA	14
0x01	<a href="#">ACT CMR</a>	Clock Managers Resets	MA	MA	MA	MA	15
0x02	<a href="#">ACT LCR</a>	Link Counters Resets	-	-	MA/M1/M2/M3	-	15
0x03	<a href="#">ACT XFR</a>	FIFOs Resets	MA	MA	MA	-	16
0x04	<a href="#">ACT ACR</a>	Address Counters Resets	MA	-	MA	-	17
0x05	<a href="#">ACT FCC</a>	Fast Control Command	-	-	-	MA	17
<b>Control/Status Register Group</b>							
0x10	<a href="#">STS CCB</a>	Fast Control Status	-	-	MA	-	17
0x11	<a href="#">STS ANA</a>	CCB Logic Analyzer	-	-	-	MA	18
0x12	<a href="#">STS MWA</a>	MS Winners Analyzer	MA	-	-	-	
0x1E	<a href="#">CSR BID</a>	Board ID	-	-	-	MA	
0x1F	<a href="#">CSR SID</a>	SP Core ID	MA	-	-	-	20
0x20	<a href="#">CSR CID</a>	Chip ID	MA	MA	MA	MA	20
0x22	<a href="#">CSR CM1</a>	Clock Manager 1 Control/Status	MA	MA	MA	MA	20
0x23	<a href="#">CSR CM2</a>	Clock Manager 2 Control/Status	MA	MA	MA	MA	21
0x24	<a href="#">CSR HR</a>	Hard Reset Mask	-	-	-	MA	21
0x25	<a href="#">CSR CFG</a>	Configuration Done Status	-	-	-	MA	21
0x26	<a href="#">CSR INI</a>	Init Status	-	-	-	MA	22
0x28	<a href="#">CSR BSY</a>	Busy Mask/Status	-	-	-	MA	22
0x29	<a href="#">CSR RDY</a>	Ready Mask/Status	-	-	-	MA	23
0x2A	<a href="#">CSR WOF</a>	WarningOfOverflow Mask/Status	-	-	-	MA	23
0x2B	<a href="#">CSR OSY</a>	OutOfSynch Mask/Status	-	MA	MA	MA	24
0x2C	<a href="#">CSR MWC</a>	MS Winners Configuration	MA	-	-	-	25
0x2D	<a href="#">CSR FCC</a>	Fast Control Configuration/Status	MA	MA	MA	MA	25

RA, hex	Register Label	Description	Valid CA / Valid MA				Page
			SP	DD	Fx	VM	
0x30	<a href="#">CSR_LEC</a>	Link Error Counters	-	-	M1/M2/M3	-	26
0x31	<a href="#">CSR_AF</a>	Alignment FIFO Status	M1/M2	-	M1/M2/M3	-	27
0x32	<a href="#">CSR_TF</a>	Test FIFO Status	M1/M2/M3	-	M1/M2/M3	-	28
0x33	<a href="#">CSR_SF</a>	Spy FIFO Status	M1/M2/M3	-	M1/M2/M3	-	28
0x34	<a href="#">CSR_PF</a>	Pipeline FIFO Status	MA	-	MA	-	28
0x35	<a href="#">CSR_DF</a>	DAQ FIFO Status	-	MA	-	-	29
0x36							
0x37	<a href="#">CSR_LF</a>	L1 FIFO Status	MA	MA	MA	-	29
0x38	<a href="#">CSR_RBW</a>	Ring Buffer Write Pointer	MA	-	MA	-	29
0x39	<a href="#">CSR_RBR</a>	Ring Buffer Read Pointer	MA	-	MA	-	30
0x3A	<a href="#">CSR_SF1</a>	F1 Spy FIFO Status	M1/M2/M3	-	-	-	30
0x3B	<a href="#">CSR_SF2</a>	F2 Spy FIFO Status	M1/M2/M3	-	-	-	30
0x3C	<a href="#">CSR_SF3</a>	F3 Spy FIFO Status	M1/M2/M3	-	-	-	31
0x3D	<a href="#">CSR_SF4</a>	F4 Spy FIFO Status	M1/M2/M3	-	-	-	31
0x3E	<a href="#">CSR_SF5</a>	F5 Spy FIFO Status	M1/M2/M3	-	-	-	31
0x3F	<a href="#">CSR_SFE</a>	EMU Spy FIFO Status	MA	-	-	-	32
0x40	<a href="#">CSR_LNK</a>	Link Control/Status	-	MA	MA/M1/M2/M3	-	32
0x41	<a href="#">CSR_AFD</a>	Alignment FIFO Read Delay	MA/M1/M2	-	MA	-	33
0x42	<a href="#">CSR_TFC</a>	Test FIFO Configuration	MA	TBD	MA	-	33
0x43	<a href="#">CSR_SFC</a>	Spy FIFO Configuration	MA	MA	MA	MA	35
0x44	<a href="#">CSR_PFD</a>	Pipeline FIFO Read Delay	MA	-	MA	-	36
0x45	<a href="#">CSR_DFC</a>	DAQ FIFO Configuration	-	MA	-	-	36
0x46	<a href="#">CSR_SCC<sup>4</sup></a>	SP Core Configuration	MA	-	-	-	37
0x47	<a href="#">CSR_TFB</a>	Barrel Test FIFO Status	M1/M2	-	-	-	37
0x48	<a href="#">CSR_SFB</a>	Barrel Spy FIFO Status	M1/M2	-	-	-	37
0x49	<a href="#">CSR_SFM</a>	Muon Sorter Spy FIFO Status	M1/M2/M3	-	-	-	37
0x4A	<a href="#">CSR_TF1</a>	F1 Test FIFO Status	M1/M2/M3	-	-	-	38
0x4B	<a href="#">CSR_TF2</a>	F2 Test FIFO Status	M1/M2/M3	-	-	-	38
0x4C	<a href="#">CSR_TF3</a>	F3 Test FIFO Status	M1/M2/M3	-	-	-	39
0x4D	<a href="#">CSR_TF4</a>	F4 Test FIFO Status	M1/M2/M3	-	-	-	39
0x4E	<a href="#">CSR_TF5</a>	F5 Test FIFO Status	M1/M2/M3	-	-	-	39
0x4F	<a href="#">CSR_TFE</a>	EMU Test FIFO Status	MA	-	-	-	40
<b>Address Counter Group</b>							
0x50	<a href="#">CNT_LPL</a>	Local Phi LUT Address Low	-	-	MA	-	40
0x51	<a href="#">CNT_LPH</a>	Local Phi LUT Address High	-	-	MA	-	40
0x52	<a href="#">CNT_GLL</a>	Global Eta/Phi/DT LUT Address Low	-	-	MA	-	41
0x53	<a href="#">CNT_GLH</a>	Global Eta/Phi/DT LUT Address High	-	-	MA	-	42
0x56	<a href="#">CNT_PTL</a>	PT LUT Address Low	MA	-	-	-	41
0x57	<a href="#">CNT_PTH</a>	PT LUT Address High	MA	-	-	-	42
0x58	<a href="#">CNT_ETA</a>	Eta Address	MA	-	-	-	42

<sup>4</sup> Access to this register is available only when SP02 is under VME control (see VM/MA/CSR\_FCC) and the L1A\_FSM is in L1\_STOP state.

RA, hex	Register Label	Description	Valid CA / Valid MA				Page
			SP	DD	Fx	VM	
<b>Data Register Group</b>							
0x5A	<a href="#">DAT TF1</a>	F1 Test FIFO Data	M1/M2/M3	-	-	-	42
0x5B	<a href="#">DAT TF2</a>	F2 Test FIFO Data	M1/M2/M3	-	-	-	43
0x5C	<a href="#">DAT TF3</a>	F3 Test FIFO Data	M1/M2/M3	-	-	-	43
0x5D	<a href="#">DAT TF4</a>	F4 Test FIFO Data	M1/M2/M3	-	-	-	44
0x5E	<a href="#">DAT TF5</a>	F5 Test FIFO Data	M1/M2/M3	-	-	-	44
0x5F	<a href="#">DAT TFE</a>	EMU Test FIFO Data	MA	-	-	-	44
0x60	<a href="#">DAT LP<sup>4</sup></a>	Local Phi LUT Data	-	-	MA/M1/M2/M3	-	45
0x62	<a href="#">DAT GP<sup>4</sup></a>	Global Phi LUT Data	-	-	MA/M1/M2/M3	-	45
0x63	<a href="#">DAT DT<sup>4</sup></a>	DT LUT Data	-	-	MA/M1/M2/M3	-	46
0x64	<a href="#">DAT GE<sup>4</sup></a>	Global Eta LUT Data	-	-	MA/M1/M2/M3	-	46
0x66	<a href="#">DAT PT<sup>4</sup></a>	PT LUT Data	MA/M1/M2/M3	-	-	-	47
0x68	<a href="#">DAT ETA<sup>4</sup></a>	Eta Data	MA	-	-	-	47
0x69	<a href="#">DAT VPC</a>	Valid Pattern Counter Data	M1/M2/M3	-	M1/M2/M3	-	48
0x6A	<a href="#">DAT SF1</a>	F1 Spy FIFO Data	M1/M2/M3	-	-	-	48
0x6B	<a href="#">DAT SF2</a>	F2 Spy FIFO Data	M1/M2/M3	-	-	-	49
0x6C	<a href="#">DAT SF3</a>	F3 Spy FIFO Data	M1/M2/M3	-	-	-	49
0x6D	<a href="#">DAT SF4</a>	F4 Spy FIFO Data	M1/M2/M3	-	-	-	49
0x6E	<a href="#">DAT SF5</a>	F5 Spy FIFO Data	M1/M2/M3	-	-	-	50
0x6F	<a href="#">DAT SFE</a>	EMU Spy FIFO Data	MA	-	-	-	50
0x72	<a href="#">DAT TF</a>	Test FIFO Data	MA/M1/M2/M3	MA	MA/M1/M2/M3	-	51
0x73	<a href="#">DAT SF</a>	Spy FIFO Data	M1/M2/M3	MA	M1/M2/M3	-	52
0x75	<a href="#">DAT DF</a>	DAQ FIFO Data	-	MA	-	-	53
0x76	<a href="#">DAT TFB</a>	Barrel Test FIFO Data	MA/M1/M2	-	-	-	55
0x77	<a href="#">DAT SFB</a>	Barrel Spy FIFO Data	M1/M2	-	-	-	55
0x78	<a href="#">DAT SFM</a>	Muon Sorter Spy FIFO Data	M1/M2/M3	-	-	-	56
0x7F	<a href="#">DAT RW</a>	Read / Write Data	MA	MA	MA	MA	57

The main VME\_FPGA interface distributes VME control all over the board via the Internal Data Transfer Bus (IDTB). IDTB is a synchronous parallel bus that is used by the VME\_FPGA to transfer data to or from other SP02 FPGA(s): the SP\_FPGA, 5 FRONT\_FPGAs, and the DDU\_FPGA.

The IDTB bus lines are grouped into 4 categories:

- Address Lines: A[11:2] see Table 10;
- Data Lines: D[15:0] Bi-directional;
- Control Lines: /CS[7:1] Chip Select, active LOW;  
/ACK[7:1] Acknowledge, active LOW;  
/WR Write, active LOW;
- Auxiliary Lines: VMB\_WR Buffer Write;  
VMB\_/OE Buffer Output Enable, active LOW.

**Table 10: IDTB Address Format**

<b>A11</b>	<b>A10</b>	<b>A9</b>	<b>A8</b>	<b>A7</b>	<b>A6</b>	<b>A5</b>	<b>A4</b>	<b>A3</b>	<b>A2</b>	
RV	MA	RA								
RV	IA									

- IA – Internal DTB Address, defines a storage location inside FPGA

- RV – Reserved line

To prevent data lines from being too long they are split into two segments: the SP segment and the FRONT/DDU segment, with bi-directional buffers in between. The SP segment connects directly to the VME\_FPGA pins. The FRONT/DDU segment is located behind the buffers. Two auxiliary lines: Buffer Write (data direction) and Buffer Output Enable, - are used to control data flow through the buffers.

The IDTB transfer is a sequence of level states on the signal lines that results in the transfer of an address and two bytes of data between the VME\_FPGA and other SP02 FPGA(s).

Each IDTB cycle is an inherent part of the backplane DTB cycle, when DTB addresses FPGA(s), other than the VME\_FPGA. Chip Select (/CS) plays a role of the DS\* strobe and Acknowledge (/ACK) plays a role of the DTACK\*. The major difference between backplane DTB and IDTB is that IDTB is a synchronous bus, i.e. both /CS and /ACK handshake signals should be asserted on the rising edge of the system clock at source, and sensed with the next rising edge of the system clock at destination.

The VME\_FPGA initiates two types of IDTB cycles:

- **IDTB Write cycle** transfers data from the VME\_FPGA to one or more destination FPGA(s). The cycle begins when the VME\_FPGA sets address, data, Write and optionally Buffer Write and Buffer Output Enable on the corresponding lines and issues one or more Chip Selects. Selected FPGA(s) capture(s) the address and check(s) to see if it is to respond to the cycle. If so, sensing Write in a LOW state, it stores the data and acknowledges the transfer. The VME\_FPGA then terminates the cycle.
- **IDTB Read cycle** transfers data from the source FPGA to the VME\_FPGA. The cycle begins when the VME\_FPGA sets address and optionally a Buffer Output Enable and issues a Chip Select. Selected FPGA captures the address and checks to see if it is to respond to the cycle. If so, sensing Write in a HIGH state, it retrieves the data from the corresponding storage, places it on the data lines and acknowledges the transfer. The VME\_FPGA then terminates the cycle.

Normally the VME\_FPGA would terminate the DTB transfer with the Data Transfer Acknowledge (DTACK\*) asserted low. If during the DTB cycle the addressable SP02 detects that the VME Master either addresses a non-existent location, or tries to write to a read-only location, the VME\_FPGA terminates the cycle with a Bus Error (BERR\*) asserted low. The VME\_FPGA is not aware of the DTB outcome, when it passed the DTB cycle to the IDTB. If the expected IDTB Acknowledge(s) is (are) not received in time, the VME\_FPGA terminates the cycle driving BERR\* low.

## A24 Non Privileged Program Access

An A24 non privileged program access (AM=0x3A) is used to load four mapping locations in the VME FPGA, see Table 11 for valid address fields

**Table 11: Address Format for Non Privileged Program Access**

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA				X												PA				0	0		

Here:

- X – Don’t care bit;
- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- PA – Program Address, defines 16 register locations in the non privileged program space, see Table 12 for valid addresses.

**Table 12: Register Address Field Format for Non Privileged Program Access**

PA, hex	Register Label	Description
<b>BLT Mapping Control/Status Register Group</b>		
0x0		
0x1	CPA_BF1	BLT Mapping FIFO 1 Control/Status
0x2	CPA_BF2	BLT Mapping FIFO 2 Control/Status
0x3	CPA_BF3	BLT Mapping FIFO 3 Control/Status
0x4		Reserved
0x5		Reserved
0x6		Reserved
0x7		Reserved
<b>BLT Mapping Data Register Group</b>		
0x8	DPA_BLT	BLT Mapping Data
0x9	DPA_BF1	BLT Mapping FIFO 1 Data
0xA	DPA_BF2	BLT Mapping FIFO 2 Data
0xB	DPA_BF3	BLT Mapping FIFO 3 Data
0xC		Reserved
0xD		Reserved
0xE		Reserved
0xF		Reserved

Details on the above registers can be found in the Register Detail section under the register label. During BLT transfers, mapping registers substitute the DTB address with a 16-bit address, used to access storage location(s) in the non privileged data space. The format of the mapping data/address is shown below:

**Table 13: BLT Mapping Location Data Format**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CA							MA			RA					

Here CA, MA, and RA are address fields, described in the A24 Non Privileged Data Access section above.

**A24 Non Privileged Block Transfer (BLT)**

Any storage location, accessible via the A24 Non Privileged Data Access, can also be accessed via an A24 non privileged block transfer (BLT), when AM=0x3B. The BLT, prior to executing, should be initialized by loading a mapping location with one or more destination addresses. The BLT mapping locations are listed in Table 12. During the BLT DTB cycle the VME\_FPGA, depending on the value in the BA field, uses one of the preloaded mapping

locations to substitute the current DTB address with the address stored in the mapping location, see Table 14. Table 13 shows the BLT mapping location data format and Table 15 lists 4 128Kbyte windows for block transfers.

**Table 14: Address Format for Non Privileged Block Transfers**

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA				BA				X															0

Here:

- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- BA – BLT Address. Defines one out of four BLT Mapping locations inside the VME\_FPGA to substitute the current VMA backplane address with the preloaded one;
- X – Don't care bit.

**Table 15: BLT Address Field Format for Non Privileged Block Transfers**

BA, binary	Register Name	First D16 Transfer Address, hex	Last D16 Transfer Address, hex	Address Space
00	BLT Mapping Register	0x00000	0x1FFFE	64 Kwords = 128 Kbytes
01	BLT Mapping FIFO_1	0x20000	0x3FFFE	64 Kwords = 128 Kbytes
10	BLT Mapping FIFO_2	0x40000	0x5FFFE	64 Kwords = 128 Kbytes
11	BLT Mapping FIFO_3	0x60000	0x7FFFE	64 Kwords = 128 Kbytes

## Register Detail

### Action Register Group

#### ACT\_HR – FPGA Hard Reset Register

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 400 ns Hard Reset pulse to the selected FPGA(s) onboard. Hard Reset is applied to the /PROG\_B pin of the corresponding FPGA. A VME-generated Hard Reset is ORed with a CCB backplane hard reset. This register address is applicable to the VME\_FPGA only.

Sensing a hard reset on its input, the FPGA reloads its configuration from the associated configuration EPROM. The user may use the ACT\_HR transfer cycle to verify chip presence on the board. To make sure all FPGA chips are present on the board, the CSR\_CFG read transfer cycle should be executed twice after the ACT\_HR: first time when chips are engaged in the configuration process and second time after a 5 sec pause, when the configuration is definitely completed. If there is a missing FPGA chip on the board (a mezzanine card is not installed, for example) then the corresponding Configuration Done line remains floating, and can be sensed by the VME\_FPGA as being either in HIGH (Logic ONE) or LOW (Logic ZERO) state. But in any case, Configuration Done line for a missing chip (for example, SP\_FPGA) would retain its state, while the one for a successfully configured FPGA will be LOW on the first read and HIGH on the second read. See Table 34 for chip mapping.

**Table 16: ACT\_HR Data Format**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	SPHR	DDHR	F5HR	F4HR	F3HR	F2HR	F1HR	X

Here:

- X – Don't care bit;
- F1HR – FRONT\_FPGA\_1 Hard Reset;
- F2HR – FRONT\_FPGA\_2 Hard Reset;
- F3HR – FRONT\_FPGA\_3 Hard Reset;
- F4HR – FRONT\_FPGA\_4 Hard Reset;
- F5HR – FRONT\_FPGA\_5 Hard Reset;
- DDHR – DDU\_FPGA Hard Reset;
- SPHR - SP\_FPGA Hard Reset.

### ACT\_CMR – Clock Manager Reset

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 50 ns reset pulse(s) to selected DCM(s). Reset pulse resets also DCM error counters described under CSR\_CM1 – System Clock Manager 1 Status and CSR\_CM2 – System Clock Manager 2 Status headings. The register address is applicable to all FPGAs.

**Table 17: ACT\_CMR Data Format for VM\_FPGA, FRONT\_FPGA, DDU\_FPGA, and SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	CMR2	CMR1	X

Here:

- X – Don't care bit;
- CMR1 – Clock Manager 1 Reset;
- CMR2 – Clock Manager 2 Reset.

### ACT\_LCR – Link Counters Resets

Writing Logic ONE to specified bit(s) of this write-only register results in sending 25 ns reset pulse(s) to selected error counter(s) described under the CSR\_LNK, CSR\_LEC and DAT\_VPC headings. The register address is applicable to the FRONT\_FPGA and to the SP\_FPGA.

**Table 18: ACT\_LCR Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	VPR	TER	SLR	CER	EWR

Here:

- X – Don't care bit;
- EWR – TLK2501 Error Word Counter Reset in the CSR\_LEC register (RXDV == HIGH, RXER == HIGH);
- CER – TLK2501 Carrier Extend Counter Reset in the CSR\_LEC register (RXDV == LOW, RXER == HIGH);
- SLR – FINISAR optical receiver Signal Loss Counter Reset in the CSR\_LEC register (RXSD goes LOW);

- TER – PRBS Test Error Counter Reset in the CSR\_LNK register;
- VPR – Valid Pattern Counter Reset in the DAT\_VPC register.

**Table 19: ACT\_LCR Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	VPR	X	X	X	X

Here:

- X – Don't care bit;
- VPR – Valid Pattern Counter Reset in the DAT\_VPC register.

**ACT\_XFR – FIFO Resets**

Writing Logic ONE to a specified bit of this write-only register results in sending a 25 ns reset pulse to the corresponding FIFO(s). The register address is applicable to the FRONT\_FPGA, DDU\_FPGA and SP\_FPGA.

**Table 20: ACT\_XFR Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	DFR	PFR	SFR	TFR	X

Here:

- X – Don't care bit;
- TFR – All Test FIFOs Reset (Init);
- SFR – All Spy FIFOs Reset (Init);
- PFR – Pipeline FIFO Reset (Init);
- DFR – DAQ (Readout Logic) Reset. It resets L1 Accept FIFO, Ring Buffer Read and Ring Buffer Write Pointers.

**Table 21: ACT\_XFR Data Format for DDU\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	DFR	X	X	X	X

Here:

- X – Don't care bit;
- DFR – DAQ FIFO Reset (Init). It also resets L1 Accept FIFO and event builder FSM;

**Table 22: ACT\_XFR Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	DFR	PFR	SFR	TFR	AFR

Here:

- X – Don't care bit;
- AFR – Barrel Alignment FIFO Reset (Init);
- TFR – All Test FIFOs Reset (Init);
- SFR – All Spy FIFOs Reset (Init);
- PFR – Pipeline FIFO Reset (Init);
- DFR – DAQ (Readout Logic) Reset. It resets L1 Accept FIFO, Ring Buffer Read and Ring Buffer Write Pointers.

**ACT\_ACR – Address Counters Reset(s)**

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 25 ns reset pulse to a corresponding address counter. The register address is applicable to FRONT\_FPGA and SP\_FPGA.

**Table 23: ACT\_ACR Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	GLR	LPR

Here:

- X – Don't care bit;
- LPR – Local Phi LUT Address Counter Reset;
- GLR – Global Phi/Eta/DT LUT Address Counter Reset.

**Table 24: ACT\_ACR Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	ETR	PTR	X	X

Here:

- X – Don't care bit;
- PTR – PT LUT Address Counter Reset;
- ETR – Eta Min/Max/Window Address Counter Reset.

**ACT\_FCC – Fast Control Command**

VME write cycle to this write-only register is equivalent to getting the same fast control command from the CCB over the backplane. The difference is that the CCB commands are available to all modules in the crate, while this command affects only the addressable SP02. Note, that ACT\_FCC commands are enabled only when the CSR\_FCM register is configured to a local fast control mode.

**Table 25: ACT\_FCC Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L1A	X	X	X	X	X	X	X	FCC7	FCC6	FCC5	FCC4	FCC3	FCC2	FCC1	FCC0

Here:

- X – Don't care bit;
- FCC[7:0] – Fast Control Command, the data format matches the TTC \$C4 register and the CCB CSR2 register formats;
- L1A – L1Accept Command.

**Control/Status Register Group****STS\_CCB – Fast Control Command bus Status.**

This read-only register returns current state of the SP02 internal Fast Control Command bus. The register address is valid for FRONT\_FPGA. The current bus state should always be zero, if there are no shorts on the board. See the CCB Interface section for a list of Fast Control Commands.

**Table 26: STS\_CCB Data Format for FRONT\_FPGA**

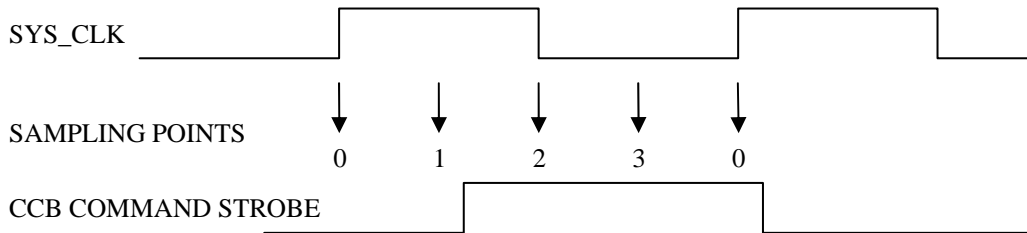
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	FCS5	FCS4	FCS3	FCS2	FCS1	FCS0	0	0	FCP5	FCP4	FCP3	FCP2	FCP1	FCP0
Current FC State								Previous FC Command							

Here:

- FCS [5:0] – current state of the Fast Control Command bus;
- FCP [5:0] – previous Fast Control Bus Command;

**STS\_ANA – CCB Analyzer**

The CCB analyzer allows registering timing of the CCB command strobe with respect to the SP02 system clock, as well as the CCB command itself. The SP02 system clock (SYS\_CLK) is a deskewed CCB\_CLK that drives every SP02 FPGA chip. The contents of the analyzer is reset on power-up and on any write command (data value is irrelevant) to this register. After reset, it starts recording non-zero data, if the SP02 is under the CCB fast control; see the CSR\_FCC register description on how to set the SP02 under the CCB control. Any read command returns recorded data in the format shown below. The analyzer keeps up to 64 data words. If the analyzer is empty, the read command returns bus error to the VME Master. Typical position of the CCB2001 command strobe is shown below:



**Figure 2: CCB2001 Command Strobe typical position**

Typical set of values that analyzer returns after recording the CCB\_L1RES, CCB\_L1STT and CCB\_BCO command sequence are:

- 1<sup>st</sup> word = 0x0C0C;
- 2<sup>nd</sup> word = 0x0100;
- 3<sup>rd</sup> word = 0x0C18;
- 4<sup>th</sup> word = 0x0100;
- 5<sup>th</sup> word = 0x0C04;
- 6<sup>th</sup> word = 0x0100.

Since the analyzer records only non-zero input, the above sequence means that:

- Valid samples are on phase 2, 3, and 0;
- Sampling on phase 1 does not register the command strobe;
- The VME\_FPGA finally samples the CCB command on phase 3, which is the middle valid sample.

**Table 27: STS\_ANA Data Format for VME\_FPGA**

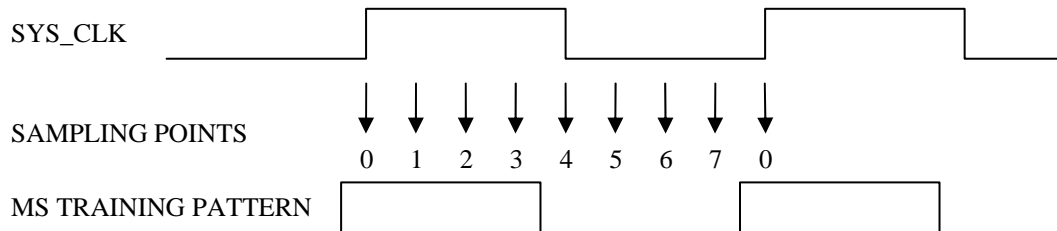
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DSTR3	DSTR2	DSTR1	DSTR0	CSTR3	CSTR2	CSTR1	CSTR0	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	ECRES	BCRES
CCB Data Strobe				CCB Command Strobe				CCB command							

Here:

- DSTR[3:0] – CCB data strobe sampled on four different phases of the SYS\_CLK clock (3/4, 2/4, 1/4, and 0/4 of the SYS\_CLK period);
- CSTR[3:0] – CCB command strobe sampled on four different phases of the SYS\_CLK clock (3/4, 2/4, 1/4, and 0/4 of the SYS\_CLK period);
- CMD [7:2] – CCB command code;
- ECRES – Event Counter Reset;
- BCRES – Bunch Counter Reset.

**STS\_MWA – MS Winners Analyzer**

This analyzer allows determining a timing position of the Muon Sorter Winner bits, when the TF crate is in L1\_STOP state and the MS provides a training pattern for the SP02. A training pattern is a 40.08 MHz positive square wave. The training pattern can also be thought of as a 80Mbit/sec sequence of logical ONES (frame 1 of a 40 MHz reference clock) and ZEROS (frame 2). The analyzer uses 4 sampling points per frame to determine position of frames' boundaries. Figure below shows typical position of winner bits for the MS2004:



**Figure 3: MS2004 Winner bit typical position**

A typical value the analyzer returns is 0x0F0F, and sometimes 0x0F1F. The latter tells us that the duty factor of the training pattern is a little bit more than 50%. So, the optimal CSR\_MWC setting is 2.

**Table 28: MWA\_ANA Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
MWM7	MWM6	MWM5	MWM4	MWM3	MWM2	MWM1	MWM0	MWL7	MWL6	MWL5	MWL4	MWL3	MWL2	MWL1	MWL0
MS Winner MSB								MS Winner LSB							

Here:

- MWL [7:0] – MS Winner LSB sampled at 8 phases of the SYS\_CLK clock (7/8, 6/8, 5/8, 4/8, 3/8, 2/8, 1/8 and 0/8 of the SYS\_CLK period);
- MWM [7:0] – MS Winner MSB sampled at 8 phases of the SYS\_CLK clock (7/8, 6/8, 5/8, 4/8, 3/8, 2/8, 1/8 and 0/8 of the SYS\_CLK period).

**CSR\_SID – SP Core ID Register**

This SP\_FPGA read-only register keeps an SP core code release date in the following format:

**Table 29: CSR\_SID Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
YY			MM				1	1	1	DD					

Here:

- DD – Day Code (01...31);
- MM – Month Code (01...12);
- YY – Year Code (00...15) = Year - 2000.

**CSR\_CID – Chip ID Register**

This read-only register keeps a firmware release date in the format shown in the table below. Register address is applicable to all FPGAs.

**Table 30: CSR\_CID Data Format for all FPGAs**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
YY			MM				NN			DD					

Here:

- DD – Day Code (01...31);
- NN – FPGA Number (0...7), which corresponds to 8 FPGA chips, numbered in the following order: VM, F1, F2, F3, F4, F5, DD, SP;
- MM – Month Code (01...12);
- YY – Year Code (00...15) = Year - 2000.

**CSR\_CM1 – System Clock Manager 1 Status**

This read-only register keeps history of Digital Clock Manager 1 behavior after the last ACT\_CM1 command. Its default value is 0x0004, which means that all enabled DCM1 features locked and there were no errors since last reset. DCM1 is a DCM with internal feedback, distributing the 40.078 MHz system clock in the chip.

**Table 31: CSR\_CM1 Data Format for all FPGAs**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LCK1 Counter			CST1 Counter				0	0	0	0	0	LCK1	CST1	PSO1	

Here:

- PSO1 – Phase Shift Overflow, should be LOW for normal operation;
- CST1 – Input Clock Stopped Toggling;
- CST1 Counter – “loss of input clock” counter. It counts number of “CST1 go HIGH” after last DCM1 reset. The counter stops when it reaches its maximum value of 15;
- LCK1 – All enabled DCM features locked;
- LCK1 Counter – “loss of lock” counter. It counts number of “LCK1 go LOW” after last DCM1 reset. The counter stops when it reaches its maximum value of 15.

### CSR\_CM2 – System Clock Manager 2 Status

This read-only register keeps history of Digital Clock Manager 2 behavior after the last ACT\_CM2 command. Its default value is 0x0004, which means that all enabled DCM2 features locked and there were no errors since last reset. For the VME\_FPGA, DCM2 is a DCM with external feedback, distributing system clock all over the board. For the FRONT\_FPGA, DDU\_FPGA and SP\_FPGA, the DCM2 distributes the 80.156 MHz clock in the chip.

**Table 32: CSR\_CM2 Data Format for all FPGAs**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LCK2 Counter				CST2 Counter				0	0	0	0	0	LCK2	CST2	PSO2

Here:

- PSO2 – Phase Shift Overflow, should be LOW for normal operation;
- CST2 – Input Clock Stopped Toggling;
- CST2 Counter – “loss of input clock” counter. It counts number of “CST2 go HIGH” after last DCM2 reset. The counter stops when it reaches its maximum value of 15;
- LCK2 – All enabled DCM features locked;
- LCK2 Counter – “lost of lock” counter. It counts number of “LCK2 go LOW” after last DCM2 reset. The counter stops when it reaches its maximum value of 15.

### CSR\_HR – Hard Reset Mask

In the VME\_FPGA the CSR\_HR register masks the CCB Hard Reset signal. By default the CCB hard reset is disabled for all SP02 chips.

**Table 33: CSR\_HR Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	HRM7	HRM6	HRM5	HRM4	HRM3	HRM2	HRM1	X

Here:

- X – Don’t care bit, reads back as zero;
- HRM [7:1] = 0x00 (default) – Hard Reset mask for SP, DD, F5...F1 chips.

### CSR\_CFG – FPGA Configuration Done Status

Addressing to this read-only register allows verifying the Configuration Done status of the FRONT\_FPGAs, DDU\_FPGA, and SP\_FPGA after hard resets. The register address is applicable to the VME\_FPGA only. Register’s default value is 0xFE, when all chips, including the mezzanine card’s chip, are in place. Being Low during configuration, Configuration Done High indicates completion of the configuration.

To make sure all FPGA chips are present on board, the CSR\_CFG command should be executed twice: first, when chips are engaged in the configuration process, i.e. immediately after the ACT\_HR command, and second, after a 5 sec pause, when the configuration is definitely completed. If there is a missing FPGA chip on board (a mezzanine card not installed, for example), then the corresponding Configuration Done line remains floating, and could be sensed by the VME\_FPGA either as a logic ONE or logic ZERO. But in any case, Configuration Done line for a missing chip would retain its state, while the one for a successfully configured FPGA will be LOW on the first read and HIGH on the second read.

**Table 34: CSR\_CFG Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	CFG7	CFG6	CFG5	CFG4	CFG3	CFG2	CFG1	0
Configuration Done Status															

Here:

- CFG [7:1] = 0xFE (default) – Configuration Done Status bits for the SP, DD, F5, F4, F3, F2, and F1 FPGAs accordingly.

### CSR\_INI – FPGA Init Status

Addressing to this read-only register allows verifying the INIT\_B pin status of the FRONT\_FPGAs, DDU\_FPGA, and SP\_FPGA after hard resets. The register address is applicable to the VME\_FPGA only. The default register value is 0xFE. INIT\_B Low indicates memory is being cleared. The INIT\_B pin transitions HIGH when the clearing of configuration memory is complete. INIT\_B LOW during configuration indicates an error.

**Table 35: CSR\_INI Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	INI7	INI6	INI5	INI4	INI3	INI2	INI1	0
Init_B Status															

Here:

- INI [7:1] = 0xFE (default) – Init\_B Status bits for the SP, DD, F5, F4, F3, F2, and F1 FPGAs accordingly.

### CSR\_BSY – Busy Control / Status

In the VME\_FPGA the CSR\_BSY register displays status of seven input and one output BSY lines. Besides, it carries eight mask bits, so each input or/and the VME\_FPGA output can be either disabled or enabled:

$$BSY0 = (BSY1 * BSC1 + BSY2 * BSC2 + BSY3 * BSC3 + BSY4 * BSC4 + BSY5 * BSC5 + BSY6 * BSC6 + BSY7 * BSC7 + BSY0\_INT) * BSC0$$

Indexes 0...7 stand for chip numbers; see Table 7 and/or Table 30 for chip numbering scheme, and BSY0\_INT is an internal busy status of the VME\_FPGA, which is “1” when counting of CCB\_L1ACCs is stopped (disabled).

The FRONT\_FPGA sets BSY to “1”, when either the Bunch counter carries 0xFFF=4095 value, or link resynch on CCB\_L1RES failed (the AF word count remains zero).

**Table 36: CSR\_BSY Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
BSM7	BSM6	BSM5	BSM4	BSM3	BSM2	BSM1	BSM0	BSY7	BSY6	BSY5	BSY4	BSY3	BSY2	BSY1	BSY0	R
BSM7	BSM6	BSM5	BSM4	BSM3	BSM2	BSM1	BSM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- BSM [7:0] – Busy Chip mask for SP, DD, F5...F1, and VM chips;
- BSY [7:0] – Busy status for SP, DD, F5...F1, and VM chips.

**CSR\_RDY – Ready Control / Status**

In the VME\_FPGA the CSR\_RDY register displays status of seven input and one output RDY lines. Besides, it carries eight mask bits, so each input or/and VME\_FPGA output can be either disabled or enabled:

$$RDY0 = (RDY1 * RDM1 + RDY2 * RDM2 + RDY3 * RDM3 + RDY4 * RDM4 + RDY5 * RDM5 + RDY6 * RDM6 + RDY7 * RDM7) * RDY0\_INT * RDM0$$

Indexes 0...7 stand for chip numbers; see Table 7 and/or Table 30 for chip numbering scheme, and RDY0\_INT is an internal ready status of the VME\_FPGA, which is “1” when passing of CCB\_L1ACCs to the FC bus is enabled.

The FRONT\_FPGA sets RDY to “1”, when link resynchronization initiated by CCB\_L1RES completed a success (the Alignment FIFO is neither empty, nor full). Only links with enabled TLK2501 receivers contribute to the chip’s RDY status; see the CSR\_LNK register for a DVEN bit description.

**Table 37: CSR\_RDY Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
RDM7	RDM6	RDM5	RDM4	RDM3	RDM2	RDM1	RDM0	RDY7	RDY6	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	R
RDM7	RDM6	RDM5	RDM4	RDM3	RDM2	RDM1	RDM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don’t care bit;
- RDM [7:0] – Ready Chip mask for SP, DD, F5...F1, and VM chips;
- RDY [7:0] – Ready status for SP, DD, F5...F1, and VM chips.

**CSR\_WOF – Warning-of-Overflow Control / Status**

In the VME\_FPGA the CSR\_WOF register displays status of seven input and one output WOF lines. Besides, it carries eight mask bits, so each input or/and VME\_FPGA output can be either disabled or enabled:

$$WOF0 = (WOF1 * WOM1 + WOF2 * WOM2 + WOF3 * WOM3 + WOF4 * WOM4 + WOF5 * WOM5 + WOF6 * WOM6 + WOF7 * WOM7) * WOM0$$

Indexes 0...7 stand for chip numbers; see Table 7 and/or Table 30 for a chip numbering convention.

The WOF0 signal controls the SP02 readout process by inhibiting the FC\_L1STR signal: incoming CCB\_L1ACC signals increment event counters to keep them in synch with other systems, but no events get added to the readout queue. Both the FRONT\_FPGA and SP\_FPGA set WOF to “1”, when either the L1 Accept FIFO or Ring Buffer are almost full. Both drop WOF to “0”, when there is a room for at least one more event. The DDU\_FPGA sets its WOF to “1”, when the DAQ FIFO is almost full, and drops it to “0”, when there is a room for at least one more event.

**Table 38: CSR\_WOF Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
WOM7	WOM6	WOM5	WOM4	WOM3	WOM2	WOM1	WOM0	WOF7	WOF6	WOF5	WOF4	WOF3	WOF2	WOF1	WOF0	R
WOM7	WOM6	WOM5	WOM4	WOM3	WOM2	WOM1	WOM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don’t care bit;
- WOM [7:0] – Warning-of-Overflow chip Mask for SP, DD, F5...F1, and VM chips;

- WOF [7:0] – Warning-of-Overflow status for SP, DD, F5...F1, and VM chips.

**CSR\_OSY – Out-of-Synch Control / Status**

In the VME\_FPGA the CSR\_OSY register displays status of seven input and one output OSY lines. Besides, it carries eight mask bits, so each input or/and output can be either disabled (mask bit = 0) or enabled (mask bit = 1 => default):

$$OSY0 = (OSY1*OSM1 + OSY2*OSM2 + OSY3*OSM3 + OSY4*OSM4 + OSY5*OSM5 + OSY6*OSM6 + OSY7 *OSM7) * OSM0$$

Indexes 0...7 stand for chip numbers; see Table 7 and/or Table 30 for chip numbering scheme. By default all masks are set to enable state.

**Table 39: CSR\_OSY Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
OSM7	OSM6	OSM5	OSM4	OSM3	OSM2	OSM1	OSM0	OSY7	OSY6	OSY5	OSY4	OSY3	OSY2	OSY1	OSY0	R
OSM7	OSM6	OSM5	OSM4	OSM3	OSM2	OSM1	OSM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- OSM [7:0] – Out-of-Synch Chip mask for SP, DD, F5...F1 and VM chips;
- OSY [7:0] – Out-of-Synch status for SP, DD, F5...F1 and VM chips.

In the FRONT\_FPGA each link has a bunch counter associated with it, which is controlled by both the L1 Accept FSM and link bc0 mark. When the FSM is in L1\_STOP state the bunch counter is preset to a 0xFFE value. The bunch counter starts counting from one and up on a first bc0 mark it gets from the link after the FSM moved on from L1\_STOP state. From this moment on the monitor logic continuously compares bc0 and bx0 marks coming from the link against the counter zero state and the counter LSB accordingly. Any mismatch found sets an error bit: mismatch in bc0 sets a BCE bit and mismatch in bx0 sets a BXE bit. Once set, the error bit holds ONE until fast control command puts the FSM into L1\_STOP state again. On this transition, errors accumulated during L1\_RUN state get stored into BCR and BXR bits, while BCE and BXE bits are reset to zero.

One more bunch counter monitors the CCB timing. The logic of operation is very similar to that of link counters, except that it starts counting on FC\_BC0 command and monitors only FC\_BC0 timing marks.

All bits are reset on power-up and FC\_L1RES command.

**Table 40: CSR\_OSY Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
BCR3	BXR3	BCE3	BXE3	BCR2	BXR2	BCE2	BXE2	BCR1	BXR1	BCE1	BXE1	BCR0	0	BCE0	0	R
M3 Link Timing Monitor				M2 Link Timing Monitor				M1 Link Timing Monitor				CCB Timing Monitor				W

Here:

- X – Don't care bit;
- BXE [3:1] – bx0 out-of-synch condition detected during current run;
- BCE [3:0] – bc0 / FC\_BC0 out-of-synch condition detected during current run;
- BXR [3:1] – bx0 out-of-synch condition detected during previous run;
- BCR [3:0] – bc0 / FC\_BC0 out-of-synch condition detected during previous run;

In the DDU\_FPGA the CSR\_OSY register carries Out-of-Synch status for the SP\_FPGA and FRONT\_FPGAs. During readout process of each event the DDU\_FPGA queries other FPGAs for their bunch counter and event counter values, compares them against templates and sets out-of-synch flags, if the comparison fails. The SP\_FPGA provides a template for the bunch counter comparison, and the DDU\_FPGA provides a template for the event counter comparison.

**Table 41: CSR\_OSY Data Format for DDU\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
OSE7	0	OSE5	OSE4	OSE3	OSE2	OSE1	0	0	0	OSB5	OSB4	OSB3	OSB2	OSB1	0	R

Here:

- OSE [7:1] – SP\_FPGA and FRONT\_FPGA Event Counter Out-of-Synch bits;
- OSB [5:1] – FRONT\_FPGA Bunch Counter Out-of-Synch bits.

### CSR\_MWC – MS Winners Configuration

This read/write register sets the SYS\_CLK sampling phase for MS Winner bits; see the STS\_MWA register description for details.

**Table 42: CSR\_MWC Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	0	0	0	0	0	0	0	0	0	0	MWP2	MWP1	MWP0	R
X	X	X	X	X	X	X	X	X	X	X	X	X	MW Phase [2:0]			W

Here:

- X – Don't care bit;
- MWP [2:0] = 0...7, 2 – default, the SYS\_CLK Sampling Phase for MS Winners.

### CSR\_FCC – Fast Control Configuration / Status

This read/write register sets the SP02 fast control modes and shows the status of the L1Accept control state machine. The FCM bit switches the source of fast control commands, which could be either from the local VME interface (default on power-up), or from the CCB over the TF crate backplane. The FCL bit controls the source for the internal FC\_L1ACC signal. The source can be either a backplane CCB\_L1ACC signal (default), or a fake signal, generated on every FC\_SFRUN to facilitate debugging of the readout logic. The feature is used for validation of the readout process in the SP02. The SP02 should be in a L1\_RUN state to let a fake L1 Accept pass through the l1 accept enable/disable logic. The FCLCT bit controls if Local Charged Triggers (LCT) from the SP\_FPGA are being sent to the backplane. The LCT is defines as Mode > 0 for the SP core output. The FCB bit controls the maximum value for the bunch counter to roll over. The L1Accept state machine is one-hot coded, so only one state bit could be equal to logical 1 at any time. For further details on the L1Accept state machine see Figure 1. There is also a copy of the L1Accept state machine in every other FPGAs, which is used for gating the Valid Pattern Counters.

**Table 43: CSR\_FCC Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	FCB	0	0	0	FCM	0	0	FCL	FCLCT	0	L1R	L1W	L1S	R
X	X	X	FCB	X	X	X	FCM	X	X	FCL	FCLCT	X	X	X	X	W

Here:

- X – Don't care bit;
- FCM = 1 (default) / 0 – VME (default) / CCB Fast Control Mode;
- FCB = 1 / 0 (default) – LHC->3563 / SPS->923 (default) BX counter mode;
- FCL = 1 / 0 (default) – FC\_SFRUN/CCB\_L1ACC (default) is a source for the FC\_L1ACC signal, see the CSR\_SFC register description for details on FC\_SFRUN.
- FCLCT = 1 / 0 (default) – enable / disable (default) Local Charge Trigger;
- L1S = 1 – L1Accept state machine is in the L1A\_STOP state;
- L1W = 1 – L1Accept state machine is in the L1A\_WAIT state;
- L1R = 1 – L1Accept state machine is in the L1A\_RUN state.

With the FCT bit set the FRONT\_FPGAs and the SP\_FPGA are configured to perform a loopback test via SP02 Transition and Test Boards to validate the Drift Tube output and input connections. Test patterns preloaded into the Test FiFOs of F1 and F2 chips are injected into the data path, then pass via the DT output connector to the Transition Board outputs, loop back via the Test Board to the Transition Board inputs, pass via the DT input connector, and get registered into the SP\_FPGA Barrel Spy FIFOs (DAT\_SFB). With the FCT bit set there is a change in the data format for the FRONT\_FPGA DAT\_TF register: otherwise ignored timing bits become valid, see the DAT\_TF register description for details.

**Table 44: CSR\_FCC Data Format for FRONT\_FPGA and SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	FCB	0	0	0	0	0	FCT	0	0	0	L1R	L1W	L1S	R
X	X	X	FCB	X	X	X	X	X	FCT	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- FCB = 1 / 0 (default) – LHC->3563 / SPS->923 (default) BX counter mode;
- FCT = 1 / 0 (default) – DT Loopback Test configuration enabled / disabled (default);
- L1S = 1 – L1A\_STOP state of the L1Accept state machine;
- L1W = 1 – L1A\_WAIT state of the L1Accept state machine;
- L1R = 1 – L1A\_RUN state of the L1Accept state machine.

**Table 45: CSR\_FCC Data Format for DDU\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	FCB	0	0	0	0	0	0	0	0	0	L1R	L1W	L1S	R
X	X	X	FCB	X	X	X	X	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- FCB = 1 / 0 (default) – LHC->3563 / SPS->923 (default) BX counter mode;
- L1S = 1 – L1A\_STOP state of the L1Accept state machine;
- L1W = 1 – L1A\_WAIT state of the L1Accept state machine;
- L1R = 1 – L1A\_RUN state of the L1Accept state machine.

### CSR\_LEC – Link Error Counters

This read-only register monitors all possible link errors. The TLK2501 synchronization procedure, when the MPC switches TLK2501 transmitters into idle mode for 128 bunch crossings, always precedes the normal operation. Normal receiving operation assumes RXSD

and RXDV to be High and RXER to be Low. To facilitate monitoring of error conditions, any combination of RXSD, RXDV and RXER other than normal is detected and countered. Error conditions are accumulated over time, starting from the previous synchronization procedure. Counter stops when it reaches its maximum value. The counters are reset on L1\_Reset and begin count errors after Alignment FIFO has been enabled for writing. Addressing the ACT\_LER register provides an alternative reset option.

**Table 46: CSR\_LEC Data Format**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SLC3	SLC2	SLC1	SLC0	CEC3	CEC2	CEC1	CEC0	EWC7	EWC6	EWC5	EWC4	EWC3	EWC2	EWC1	EWC0
Signal Loss Counter				Carrier Extend Counter				Error Word Counter							

Here:

- EWC [7:0] – TLK2501 Error Word Counter (RXDV == High, RXER == High);
- CEC [3:0] – TLK2501 Carrier Extend Counter (RXDV == Low, RXER == High);
- SLC [3:0] – FINISAR optical receiver Signal Loss Counter (RXSD goes Low).

### CSR\_AF – Alignment FIFO Status

This read-only register shows the number of words currently sitting in the Alignment FIFO (AF).

In the FRONT\_FPGA Alignment FIFOs are used to switch from the receiver clock domain to the system clock domain and to compensate for different optical link latencies. Different links may show different AF word counts after link synchronization procedure has been performed. Dispersion of word count values corresponds to the dispersion of link latencies. To time-in all active links and minimize the overall AF latency one has to adjust the CSR\_AFD register value and perform L1 Resets until the minimal AF value amongst all active links becomes equal to 2 or 3. The FRONT\_FPGA AF runs at 80 MHz clock, so the AF latency in bunch crossings is twice less the AFC value.

**Table 47: CSR\_AF Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AFFF	AFEF	0	0	0	0	0	AFC8	AFC7	AFC6	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0
Flags		Alignment FIFO Word Count													

Here:

- AFC [8:0] = 0...511 – Alignment FIFO Read Word Count;
- AFFF – Alignment FIFO Full Flag or AFC = 511;
- AFEF – Alignment FIFO Empty Flag.

In the SP\_FPGA Alignment FIFOs perform the same function for the barrel muon data. The difference is that to time-in barrel data one has to adjust only the CSR\_AFD value, no L1 Resets are required. The SP\_FPGA AF runs at 40 MHz clock, so the AF latency in bunch crossings equals to the AFC value.

**Table 48: CSR\_AF Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AFFF	AFEF	0	0	0	0	0	0	0	0	0	0	AFC3	AFC2	AFC1	AFC0
Flags		Alignment FIFO Word Count													

Here:

- AFC [3:0] = 0...15– Alignment FIFO Read Word Count;
- AFFF – Alignment FIFO Full Flag or AFC = 15;
- AFEF – Alignment FIFO Empty Flag.

#### CSR\_TF – Test FIFO Status

This read-only register shows word count currently loaded into the Test FIFO (TF) and FIFO Flags. The maximum available TF capacity is 1024 16-bit words. Register address is applicable to FRONT\_FPGA (3 each), DDU\_FPGA (1 each) and SP\_FPGA (3 each).

**Table 49: CSR\_TF Data Format**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFFF	TFEF	0	0	0	TFC10	TFC9	TFC8	TFC7	TFC6	TFC5	TFC4	TFC3	TFC2	TFC1	TFC0
Flags		Test FIFO Word Count													

Here:

- TFC [10:0] = 0...1024 – Test FIFO Word Count;
- TFFF – Test FIFO Full Flag or TFC = 1024;
- TFEF – Test FIFO Empty Flag.

#### CSR\_SF – Spy FIFO Status

This read-only register shows the number of words currently sitting in the Spy FIFO (SF). One would probably want to know this value before setting up the BLT read cycle to read out the SF content. Maximum available SF capacity is 1024 16-bit words. Register address is applicable to FRONT\_FPGA (3 each), DDU\_FPGA (1 each) and SP\_FPGA (3 each).

**Table 50: CSR\_SF Data Format**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFFF	SFEF	RXDV	RXER	0	SFC10	SFC9	SFC8	SFC7	SFC6	SFC5	SFC4	SFC3	SFC2	SFC1	SFC0
Flags		RX Status		Spy FIFO Word Count											

Here:

- SFC [10:0] = 0..1024 – Spy FIFO Word Count;
- SFFF – Spy FIFO Full Flag or 1024 Word Count;
- SFEF – Spy FIFO Empty Flag;
- RXDV, RXER – TLK2501 Receiver Status for the last data read out from the Spy FIFO.

#### CSR\_PF – Pipeline FIFO Status

This read-only register shows the number of words currently loaded to the Pipeline FIFO (PF) and FIFO Flags. The maximum available PF capacity is 512 72-bit words. Since the Pipeline FIFO runs at the doubled BX frequency, its word count equals to (PFD +1) \* 2, where PFD is a CSR\_PFD register setting. Register address is applicable to FRONT\_FPGA. The PF content is not available for direct reads. Use Spy FIFO to grab data of interest at the SF inputs or outputs.

**Table 51: CSR\_PF Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PFFF	PFEF	0	0	0	0	PFC9	PFC8	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0
Flags		Pipeline FIFO Word Count													

Here:

- PFC [9:0] = 0...512 – Pipeline FIFO Word Count;
- PFFF – Pipeline FIFO Full Flag or PFC = 512;
- PFEF – Pipeline FIFO Empty Flag.

#### CSR\_DF – DAQ FIFO Status

This read-only register shows the number of words currently loaded to the DAQ FIFO (DF) and link error status for muon data words. The maximum available DF capacity is 8192 18-bit words. Register address is applicable to DDU\_FPGA.

**Table 52: CSR\_DF Data Format for DDU\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DFFF	DFEF	DFC13	DFC12	DFC11	DFC10	DFC9	DFC8	DFC7	DFC6	DFC5	DFC4	DFC3	DFC2	DFC1	DFC0
Flags		DAQ FIFO Word Count													

Here:

- DFC [13:0] = 0...8192 – DAQ FIFO Word Count;
- DFFF – Pipeline FIFO Full Flag or DFC = 8192;
- DFEF – Pipeline FIFO Empty Flag;

#### CSR\_LF – L1 Accept FIFO Status

This read-only register shows the number of words currently loaded to the L1 Accept FIFO (LF) and FIFO Flags. The maximum available LF capacity is 1024 54-bit words. Register address is applicable to FRONT\_FPGA.

**Table 53: CSR\_LF Data Format**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LFFF	LFEF	0	0	0	LFC10	LFC9	LFC8	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
Flags		L1 Accept FIFO Word Count													

Here:

- LFC [10:0] = 0...1024 – L1 Accept FIFO Word Count;
- LFFF – L1 Accept FIFO Full Flag or LFC = 1024;
- LFEF – L1 Accept FIFO Empty Flag.

#### CSR\_RBW – Ring Buffer Write Pointer

This read-only register shows the current address of the Ring Buffer Write Pointer. Ring Buffer is a 54 bit x 1024 word temporary storage for muon data, before they are get reformatted and put in the DAQ FIFO for readout. The register is valid for FRONT\_FPGA and used for firmware debugging.

**Table 54: CSR\_RBW Data Format**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	RBW9	RBW8	RBW7	RBW6	RBW5	RBW4	RBW3	RBW2	RBW1	RBW0
Ring Buffer Write Pointer Address															

Here:

- RBW [9:0] = 0...1023– Ring Buffer Write Pointer Address.

### CSR\_RBR – Ring Buffer Read Pointer

This read-only register shows the current position of the Ring Buffer Read Pointer. Ring Buffer is a 54 bit x 1024 word temporary storage for muon data, before they are get reformatted and put in the DAQ FIFO for readout. The register is valid for FRONT\_FPGA and used for firmware debugging.

**Table 55: CSR\_RBR Data Format**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	RBR9	RBR8	RBR7	RBR6	RBR5	RBR4	RBR3	RBR2	RBR1	RBR0
Ring Buffer Read Pointer Address															

Here:

- RBR [9:0] = 0...1023 – Ring Buffer Read Pointer.

### CSR\_SF1 – F1 Spy FIFO Status

This read-only registers, one register per F1 EMU muon, return the F1 Spy FIFO (SF1) Flags and the SF1 Word Count. The maximum available SF1 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 56: CSR\_SF1 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF1FF	SF1EF	0	0	0	SF1C10	SF1C9	SF1C8	SF1C7	SF1C6	SF1C5	SF1C4	SF1C3	SF1C2	SF1C1	SF1C0
Flags		F1 Spy FIFO Word Count													

Here:

- SF1C [10:0] = 0...1024 – F1 Spy FIFO Word Count;
- SF1FF – F1 Spy FIFO Full Flag or SF1C = 1024;
- SF1EF – F1 Spy FIFO Empty Flag.

### CSR\_SF2 – F2 Spy FIFO Status

This read-only registers, one register per F2 EMU muon, return the F2 Spy FIFO (SF2) Flags and the SF2 Word Count. The maximum available SF2 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 57: CSR\_SF2 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF2FF	SF2EF	0	0	0	SF2C10	SF2C9	SF2C8	SF2C7	SF2C6	SF2C5	SF2C4	SF2C3	SF2C2	SF2C1	SF2C0
Flags		F2 Spy FIFO Word Count													

Here:

- SF2C [10:0] = 0...1024 – F2 Spy FIFO Word Count;
- SF2FF – F2 Spy FIFO Full Flag or SF2C = 1024;
- SF2EF – F2 Spy FIFO Empty Flag.

### CSR\_SF3 – F3 Spy FIFO Status

This read-only registers, one register per F3 EMU muon, return the F3 Spy FIFO (SF3) Flags and the SF3 Word Count. The maximum available SF3 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 58: CSR\_SF3 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF3FF	SF3EF	0	0	0	SF3C10	SF3C9	SF3C8	SF3C7	SF3C6	SF3C5	SF3C4	SF3C3	SF3C2	SF3C1	SF3C0
Flags				F3 Spy FIFO Word Count											

Here:

- SF3C [10:0] = 0...1024 – F3 Spy FIFO Word Count;
- SF3FF – F3 Spy FIFO Full Flag or SF3C = 1024;
- SF3EF – F3 Spy FIFO Empty Flag.

### CSR\_SF4 – F4 Spy FIFO Status

This read-only registers, one register per F4 EMU muon, return the F4 Spy FIFO (SF4) Flags and the SF4 Word Count. The maximum available SF4 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 59: CSR\_SF4 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF4FF	SF4EF	0	0	0	SF4C10	SF4C9	SF4C8	SF4C7	SF4C6	SF4C5	SF4C4	SF4C3	SF4C2	SF4C1	SF4C0
Flags				F4 Spy FIFO Word Count											

Here:

- SF4C [10:0] = 0...1024 – F4 Spy FIFO Word Count;
- SF4FF – F4 Spy FIFO Full Flag or SF4C = 1024;
- SF4EF – F4 Spy FIFO Empty Flag.

### CSR\_SF5 – F5 Spy FIFO Status

This read-only registers, one register per F5 EMU muon, return the F5 Spy FIFO (SF5) Flags and the SF5 Word Count. The maximum available SF5 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 60: CSR\_SF5 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF5FF	SF5EF	0	0	0	SF5C10	SF5C9	SF5C8	SF5C7	SF5C6	SF5C5	SF5C4	SF5C3	SF5C2	SF5C1	SF5C0
Flags				F5 Spy FIFO Word Count											

Here:

- SF5C [10:0] = 0...1024 – F5 Spy FIFO Word Count;

- SF5FF – F5 Spy FIFO Full Flag or SF5C = 1024;
- SF5EF – F5 Spy FIFO Empty Flag.

### CSR\_SFE – EMU Spy FIFO Status

This read-only register, common for all EMU muons, returns the FE Spy FIFO (SFE) Flags and the SFE Word Count. The maximum available SFE capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA.

**Table 61: CSR\_SFE Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFEFF	SFEFF	0	0	0	SFEC10	SFEC9	SFEC8	SFEC7	SFEC6	SFEC5	SFEC4	SFEC3	SFEC2	SFEC1	SFEC0
Flags		FE Spy FIFO Word Count													

Here:

- SFEC [10:0] = 0...1024 – FE Spy FIFO Word Count;
- SFEFF – FE Spy FIFO Full Flag or SFEC = 1024;
- SFEEF – FE Spy FIFO Empty Flag.

### CSR\_LNK – Link Control/Status

This register provides static link control and status directly to and from both Finisar and TLK2501 transceivers' pins. Read-only upper byte shows receiver status, while lower byte provides access to control pins. Under the normal operational conditions register value equals to 0x0511 for a receiving link and equals to 0x0014 for a transmitting link. When TSEN is asserted High, results of pseudorandom bit stream tests can be monitored on the RXER output. A High on this terminal indicates that valid PRBS is being received. The PRBS test counter counts (RXER goes Low) events, when TSEN is High. It stops, when reaches its maximum value of 31. Counter reset is provided through addressing to the ACT\_LER register.

When the TLK2501 device is disabled (DVEN is set to "0") the corresponding ready/busy link status is masked off and does not contribute to the overall FRONT\_FPGA fast monitoring status.

**Table 62: CSR\_LNK Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
TEC4	TEC3	TEC2	TEC1	TEC0	RXDV	RXER	RXSD	0	TSEN	LPEN	DVEN	0	TXEN	TXER	TXDI	R
X	X	X	X	X	X	X	X	X	TSEN	LPEN	DVEN	X	TXEN	TXER	TXDI	W

Here:

- X – Don't care bit for writes;
- TXDI = 1/0 – Disable / Enable (default) the FINISAR optical Transmitter;
- {TXEN, TXER} = {Transmit Enable, Error Coding} – Transmit Data Control:
  - {TXEN, TXER} = {0,0} – Transmit Idle Character (0xC5BC or 0x50BC);
  - {TXEN, TXER} = {0,1} – Transmit Carrier Extend (0xF7F7);
  - {TXEN, TXER} = {1,0} – Transmit Normal Data Character -> default
  - {TXEN, TXER} = {1,1} – Transmit Error Propagation (0xFEFE);
- DVEN = 1/0 – Enable (default) / Disable the TLK2501 Device;
- LPEN = 1/0 – Enable / Disable (default) the TLK2501 Loop mode;

- TSEN = 1/0 – Enable / Disable (default) the TLK2501 Pseudorandom Bit Stream (PRBS) Test ;
  - RXSD = 1/0 – Signal Detect/No Signal from FINISAR optical receiver;
  - { RXDV, RXER } = { Receive Data Valid, Receive Error } – Receive Status Signals
    - {RXDV, RXER} = {0,0} – Receive Idle Character (0xC5BC or 0x50BC);
    - {RXDV, RXER} = {0,1} – Receive Carrier Extend (0xF7F7);
    - {RXDV, RXER} = {1,0} – Receive Normal Data Character;
    - {RXDV, RXER} = {1,1} – Receive Error Propagation (0xFEFE);
- TEC [4:0] – PRBS Test Error Counter;

### CSR\_AFD - Alignment FIFO Read Delay

In the FRONT\_FPGA this read/write register controls delaying of the AF read enable signal after an L1 Reset occurs. In fact, the total delay calculates as (64 + CSR\_AFD Value) bx after an L1 Reset. The register is used to optimize the MPC-to-SP data path latency budget.

**Table 63: CSR\_AFD Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	AFD6	AFD5	AFD4	AFD3	AFD2	AFD1	AFD0
Alignment FIFO Read Delay															

Here:

- X – don't care bit for writes and zero for reads
- AFD [6:0] = 0...127 – AF resumes reads on the (64+1... 64+127) bunch crossing after an L1 Reset has been received. The register default value on power-up is 112, which gives the default delay of 176 bunch crossings.

In the SP\_FPGA this read/write register controls the AF latency in bunch crossings. The latency is updated on either AF reset command, see the ACT\_XFR register description for detail, or any write command to this register.

**Table 64: CSR\_AFD Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	AFD3	AFD2	AFD1	AFD0
Alignment FIFO Read Delay															

Here:

- X – don't care bit for writes and zero for reads
- AFD [3:0] = 0...15 – AF write-to-read delay in bunch crossings. The register default value on power-up is 0.

### CSR\_TFC – Test FIFO Configuration

This read/write register defines data injection points, amount of data to be injected and whether injected patterns get written back to the TF.

There are two injection points in the FRONT\_FPGA and three injection points in the SP\_FPGA.

The default register settings are used to run a link test with data patterns, similar to the MPC-SP one. The difference is that the SP can drive 15 optical outputs to test its 15 optical

inputs at once, while one MPC is capable to drive only 3 optical cables. As for the rest, the procedure is quite similar, i.e. the user:

- connects 15 SP outputs to the 15 inputs of the same or another SP;
- configures the CSR\_LNK register, if needed;
- sets the CSR\_FCC into a local fast control mode, in order not to interfere with other modules in the same crate, if only one SP is under tests;
- addresses ACT\_FCC to issue L1 Reset and perform link alignment procedure;
- loads the DAT\_TF register with the test patterns in the same format, as he would do it for the MPC;
- compensates for the data path latency (the optical cable length, the AF word count, and the PF word count, if the SF is hooked up to its output) by configuring the CSR\_SFC registers accordingly;
- runs the CCB\_TPSP command;
- reads back the DAT\_SF content and compares it with the original test patterns.

For the TFT = 1, when the TLK2501 transmitter is the test pattern destination, BC0 and BX0 timing bits are picked dynamically from the ccb bunch counter, running at the CCB backplane timing. It is done to prevent the Out-of-Synch condition to occur, once the link bunch counter has been tuned during the alignment procedure.

For the TFA = 1, when test patterns are injected in the incoming link data stream at the AF output, BC0 and BX0 bits are picked dynamically from the link data. Again, it is done to prevent the Out-of-Synch condition to occur, once the link bunch counter has been tuned during the alignment procedure.

**Table 65: CSR\_TFC Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFL	X	TFA	TFT	X	X	X	TFW8	TFW7	TFW6	TFW5	TFW4	TFW3	TFW2	TFW1	TFW0
Loop		Injection Points					Test FIFO Window								

Here:

- X – don't care bit for writes and zero for reads;
- TFW [8:0] = 0...511 – if TFM bit is set, then inject test patterns for 1...512 bunch crossings on the next CCB\_TPSP / FC\_TFRUN command, default value is 0;
- TFL = 1/0 – TF Loopback option: inject and write back data into the TF / just inject data into the destination circuit (default);
- TFA = 1/0 – enable / disable (default) injecting test data at the AF output;
- TFT = 1/0 – enable / disable (default) injecting test data into the TLK2501 transmitter.

**Table 66: CSR\_TFC Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFL	TFB	TFE	TFT	X	X	X	TFW8	TFW7	TFW6	TFW5	TFW4	TFW3	TFW2	TFW1	TFW0
Loop	Injection points						Test FIFO Window								

Here:

- X – don't care bit for writes and zero for reads;
- TFW [8:0] = 0...511 – if TFM bit is set, then inject test patterns for 1...512 bunch crossings on the next CCB\_TPSP / FC\_TFRUN command, default value is 0;

- TFL = 1/0 – TF Loopback option: inject and write back data into the TF / just inject data into the destination circuit (default);
- TFE = 1/0 – enable / disable (default) injecting EMU muon test data (simulates EMU track stubs) from the EMU Test FIFOs: DAT\_TF1/ DAT\_TF2/ DAT\_TF3/ DAT\_TF4/ DAT\_TF5/ DAT\_TFE;
- TFB = 1/0 – enable / disable (default) injecting Barrel muon test data (simulates Barrel track stubs) from the Barrel Test FIFOs: DAT\_TFB;
- TFT = 1/0 – enable / disable (default) injecting Track test data (simulates SP core output) from the Test FIFOs: DAT\_TF.

**CSR\_SFC – Spy FIFO Configuration**

In the VME\_FPGA this register defines the delay inserted between the CCB test commands and the FC\_SFRUN command on the internal FC bus, see Table 2. The delay is intended to compensate for the time required for the corresponding test data to reach the Spy FIFO input. The delay is not applicable to the CCB\_L1ACC command. The register also determines if request for data is one-time or persistent. Power-up default state for this register is 0x0000.

**Table 67: CSR\_SFC Data Format for VME\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFM	SFRL	SFRS	SFRM	SFRT	X	SFD9	SFD8	SFD7	SFD6	SFD5	SFD4	SFD3	SFD2	SFD1	SFD0
Mode	Requests					Spy FIFO Delay Setting									

Here:

- X – don’t care bit for writes and zero for reads;
- SFD [9:0] = 0 (default)...1023 - Spy FIFO starts writing data, when 1...1024 bunch crossings have passed after the requested event;
- SFRT = 1/0 (default) – store/don’t store data on the next CCB\_TPTMB command;
- SFRM = 1/0 (default) – store/don’t store data on the next CCB\_TPMPC command;
- SFRS = 1/0 (default) – store/don’t store data on the next CCB\_TPSP command;
- SFRL = 1/0 (default) – store/don’t store data on the next CCB\_L1ACC command;
- SFM = 1/0 (default) – persistent/one-time request. Persistent request stores data on all events that followed. One-time request stores data on the next event only and self-resets after that.

In the FRONT\_FPGA this register defines the data source for the Spy FIFO input and the number of beam crossings to be stored upon receiving the FC\_SFRUN command. Note that the actual number of 16-bit words, saved in the Spy FIFO is twice as big, since each beam crossing data consists of two frames.

**Table 68: CSR\_SFC Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFS	X	X	X	X	X	X	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
Source							Spy FIFO Bunch Crossing Count								

Here:

- X – Don’t care bit for writes and zero for reads;

- SF [8:0] = 0 (default)...511 – Spy FIFO grabs data from 1...512 bunch crossings;
- SFS = 1 / 0 (default) – connects the Spy FIFO input to the Pipeline FIFO output / input (default) to grab data.

**Table 69: CSR\_SFC Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFS	X	SFM1	SFM0	X	X	X	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
Source		Data Source													Spy FIFO Bunch Crossing Count

Here:

- X – Don’t care bit for writes and zero for reads;
- SF [8:0] = 0 (default)...511 – Spy FIFO grabs data from 1...512 bunch crossings;
- SFM [1:0] = 0...3 – MS Spy FIFO (DAT\_SFM) spies on the PT[1] (default) output data;
- SFS = 1 / 0 (default) – connects the Spy FIFO (DAT\_SF), Barrel Spy FIFO (DAT\_SFB) and MS Spy FIFO (DAT\_SFM) inputs to the Pipeline FIFO output / input (default) to grab data.

**CSR\_PFD – Pipeline FIFO Data Delay**

This read/write register controls data delay in the Pipeline FIFO to compensate for L1 Accept latency. Default value on power-up is 0.

**Table 70: CSR\_PFD Data Format for FRONT\_FPGA and SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	PFD7	PFD6	PFD5	PFD4	PFD3	PFD2	PFD1	PFD0
															Pipeline FIFO Data Delay

Here:

- X – Don’t care bit for writes and zero bit for reads;
- PFD = 0...255 – PF delays data for 1... 256 bunch crossings or up to 6.4 μsec.

**CSR\_DFC – DAQ FIFO Configuration**

This read/write register keeps the Event Configuration word that includes: a number of bunch crossings to readout, a zero suppression option, an active FRONT\_FPGA mask, and an active barrel muon mask. The register default value on power-up is 0x1FC. The DDU\_FPGA collects only data that are prescribed by the register value.

**Table 71: CSR\_DFC Data Format for DDU\_FPGA.**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	BM	F5M	F4M	F3M	F2M	F1M	ZS	DFB2	DFB1	DFB0
						Barrel Mask	FRONT_FPGA Mask bits					Zero Supp.	BX count		

Here:

- X – Don’t care bit for writes;
- DFB [2:0] = 0...7 – DAQ FIFO stores data from 0...7 bunch crossings. The DFB default value is 4.
- ZS – Zero Suppression bit. If set to 1 (default), then only valid LCTs and tracks are collected.

- F5M... F1M –FRONT\_FPGA Mask bits. If any mask bit is set to 1 (default), then the corresponding FRONT\_FPGA is queried for muon stub data;
- BM – Barrel Mask bit. If any mask bit set to 1, then the SP\_FPGA is queried for the corresponding barrel muon stub data.

**CSR\_SCC – SP Core Configuration**

This read/write register keeps the SP core configuration options.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1\_STOP state. The above implies executing the following two VME commands:

- VW/MA/CSR\_FCC/W/0x0100 -> put the SP02 under the VME control
- VM/MA/ACT\_FCC/W/0x00C8 -> issue the bx reset command

before addressing the data register.

**Table 72: CSR\_SCC Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	BXE

Here:

- X – Don’t care bit for writes and zero for reads;
- BXE = 1(default) / 0 – Bunch crossing analyzer enable (default) / disable.

**CSR\_TFB – Barrel Test FIFO Status**

This read-only register, one per MB input link, returns the Barrel Test FIFO (TFB) Flags and the TFB Word Count. The maximum available TFB capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA.

**Table 73: CSR\_TFB Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFBFF	TFBEF	0	0	0	TFBC10	TFBC9	TFBC8	TFBC7	TFBC6	TFBC5	TFBC4	TFBC3	TFBC2	TFBC1	TFBC0
Flags				Barrel Test FIFO Word Count											

Here:

- TFBC [10:0] = 0...1024 – Barrel Test FIFO Word Count;
- TFBFF – Barrel Test FIFO Full Flag or TFBC = 1024;
- TFBEF – Barrel Test FIFO Empty Flag.

**CSR\_SFB – Barrel Spy FIFO Status**

This read-only register, ne per MB input link, returns the Barrel Spy FIFO (SFB) Flags and the SFB Word Count. The maximum available SFB capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA.

**Table 74: CSR\_SFB Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFBBF	SFBEF	0	0	0	SFBC10	SFBC9	SFBC8	SFBC7	SFBC6	SFBC5	SFBC4	SFBC3	SFBC2	SFBC1	SFBC0
Flags		Barrel Spy FIFO Word Count													

Here:

- SFBC [10:0] = 0...1024 – MS Spy FIFO Word Count;
- SFBBF – MS Spy FIFO Full Flag or SFBC = 1024;
- SFBEF – MS Spy FIFO Empty Flag.

**CSR\_SFM – Muon Sorter Spy FIFO Status**

This read-only register, one per SP output track, returns the MS Spy FIFO (SFM) Flags and the SFM Word Count. The maximum available SFM capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA.

**Table 75: CSR\_SFM Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFMFF	SFMEF	0	0	0	SFMC10	SFMC9	SFMC8	SFMC7	SFMC6	SFMC5	SFMC4	SFMC3	SFMC2	SFMC1	SFMC0
Flags		MS Spy FIFO Word Count													

Here:

- SFMC [10:0] = 0...1024 – MS Spy FIFO Word Count;
- SFMFF – MS Spy FIFO Full Flag or SFMC = 1024;
- SFMEF – MS Spy FIFO Empty Flag.

**CSR\_TF1 – F1 Test FIFO Status**

This read-only registers, one register per F1 EMU muon, return the F1 Test FIFO (TF1) Flags and the TF1 Word Count. The maximum available TF1 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 76: CSR\_TF1 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF1FF	TF1EF	0	0	0	TF1C10	TF1C9	TF1C8	TF1C7	TF1C6	TF1C5	TF1C4	TF1C3	TF1C2	TF1C1	TF1C0
Flags		F1 Test FIFO Word Count													

Here:

- TF1C [10:0] = 0...1024 – F1 Test FIFO Word Count;
- TF1FF – F1 Test FIFO Full Flag or TF1C = 1024;
- TF1EF – F1 Test FIFO Empty Flag.

**CSR\_TF2 – F2 Test FIFO Status**

This read-only registers, one register per F2 EMU muon, return the F2 Test FIFO (TF2) Flags and the TF2 Word Count. The maximum available TF2 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 77: CSR\_TF2 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF2FF	TF2EF	0	0	0	TF2C10	TF2C9	TF2C8	TF2C7	TF2C6	TF2C5	TF2C4	TF2C3	TF2C2	TF2C1	TF2C0
Flags		F2 Test FIFO Word Count													

Here:

- TF2C [10:0] = 0...1024 – F2 Test FIFO Word Count;
- TF2FF – F2 Test FIFO Full Flag or TF2C = 1024;
- TF2EF – F2 Test FIFO Empty Flag.

### CSR\_TF3 – F3 Test FIFO Status

This read-only registers, one register per F3 EMU muon, return the F3 Test FIFO (TF3) Flags and the TF3 Word Count. The maximum available TF3 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 78: CSR\_TF3 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF3FF	TF3EF	0	0	0	TF3C10	TF3C9	TF3C8	TF3C7	TF3C6	TF3C5	TF3C4	TF3C3	TF3C2	TF3C1	TF3C0
Flags		F3 Test FIFO Word Count													

Here:

- TF3C [10:0] = 0...1024 – F3 Test FIFO Word Count;
- TF3FF – F3 Test FIFO Full Flag or TF3C = 1024;
- TF3EF – F3 Test FIFO Empty Flag.

### CSR\_TF4 – F4 Test FIFO Status

This read-only registers, one register per F4 EMU muon, return the F4 Test FIFO (TF4) Flags and the TF4 Word Count. The maximum available TF4 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 79: CSR\_TF4 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF4FF	TF4EF	0	0	0	TF4C10	TF4C9	TF4C8	TF4C7	TF4C6	TF4C5	TF4C4	TF4C3	TF4C2	TF4C1	TF4C0
Flags		F4 Test FIFO Word Count													

Here:

- TF4C [10:0] = 0...1024 – F4 Test FIFO Word Count;
- TF4FF – F4 Test FIFO Full Flag or TF4C = 1024;
- TF4EF – F4 Test FIFO Empty Flag.

### CSR\_TF5 – F5 Test FIFO Status

This read-only registers, one register per F5 EMU muon, return the F5 Test FIFO (TF5) Flags and the TF5 Word Count. The maximum available TF5 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 80: CSR\_TF5 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF5FF	TF5EF	0	0	0	TF5C10	TF5C9	TF5C8	TF5C7	TF5C6	TF5C5	TF5C4	TF5C3	TF5C2	TF5C1	TF5C0
Flags				F5 Test FIFO Word Count											

Here:

- TF5C [10:0] = 0...1024 – F5 Test FIFO Word Count;
- TF5FF – F5 Test FIFO Full Flag or TF5C = 1024;
- TF5EF – F5 Test FIFO Empty Flag.

### CSR\_TFE – EMU Test FIFO Status

This read-only register, common for all EMU muons, returns the FE Test FIFO (TFE) Flags and the TFE Word Count. The maximum available TFE capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP\_FPGA only.

**Table 81: CSR\_TFE Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFE FF	TFE EF	0	0	0	TFEC10	TFEC9	TFEC8	TFEC7	TFEC6	TFEC5	TFEC4	TFEC3	TFEC2	TFEC1	TFEC0
Flags				FE Test FIFO Word Count											

Here:

- TFEC [10:0] = 0...1024 – FE Test FIFO Word Count;
- TFEFF – FE Test FIFO Full Flag or TFEC = 1024;
- TFE EF – FE Test FIFO Empty Flag.

## Address Counter Register Group

### CNT\_LPL – Local Phi LUT Address Counter Low

This read/write register carries current value of the local phi LUT address counter 16 Least Significant Bits (LSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all local LUTs serviced by the FRONT\_FPGA and auto-increments on every access to any DAT\_LP register in a chip. The counter can be reset with the ACT\_ACR command.

**Table 82: CNT\_LPL Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LA15	LA14	LA13	LA12	LA11	LA10	LA9	LA8	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0
Local Phi LUT Address Counter LSB															

Here:

- X – Don't care bit;
- LA [15:0] – Local Phi LUT Address Counter, 16 LSB.

### CNT\_LPH – Local Phi LUT Address Counter High

This read/write register carries current value of the local phi LUT address counter 3 Most Significant Bits (MSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all local LUTs serviced by the FRONT\_FPGA and auto-

increments on every access to any DAT\_LP register in a chip. The counter can be reset with the ACT\_ACR command.

**Table 83: CNT\_LPH Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	LA18	LA17	LA16
													LP LUT AC MSB		

Here:

- X – Don't care bit;
- LA [18:16] – Local Phi LUT Address Counter, 3 MSB.

#### **CNT\_GLL – Global LUTs Address Counter Low**

This read/write register carries current value of the global LUTs address counter 16 Least Significant Bits (LSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all global LUTs serviced by the FRONT\_FPGA and auto-increments on every access to any DAT\_GP/DAT\_DT/DAT\_GE register in a chip. The counter can be reset with the ACT\_ACR command.

**Table 84: CNT\_GLL Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GA15	GA14	GA13	GA12	GA11	GA10	GA9	GA8	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0
Global LUTs Address Counter LSB															

Here:

- X – Don't care bit for writes and zero for reads;
- GA [15:0] – Global LUTs Address Counter, 16 LSB.

#### **CNT\_GLH – Global LUTs Address Counter High**

This read/write register carries current value of the global LUTs address counter 3 Most Significant Bits (MSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all global LUTs serviced by the FRONT\_FPGA and auto-increments on every access to any DAT\_GP/DAT\_DT/DAT\_GE register in a chip. The counter can be reset with the ACT\_ACR command.

**Table 85: CNT\_GLH Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	GA18	GA17	GA16
													GL LUTs AC MSB		

Here:

- X – Don't care bit for writes and zero for reads;
- GA [18:16] – Global LUTs Address Counter, 3 MSB.

#### **CNT\_PTL – PT LUTs Address Counter Low**

This read/write register carries current value of the PT LUTs address counter 16 Least Significant Bits (LSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all PT LUTs serviced by the SP\_FPGA and auto-increments on

every access to any DAT\_PT register in a chip. The counter can be reset with the ACT\_ACR command.

**Table 86: CNT\_PTL Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PTA15	PTA14	PTA13	PTA12	PTA11	PTA10	PTA9	PTA8	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
PT LUTs Address Counter LSB															

Here:

- X – Don’t care bit for writes and zero for reads;
- PTA [15:0] – PT LUTs Address Counter, 16 LSB.

**CNT\_PTH – PT LUTs Address Counter High**

This read/write register carries current value of the global LUTs address counter 3 Most Significant Bits (MSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all PT LUTs serviced by the SP\_FPGA and auto-increments on every access to any DAT\_PT register in a chip. The counter can be reset with the ACT\_ACR command.

**Table 87: CNT\_PTH Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	PTA20	PTA19	PTA18	PTA17	PTA16
PT LUTs AC MSB															

Here:

- X – Don’t care bit for writes and zero for reads;
- PTA [20:16] – Global LUTs Address Counter, 5 MSB.

**CNT\_ETA – Eta Address Counter**

This read/write register carries current value of the Eta Min/Max/Window/Offset Address Counter, as shown in the table below. The default register value on power-up is zero. The counter auto-increments on every access to the DAT\_ETA register. The counter can be reset with the ACT\_ACR command.

**Table 88: CNT\_ETA Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	ETA4	ETA3	ETA2	ETA1	ETA0
ETA Address Counter															

Here:

- X – Don’t care bit for writes and zero for reads;
- ETA [4:0] = 0...25 – Eta Min/Max/Window/Offset Address Counter.

**Data Register Group**

**DAT\_TF1 – F1 Test FIFO Data**

This write-only register in the SP\_FPGA, one register per F1 EMU muon, keeps the F1 Test FIFO (TF1) data. The TF1 data can be injected into the data path on the fast control FC\_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and

synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR\_TFC register description.

**Table 89: DAT\_TF1 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame	
Quality [3:0]											Global Phi [11:0]						FR1
CSC ID [3:0]				Global Phi Bend[4:0]				Global Eta[6:0]						FR2			

Here:

- Global Phi [11:0] = 0...4095;
- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15;
- CSC ID [3:0] = 1...9.

### DAT\_TF2 – F2 Test FIFO Data

This write-only register in the SP\_FPGA, one register per F2 EMU muon, keeps the F2 Test FIFO (TF2) data. The TF2 data can be injected into the data path on the fast control FC\_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR\_TFC register description.

**Table 90: DAT\_TF2 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame	
Quality [3:0]											Global Phi [11:0]						FR1
CSC ID [3:0]				Global Phi Bend[4:0]				Global Eta[6:0]						FR2			

Here:

- Global Phi [11:0] = 0...4095;
- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15;
- CSC ID [3:0] = 1...9.

### DAT\_TF3 – F3 Test FIFO Data

This write-only register in the SP\_FPGA, one register per F3 EMU muon, keeps the F3 Test FIFO (TF3) data. The TF3 data can be injected into the data path on the fast control FC\_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR\_TFC register description.

**Table 91: DAT\_TF3 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame	
Quality [3:0]											Global Phi [11:0]						FR1
X	X	X	X	Global Phi Bend[4:0]				Global Eta[6:0]						FR2			

Here:

- X – don't care bit;
- Global Phi [11:0] = 0...4095;

- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15.

#### DAT\_TF4 – F4 Test FIFO Data

This write-only register in the SP\_FPGA, one register per F4 EMU muon, keeps the F4 Test FIFO (TF4) data. The TF4 data can be injected into the data path on the fast control FC\_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR\_TFC register description.

**Table 92: DAT\_TF4 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
X	X	X	X	Global Phi Bend[4:0]				Global Eta[6:0]				FR2				

Here:

- X – don't care bit;
- Global Phi [11:0] = 0...4095;
- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15.

#### DAT\_TF5 – F5 Test FIFO Data

This write-only register in the SP\_FPGA, one register per F5 EMU muon, keeps the F5 Test FIFO (TF5) data. The TF5 data can be injected into the data path on the fast control FC\_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR\_TFC register description.

**Table 93: DAT\_TF5 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
X	X	X	X	Global Phi Bend[4:0]				Global Eta[6:0]				FR2				

Here:

- X – don't care bit;
- Global Phi [11:0] = 0...4095;
- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15.

#### DAT\_TFE – EMU Test FIFO Data

This write-only register in the SP\_FPGA keeps the FE Test FIFO data, which carries VP and SE bits for all fifteen EMU muons. The content of the TFE can be injected into the data path on the fast control FC\_TFRUN command to test the SP core functionality. On how to configure the testing process refer to the CSR\_TFC register description.

**Table 94: DAT\_TFE Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
X	F5 VP Flags			F4 VP Flags			F3 VP Flags			F2 VP Flags			F1 VP flags			FR1
X	F5 SE Flags			F4 SE Flags			F3 SE Flags			F2 SE Flags			F1 SE flags			FR2

Here:

- X – don't care bit;
- Valid Pattern flags, one per EMU muon;
- Synch Error flags, one per EMU muon.

#### DAT\_LP – Local Phi LUT Data

This read/write registers provides access to the Local Phi LUT content. The LP LUT data format is shown in Table 95. Read/write transfers are performed on the LP LUT current address defined by the CNT\_LPL and CNT\_LPH values; after that the counter auto-increments. Note, that the local phi LUT address counter is common to all three muons, serviced by the FRONT\_FPGA. Register address is applicable to the FRONT\_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1\_STOP state. The above implies executing the following two commands:

- VW/MA/CSR\_FCC/W/0x0100 -> under VME control
- VM/MA/ACT\_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

**Table 95: DAT\_LP Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LPB5	LPB4	LPB3	LPB2	LPB1	LPB0	LP9	LP8	LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0
Local Phi Bend						Local Phi									

Here:

- LP [9:0] = 0...1023 – Local Phi.
- LPB [5:0] = 0...31 – Local Phi Bend.

#### DAT\_GP – Global Phi LUT Data

This read/write registers provides access to the Global Phi LUT content. The GP LUT data format is shown in the table below. Read/write transfers are performed on the GP LUT current address defined by the CNT\_GLL and CNT\_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT\_FPGA. Register address is applicable to the FRONT\_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1\_STOP state. The above implies executing the following two commands:

- VW/MA/CSR\_FCC/W/0x0100 -> under VME control
- VM/MA/ACT\_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

**Table 96: DAT\_GP Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
Global Phi															

Here:

- X – don't care bit, returns zero on reads;
- GP [11:0] = 0...4095 – Global Phi.

#### DAT\_DT – Drift Tube Global Phi LUT Data

This read/write registers provides access to the Drift Tube Global Phi LUT content. The DT LUT data format is shown in the table below. Read/write transfers are performed on the DT LUT current address defined by the CNT\_GLL and CNT\_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT\_FPGA. Register address is applicable to the FRONT\_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1\_STOP state. The above implies executing the following two commands:

- VW/MA/CSR\_FCC/W/0x0100 -> under VME control
- VM/MA/ACT\_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

**Table 97: DAT\_DT Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	DT11	DT10	DT9	DT8	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
Drift Tube Global Phi															

Here:

- X – don't care bit, returns zero on reads;
- DT [11:0] = 0...4095 – Drift Tube Global Phi.

#### DAT\_GE – Global Eta LUT Data

This read/write registers provides access to the Global Eta LUT content. The GE LUT data format is shown in the table below. Read/write transfers are performed on the GE LUT current address defined by the CNT\_GLL and CNT\_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT\_FPGA. Register address is applicable to the FRONT\_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1\_STOP state. The above implies executing the following two commands:

- VW/MA/CSR\_FCC/W/0x0100 -> under VME control
- VM/MA/ACT\_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

**Table 98: DAT\_GE Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	GE11	GE10	GE9	GE8	GE7	GE6	GE5	GE4	GE3	GE2	GE1	GE0
Global Phi Bend									Global Eta						

Here:

- X – don't care bit, returns zero on reads;
- GE [6:0] = 0...127 – Global Eta;
- GE[11:7] = 0...31 – Global Phi Bend;

#### DAT\_PT – PT LUT Data

This read/write registers provides access to the PT LUT content. The PT LUT data format is shown in the table below. Read/write transfers are performed on the PT LUT current address defined by the CNT\_PTL and CNT\_PTH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three PT LUTs serviced by the SP\_FPGA.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1\_STOP state. The above implies executing the following two commands:

- VW/MA/CSR\_FCC/W/0x0100 -> under VME control
- VM/MA/ACT\_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

**Table 99: DAT\_PT Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RVC	RQ1	RQ0	RR4	RR3	RR2	RR1	RR0	FVC	FQ1	FQ0	FR4	FR3	FR2	FR1	FR0
Rear Muon Data								Front Muon Data							

Here:

- RVC – Rear muon Valig Charge;
- RQ[1:0] – Rear muon Quality;
- RR[4:0] – Rear muon Rank;
- FVC – Front muon Valig Charge;
- FQ[1:0] – Front muon Quality;
- FR[4:0] – Front muon Rank.

#### DAT\_ETA – Eta Min/Max/Win Data

This read/write register provides access to the Eta register file content. The register file keeps data for Eta Minimum – 8 words, Eta Maximum – 8 words, Eta Window – 6 words and Eta Offset – 4 words setting, which totals to 26 data words. The CNT\_ETA counter provides indexed access to the register content; see the CNT\_ETA register description for details.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1\_STOP state. The above implies executing the following two VME commands:

- VW/MA/CSR\_FCC/W/0x0100 -> put the SP02 under the VME control
- VM/MA/ACT\_FCC/W/0x00C8 -> issue the bx reset command

before addressing the data register.

**Table 100: DAT\_ETA Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	ETAP7	ETAP6	ETAP5	ETAP4	ETAP3	ETAP2	ETAP1	ETAP0
Eta Parameters															

Here:

- X – don't care bit, reads back as zero;
- ETAP [7:0] = 0...127 for Eta Minimum;
- ETAP [7:0] = 0...127 for Eta Maximum;
- ETAP [7:0] = 0...255 for Eta Window;
- ETAP [7:0] = 0...127 for Eta Offset;

**DAT\_VPC – Valid Pattern Counter Data**

This read-only register is intended to monitor incoming muon stub rate for each link by counting the number of Valid Pattern bits at the Alignment FIFO output in the FRONT\_FPGAs and outgoing track rate for each SP core output by counting the number of Mode>0 decisions in the SP\_FPGA. The counter control follows that of the event counter: it is reset on the FC\_L1RES and FC\_ECRES commands and enabled when data taking state machine is in L1A\_RUN state, see Figure 1 for details on L1Accept control. An internal 42-bit binary counter is read out in a floating point format as  $VPM * 2^{VPP}$ . The DAT\_VPC address is applicable to FRONT\_FPGAs and SP\_FPGA.

**Table 101: DAT\_VP Data Format for FRONT\_FPGA and SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VPM10	VPM9	VPM8	VPM7	VPM6	VPM5	VPM4	VPM3	VPM2	VPM1	VPM0	VPP4	VPP3	VPP2	VPP1	VPP0
Mantissa											Power of 2				

Here:

- VPM [10:0] = 0...2047 - Mantissa;
- VPP [4:0] = 0...31 – Power of 2.

**DAT\_SF1 – F1 Spy FIFO Data**

This read-only register in the SP\_FPGA, one register per F1 EMU muon, returns data from the F1 Spy FIFO (SF1). The SF1 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR\_SFC register description.

**Table 102: DAT\_SF1 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]					Global Eta[6:0]						FR2	

Here:

- Global Phi [11:0] = 0...4095;

- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15;
- CSC ID [3:0] = 1...9.

**DAT\_SF2 – F2 Spy FIFO Data**

This read-only register in the SP\_FPGA, one register per F2 EMU muon, returns data from the F2 Spy FIFO (SF2). The SF2 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR\_SFC register description.

**Table 103: DAT\_SF2 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]				Global Eta[6:0]								FR2

Here:

- Global Phi [11:0] = 0...4095;
- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15;
- CSC ID [3:0] = 1...9.

**DAT\_SF3 – F3 Spy FIFO Data**

This read-only register in the SP\_FPGA, one register per F3 EMU muon, returns data from the F3 Spy FIFO (SF3). The SF3 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR\_SFC register description.

**Table 104: DAT\_SF3 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
0	0	0	0	Global Phi Bend[4:0]				Global Eta[6:0]								FR2

Here:

- Global Phi [11:0] = 0...4095;
- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15.

**DAT\_SF4 – F4 Spy FIFO Data**

This read-only register in the SP\_FPGA, one register per F4 EMU muon, returns data from the F4 Spy FIFO (SF4). The SF4 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and

BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR\_SFC register description.

**Table 105: DAT\_SF4 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]								Global Phi [11:0]								FR1
0	0	0	0	Global Phi Bend[4:0]				Global Eta[6:0]								FR2

Here:

- Global Phi [11:0] = 0...4095;
- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15.

#### DAT\_SF5 – F5 Spy FIFO Data

This read-only register in the SP\_FPGA, one register per F5 EMU muon, returns data from the F5 Spy FIFO (SF5). The SF5 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR\_SFC register description.

**Table 106: DAT\_SF5 Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]								Global Phi [11:0]								FR1
0	0	0	0	Global Phi Bend[4:0]				Global Eta[6:0]								FR2

Here:

- Global Phi [11:0] = 0...4095;
- Global Eta [6:0] = 0...127;
- Global Phi Bend [11:7] = 0...31;
- Quality [3:0] = 0...15.

#### DAT\_SFE – EMU Spy FIFO Data

This read-only register in the SP\_FPGA returns data from the FE Spy FIFO, which carries VP, SE and timing marks for all fifteen EMU muons. Each FRONT\_FPGA sends a pair of timing marks to the SP\_FPGA, but all active muon links should be timed on L1 Reset, so that the timing is the same for all FRONT\_FPGAs. What the Spy FIFO captures is a logical OR of five BC0 and five BX0 timing signals. On how to configure the spying process refer to the CSR\_SFC register description.

**Table 107: DAT\_SFE Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
BX0	F5 VP Flags			F4 VP Flags			F3 VP Flags			F2 VP Flags			F1 VP flags			FR1
BC0	F5 SE Flags			F4 SE Flags			F3 SE Flags			F2 SE Flags			F1 SE flags			FR2

Here:

- Valid Pattern flags, one per EMU muon;
- Synch Error flags, one per EMU muon;
- BX0 – Bunch Counter LSB;

- BC0 – Bunch Crossing Zero mark.

**DAT\_TF – Test FIFO Data**

VME cycles addressed to this write-only register load data in the Test FIFO (TF). Address is valid for FRONT\_FPGA (3 each) and SP\_FPGA (3 each).

The output of the FRONT\_FPGA TF is normally connected to the TLK2501 transmitter to provide a source of data patterns for link tests. Alternatively, during data taking phase TF data may be injected in the data steam, substituting the Alignment FIFO output for one or more bunch crossings. TF destination is defined by the CSR\_TFC register. CCB fast control signals (TBD) are responsible for test pattern injection. Table 108 shows the TF data format, which exactly follows the MPC – SP two-frame data format.

Data loaded into the TF cannot be verified by reading it back, since FIFO reads are destructive. Addressing to the CSR\_TF register provides an indirect verification method of the current TF word count.

**Table 108: DAT\_TF Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]						FR1	
CSC ID [3:0]				X	X	SE	L/R	CLCT Pattern ID [7:0]						FR2		

**Table 109: DAT\_TF Data Format for FRONT\_FPGA during the DT Interface Loopback Test**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]						FR1	
CSC ID [3:0]				BC0	BX0	BX1	L/R	CLCT Pattern ID [7:0]						FR2		

Here:

- X – Don’t care bit;
- VP – Valid Pattern flag;
- Quality - the more hits the higher track Quality;
- CLCT Pattern # - the 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit;
- Wire Group ID - the 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111;
- CSC ID - the 4-bit CSC ID indicates the chamber # and runs from 1 to 9;
- SE - Synchronization Error bit;
- L/R - the Left/Right bend bit indicates whether the track is heading towards lower or higher strip number;
- CLCT Pattern ID - For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber.

**Table 110: DAT\_TF Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
RSV	SE	HL	CHRG	FR	SIGN	Eta [4:0]				Phi [4:0]				FR1		
Mode [3:0]				Delta23 Phi [3:0]				Delta12 Phi [7:0]				FR2				

Here:

- Phi [4:0] is the Azimuth Coordinate;
- Eta [4:0] is the Pseudorapidity, the Eta [4:1] is a part of the PT LUT address;
- SIGN – the Delta Phi Sign bit is a part of the PT LUT address;
- FR – the Front/Rear bit;
- CHRG – the Muon Charge or Sign bit;
- HL – the Halo bit;
- SE – the Synchronization Error bit;
- RSV – the Reserved bit;
- Delta12 Phi [7:0] is a part of the PT LUT address;
- Delta23 Phi [3:0] is a part of the PT LUT address;
- Mode [3:0] is a part of the PT LUT address.

#### **DAT\_SF – Spy FIFO Data – add cnt info after PF**

VME cycles addressed to this read-only register return data from the Spy FIFO (SF). Preferred method of reading the SF content is setting up the BLT read. Before reading the SF content it is useful to check the SF status, by addressing to the CSR\_SF register, which would return the current SF word count. Address is valid for FRONT\_FPGA (3 each) and SP\_FPGA (3 each).

The FRONT\_FPGA SF input could be connected to either Pipeline FIFO Input or Pipeline FIFO output, as defined by the CSR\_SFC register. Data format for both sources is shown in table below. The process of collecting data into the SF is regulated by fast control commands.

Every input muon link has a Bunch Counter associated with it and driven by link timing marks. On power-up and after CCB\_BXRES, or CCB\_LIRES commands the Bunch Counter gets preloaded with a 0xFFE=4094 value. On the next clock upon receiving BC0 mark it starts counting from 1 and up. The Bunch counter rolls over to zero count, when it reaches its maximum value, which are 923 for the beam test at SPS and 3563 for LHC operations.

In a properly timed-in setup, all link Bunch Counters should be in synch. This ensures that at any given moment the SP02 gets data tagged by the same bunch crossing number. The SP02 can only diagnose if the data on different links is timed-in or not, using its Spy FIFO triggered by the CCB\_L1ACC signal, see the CSR\_SFC and DAT\_SF register descriptions for detail. It is the Peripheral Crate electronics that actually performs a data tagging procedure, while the SP02 gets link data with already embedded timing marks.

**Table 111: DAT\_SF Data Format for FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]				FR1			
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]				FR2				

Here:

- VP – Valid Pattern flag;
- Quality - the more hits the higher track Quality;
- CLCT Pattern # - the 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit;
- Wire Group ID - the 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111;
- CSC ID - the 4-bit CSC ID indicates the chamber # and runs from 1 to 9;
- BC0 - the Bunch Crossing Zero flag marks bunch zero data;
- BX0 - the least significant bit of Bunch Crossing Number (BXN ranges from 0 to 3563);
- SE - Synchronization Error bit;
- L/R - the Left/Right bend bit indicates whether the track is heading towards lower or higher strip number;
- CLCT Pattern ID - For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber.

The SP\_FPGA SF input could be connected to either Pipeline FIFO Input or Pipeline FIFO output, as defined by the CSR\_SFC register. Data format for both sources is shown in table below. The process of collecting data into the SF is regulated by fast control commands.

**Table 112: DAT\_SF Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
RSV	SE	HL	CHRG	FR	SIGN	Eta [4:0]				Phi [4:0]				FR1		
Mode [3:0]			Delta23 Phi [3:0]			Delta12 Phi [7:0]						FR2				

Here:

- Phi [4:0] is the Azimuth Coordinate;
- Eta [4:0] is the Pseudorapidity, the Eta [4:1] is a part of the PT LUT address;
- SIGN – the Delta Phi Sign bit is a part of the PT LUT address;
- FR – the Front/Rear bit;
- CHRG – the Muon Charge or Sign bit;
- HL – the Halo bit;
- SE – the Synchronization Error bit;
- RSV – the Reserved bit;
- Delta12 Phi [7:0] is a part of the PT LUT address;
- Delta23 Phi [3:0] is a part of the PT LUT address;
- Mode [3:0] is a part of the PT LUT address.

**DAT\_DF – DAQ FIFO Data**

VME cycles addressed to this read-only register retrieve event data from the DAQ FIFO (DF). The data format has a header followed by a specified number of data blocks. Each block is composed of 3 muons, 2 frames per muon, see Table 113 for details. The SP header structure

follows the DMB header structure and starts with the number of data blocks or, in other words, the number of bunch crossings for which the muon data is presented. Two next words carry the L1 Accept or event number, and, finally, the fourth word is the bunch crossing counter reading for the first data block in the event. The header carries a specific signature of hexadecimal 0xF values to facilitate the separation of events. The data block format exactly follows the MPC-SP link format.

**Table 113: DAT\_DF Data Format for the FRONT\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word	Block
0xF			0xF			BC# – # of Bunch Crossings in Event									HD1	Header	
0xF			EC [11:0] – Event Counter 12 Less Significant Bits									HD2					
0xF			EC [23:12] – Event Counter 12 Most Significant Bits									HD3					
0xF			BC [11:0] – Bunch Crossing Counter value for data block 1									HD4					
VP	Quality [3:0]			CLCT Pattern # [3:0]			Wire Group ID [6:0]						M1FR1	Data Block 1			
CSC ID [3:0]			BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]						M1FR2				
VP	Quality [3:0]			CLCT Pattern # [3:0]			Wire Group ID [6:0]						M2FR1				
CSC ID [3:0]			BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]						M2FR2				
VP	Quality [3:0]			CLCT Pattern # [3:0]			Wire Group ID [6:0]						M3FR1				
CSC ID [3:0]			BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]						M3FR2				
VP	Quality [3:0]			CLCT Pattern # [3:0]			Wire Group ID [6:0]						M1FR1	Data Block BC#			
CSC ID [3:0]			BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]						M1FR2				
VP	Quality [3:0]			CLCT Pattern # [3:0]			Wire Group ID [6:0]						M2FR1				
CSC ID [3:0]			BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]						M2FR2				
VP	Quality [3:0]			CLCT Pattern # [3:0]			Wire Group ID [6:0]						M3FR1				
CSC ID [3:0]			BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]						M3FR2				

Here:

- VP – Valid Pattern flag
- Quality - the more hits the higher track Quality
- CLCT Pattern # - the 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit.
- Wire Group ID - the 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111.
- CSC ID - the 4-bit CSC ID indicates the chamber # and runs from 1 to 9.
- BC0 - the Bunch Crossing Zero flag marks bunch zero data
- BX0 - the least significant bit of Bunch Crossing Number (BXN ranges from 0 to 3563 in LHC mode and from 0 to 923 in SPS mode).
- SE - Synchronization Error bit
- L/R - the Left/Right bend bit indicates whether the track is heading towards lower or higher strip number
- CLCT Pattern ID - For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber.

**DAT\_TFB – Barrel Test FIFO Data**

This write-only register in the SP\_FPGA, one register per F1 EMU muon, keeps the F1 Test FIFO (TF1) data. The TF1 data can be injected into the data path on the fast control FC\_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR\_TFC register description. This read-only register in the SP\_FPGA, one per output track, returns data from the MS Spy FIFO, which carries track ID, MS winner bits, and the PT LUT output. If the ID is non-zero, it shows the input stub number used by the SP core logic to build the output track. Although there is a DAT\_SFM register for each output track, only one register at a time can be selected for spying on the PT LUT output data, refer to the CSR\_SFC register descriptions for details.

**Table 114: DAT\_TFB Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
X	X	Calib	Flag	X	X	X	Phi Bend [4:0]				X	Quality [2:0]		FR1		
X	X	X	X	Phi [11:0]											FR2	

Here:

- X – don't care bit
- Quality [2:0] = 0...7 – Muon Quality; For valid data Quality is always > 0;
- Phi Bend {4:0} – Phi Bend angle;
- Phi [11:0] – Azimuth Coordinate;
- Flag, if 1 then it is a second muon from previous bunch crossing;
- Calib – a DT special mode flag;
- BX [1:0] – two LSB of the DT bunch counter;
- BC0 – Bunch crossing zero flag.

**DAT\_SFB – Barrel Spy FIFO Data**

This read-only register in the SP\_FPGA, one per a barrel muon link, returns data from the Barrel Spy FIFO, which carries track stubs from the overlapping DT region. Refer to the CSR\_SFC register descriptions for details on how to configure the Barrel Spy FIFO.

**Table 115: DAT\_SFB Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
0	0	Calib	Flag	0	0	0	Phi Bend [4:0]				0	Quality [2:0]		FR1		
0	BC0	BX [1:0]		Phi [11:0]											FR2	

Here:

- Quality [2:0] = 0...7 – Muon Quality; For valid data Quality is always > 0;
- Phi Bend {4:0} – Phi Bend angle;
- Phi [11:0] – Azimuth Coordinate;
- Flag, if 1 then it is a second muon from previous bunch crossing;
- Calib – a DT special mode flag;
- BX [1:0] – two LSB of the DT bunch counter;
- BC0 – Bunch crossing zero flag.

When the CSR\_FCC/FCT bit is set and a loopback test is being performed on the DT outputs/inputs, the DAT\_SFB format changes. Since the Transition Board has 4 output connectors and only 2 input connectors, the user can loop back the DT output from only one FRONT\_FPGA (F1 or F2) at any given time.

**Table 116: DAT\_SFB/M1 Data Format for SP\_FPGA: DT loopback test option**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
0	0	ME1B_PHI[5:4]		0	0	0	ME1B_PHI0	ME1A_Q[2:0]			ME1A_ETA	0	ME1B_PHI[3:1]			FR1
ME1B_PHI[9:6]				ME1A_PHI[11:0]												FR2

**Table 117: DAT\_SFB/M2 Data Format for SP\_FPGA: DT loopback test option**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
0	0	ME1C_Q[2:1]		0	0	0	ME1C_PHI[10:6]					0	ME1C_Q0	ME1C_ETA	ME1C_PHI11	FR1
0	ME1A_BC0	ME1A_BX[1:0]		ME1C_PHI[5:0]				ME1B_Q[2:0]			ME1B_ETA	ME1B_PHI[11:10]			FR2	

Here:

- ME1A\_PHI [11:0] – FX/M1 muon azimuth coordinate, FX = F1 or F2;
- ME1B\_PHI [11:0] – FX/M2 muon azimuth coordinate, FX = F1 or F2;
- ME1C\_PHI [11:0] – FX/M3 muon azimuth coordinate, FX = F1 or F2;
- ME1A\_Q [2:0] – FX/M1 muon Quality, FX = F1 or F2;
- ME1B\_Q [2:0] – FX/M2 muon Quality, FX = F1 or F2;
- ME1C\_Q [2:0] – FX/M3 muon Quality, FX = F1 or F2;
- ME1A\_ETA – FX/M1 muon region flag, FX = F1 or F2;
- ME1B\_ETA – FX/M2 muon region flag, FX = F1 or F2;
- ME1C\_ETA – FX/M3 muon region flag, FX = F1 or F2;
- ME1A\_BX [1:0] – two LSBs of the FX/M1 bunch counter, FX = F1 or F2;
- ME1A\_BC0 – FX/M1 bunch crossing zero flag, FX = F1 or F2.

**DAT\_SFM – MS Spy FIFO Data**

This read-only register in the SP\_FPGA, one per output track, returns data from the MS Spy FIFO, which carries track ID, MS winner bits, and the PT LUT output. If the ID is non-zero, it shows the input stub number used by the SP core logic to build the output track. Although there is a DAT\_SFM register for each output track, only one register at a time can be selected for spying on the PT LUT output data, refer to the CSR\_SFC register descriptions for details.

**Table 118: DAT\_SFM Data Format for SP\_FPGA**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame	
0	MS_ID [3:1]			MB_ID [2:0]			ME4_ID[1:0]	ME3_ID [1:0]	ME2_ID [1:0]	ME1_ID [2:0]							FR1
Rear Muon PT LUT Data								Front Muon PT LUT Data									FR2

Here:

- MS\_ID [3:1] = Muon Sorter Winner bit positional code;
- For PT LUT Data format refer to the DAT\_PT register description;
- For the ID to firmware muon correspondence see table below.

**Table 119: Spy FIFO to Muon ID Correspondence**

Look for track stub into the Spy FIFO	Muon ID
SP/DAT_SF1/M1	ME1_ID = 1
SP/DAT_SF1/M2	ME1_ID = 2
SP/DAT_SF1/M3	ME1_ID = 3
SP/DAT_SF2/M1	ME1_ID = 4
SP/DAT_SF2/M2	ME1_ID = 5
SP/DAT_SF2/M3	ME1_ID = 6
SP/DAT_SF3/M1	ME2_ID = 1
SP/DAT_SF3/M2	ME2_ID = 2
SP/DAT_SF3/M3	ME2_ID = 3
SP/DAT_SF4/M1	ME3_ID = 1
SP/DAT_SF4/M2	ME3_ID = 2
SP/DAT_SF4/M3	ME3_ID = 3
SP/DAT_SF5/M1	ME4_ID = 1
SP/DAT_SF5/M2	ME4_ID = 2
SP/DAT_SF5/M3	ME4_ID = 3
SP/DAT_SFB/M1	MB_ID = 1
SP/DAT_SFB/M1 – next bx	MB_ID = 2
SP/DAT_SFB/M2	MB_ID = 3
SP/DAT_SFB/M2 – next bx	MB_ID = 4

**DAT\_RW – Data Transfer Bus Read/Write Register**

This register is used for backplane and internal data bus validation. It allows write/read cycles to be performed to/from each FPGA chip without affecting SP02 functionality in any way.

**Table 120: DAT\_RW Data Format**

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Validation Data Word															

## History

### Version 5.0 – Sep 01, 2003

- Clock routing changed due to patches:
  - Eliminated the osc\_clk input in the VME\_FPGA;
  - Eliminated the clk\_sel input in the VME\_FPGA;
  - Returned two DCMs: internal and external to the VME\_FPGA;
  - Eliminated the CSR\_CLK register in the VME\_FPGA;
  - Changed default value of the CSR\_CLK register in the FRONT\_FPGA from DCM to VCXO clock;
- Changed the CCB\_BC0 to DATA\_BC0 adjustment scheme:
  - Eliminated the CSR\_CCB register in the VME\_FPGA;
  - Added the CSR\_BCO register in the FRONT\_FPGA (with the same access address);
  - Changed format of the CSR\_OSY registers in the FRONT\_FPGA, now it displays the latched bunch counter value without calculating positive/negative offsets;

3. Added data taking state diagrams in the interface description;
4. Added the STS\_VPC (Valid Pattern Counter) register for each link in the FRONT\_FPGA;
5. Renamed ACT\_LER – Link Error Counters Resets to ACT\_LCR – Link Counter Resets, added the VPR bit to reset the STS\_VPC counter;
6. Fake L1Accept generated by CCB\_TPxxx commands is ORed with the CCB\_L1A line BEFORE the L1Accept delay, not AFTER;
7. Added intercept of the CCB\_TPTMB(0x24) command;
8. Changed the CSR\_SFC format in the VME\_FPGA;

### **Version 5.1 – Nov 25, 2003**

1. Changed the usage of the 39 and 3A access codes, Table 4. Previously identical data and program access is now split according to its function.
2. Changed the IDTB protocol from synchronous with a handshake to synchronous with a predetermined timing.
3. Added the CSR\_BF(0x36) and DAT\_BF(0x76) registers for the Barrel FIFO, Table 9;
4. Added the BF reset bit in the ACT\_XFR, Table 20;
5. Added the ACT\_ACR register description;
6. Changed the CSR\_LF address from 0x36 to 0x37, Table 9;
7. Changed the CSR\_RBW address from 0x37 to 0x38, Table 9;
8. Changed the CSR\_RBR address from 0x38 to 0x39, Table 9;
9. Eliminated the CNT\_GEL/CNT\_GEH/CNT\_GPL/CNT\_GPH registers description;
10. Added the CNT\_GLL/CNT\_GLH registers description.

### **Version 5.2 – Dec 10, 2003**

1. Added the DAT\_GP register description;
2. Added the DAT\_DT register description;
3. Added the DAT\_GE register description.

### **Version 5.3 – Dec 25, 2003**

1. Added the CNT\_PTL/CNT\_PTH registers description;
2. Added the DAT\_PT register description;
3. Modified the ACT\_ACR register description;
4. Modified the CSR\_AFD register description;
5. Added the CSR\_TFC register description;
6. Completely redefined CSR\_OSY for FRONT\_FPGA.

### **Version 5.6 – Mar 8, 2004**

1. Added the CSR\_F1/CSR\_F2/CSR\_F3/CSR\_F4/CSR\_F5 registers description;

2. Added the DAT\_F1/DAT\_F2/DAT\_F3/DAT\_F4/DAT\_F5 registers description;
3. Eliminated the STS\_CCB register description;
4. Changed the STS\_ANA register description;
5. Added the ACT\_FCC register description;
6. Eliminated the ACT\_TST register description, the ACT\_FCC took over this register;
7. Added the CSR\_FCM register description;
8. Changed the CSR\_TFC register description;
9. Eliminated the CSR\_L1D register description since this the CCB function;
10. Restricted access to DAT\_LP, DAT\_GP, DAT\_DT, DAT\_GE, DAT\_PT, DAT\_ETA, and CSR\_SCC registers

### **Version 5.7 – Jun 1, 2004**

1. Changed the STS\_ANA register description;
2. Added description of the QPLL lock LED;
3. Changed link data logic; now link data passes through SP02 logic unconditionally.
4. Changed the CCB\_CMD to FC\_CMD mapping.

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[i] CSC Track Finder Crate Specification, created by Mike Matveev and updated by Alex Madorsky, December 12, 2002; [http://www.phys.ufl.edu/~madorsky/TrackFinder/TF\\_backplane\\_v4.doc](http://www.phys.ufl.edu/~madorsky/TrackFinder/TF_backplane_v4.doc)  
[ii] ANSI/VITA 1.1-1997, American National Standard for VME64 Extensions.