

LUT Downloading and Verification Procedure

Downloading and verification procedure for ALL SP LUTs

The same procedure can be performed on any subset of SP LUTs or just one LUT.

1 LUT Downloading

Note. The Monitor FIFO (MF) keeps info on “where” and “what” has been downloaded as a 4-word record for each download. Each download procedure is monitored by the Monitor Finite State Machine (MFSM). The download procedure can use either multicast register addresses, like FA or MA, when a group of LUTs is being downloaded simultaneously, or a single register address, like SP, F2 or M1, when only one LUT is being downloaded.

Note. Almost any other VME cycle can be executed anywhere in between the specified cycles and it will not affect the CRC calculation in any way.

Exception:

- ACT_ACR/W terminates the current CRC calculation and starts a new MFSM monitor cycle;
- VM/ACT_HR/W/0x001 or VM/ACT_XFR/W/0x0100 terminates the current monitor cycle and resets the MF;
- DAT_”LUT” cycles different from the first cycle after ACR_ACR cycle may corrupt the CRC calculation.

1.1 (optional) SL/VM/MA/ACT_HR/W/0x0001 => sends Soft Reset

1.2 SL/VM/CSR_FCC/W/0x0100 => sets the SP under VME control

1.3 SL/VM/MA/ACT_XFR/W/0x0300 => resets MF & Verification FIFO (VF).

1.4 (optional) SL/VM/MA/CSR_MF/R/ => 0x4000 => checks the MF is empty.

1.5 (optional) SL/VM/MA/CSR_VF/R/ => 0x4000 => checks the VF is empty.

1.6 LP LUT Loading

1.6.1 SL/FA/MA/ACT_ACR/W/0x0003 => resets the Local & Global Address Counters in the FRONT_FPGAs.

1.6.2 (optional) SL/VM/MA/CSR_MF/R => 0x5000 => the MFSM is running and expects LP/GE/GP or DT LUT to be loaded, the MF is still empty.

1.6.3 SL/FA/MA/DAT_LP/W/DAT [ADDR==0] => the MFSM detects LP LUT is being loaded. The MFSM stores the current LUT address as a 1st word into the MF. This LUT address serves as a model for VME cycles that follow. The MFSM stops only when $(2^{19}-1)$ more matching the model cycles have passed. For all matching cycles (including the first one) the CRC is calculated.

1.6.4 (optional) SL/VM/MA/CSR_MF/R => 0x1001– the MFSM is running and keeps 1 word.

1.6.5 SL/FA/MA/DAT_LP/W/DAT [ADDR==1]

1.6.6 ...

1.6.7 ...

- 1.6.8 SL/FA/MA/DAT_LP/W/DAT [ADDR== $(2^{19}-1)$]
- 1.6.9 SL/FA/MA/DAT_LP/W/DAT [ADDR== 2^{19}] => the FM FSM detects the last LUT address is being loaded. The MFSM stores the last address data as a 2nd word in the MF, and calculated CRC as 3rd and 4th words.
- 1.6.10 (optional) SL/VM/MA/CSR_MF/R => 0x0004 => the MFSM is not running and keeps 4 words.

1.7 GP LUT Loading

- 1.7.1 SL/FA/MA/ACT_ACR/W/0x0003 => resets the Local & Global Address Counters in the FRONT_FPGAs.
- 1.7.2 (optional) SL/VM/MA/CSR_MF/R => 0x1004 => the MFSM is running and keeps 4 words from the previous LUT download; The MFSM expects LP/GE/GP or DT LUT to be loaded.
- 1.7.3 SL/FA/MA/DAT_GP/W/DAT [ADDR==0] => the MFSM detects GP LUT is being loaded. The MFSM stores the current LUT address as a 1st word into the MF. This LUT address serves as a model for VME cycles that follow. The MFSM stops only when $(2^{19}-1)$ more matching the model cycles have passed. For all matching cycles (including the first one) the CRC is calculated.
- 1.7.4 (optional) SL/VM/MA/CSR_MF/R => 0x1005 => the MFSM is running and keeps 5 words: 4 words from the previous download, and 1 word from the current one.
- 1.7.5 SL/FA/MA/DAT_GP/W/DAT [ADDR==1]
- 1.7.6 ...
- 1.7.7 ...
- 1.7.8 SL/FA/MA/DAT_GP/W/DAT [ADDR== $(2^{19}-1)$]
- 1.7.9 SL/FA/MA/DAT_GP/W/DAT [ADDR== 2^{19}] => the MFSM detects the last LUT address is being loaded. The MFSM stores the last address data as a 2nd word in the MF, and calculated CRC as 3rd and 4th words.
- 1.7.10 (optional) SL/VM/MA/CSR_MF/R => 0x0008 => the MFSM is not running and keeps 8 words from 2 downloads.

1.8 GE LUT Loading

- 1.8.1 SL/FA/MA/ACT_ACR/W/0x0003 => resets the Local & Global Address Counters in the FRONT_FPGAs.
- 1.8.2 (optional) SL/VM/MA/CSR_MF/R => 0x1008 => the MFSM is running and keeps 8 words from the previous LUT downloads; The MFSM expects LP/GE/GP or DT LUT to be loaded.
- 1.8.3 SL/FA/MA/DAT_GE/W/DAT [ADDR==0] => the MFSM detects GE LUT is being loaded. The MFSM stores the current LUT address as a 1st word into the MF. This LUT address serves as a model for VME cycles that follow. The MFSM stops only when $(2^{19}-1)$ more matching the model cycles have passed. For all matching cycles (including the first one) the CRC is calculated.
- 1.8.4 (optional) SL/VM/MA/CSR_MF/R => 0x1005 => the MFSM is running and keeps 9 words: 8 words from the previous downloads, and 1 word from the current one.

- 1.8.5 SL/FA/MA/DAT_GE/W/DAT [ADDR==1]
- 1.8.6 ...
- 1.8.7 ...
- 1.8.8 SL/FA/MA/DAT_GE/W/DAT [ADDR==(2¹⁹-1)]
- 1.8.9 SL/FA/MA/DAT_GE/W/DAT [ADDR== 2¹⁹] => the MFSM detects the last LUT address is being loaded. The MFSM stores the last address data as a 2nd word in the MF, and calculated CRC as 3rd and 4th words.
- 1.8.10 (optional) SL/VM/MA/CSR_MF/R => 0x000C => the MFSM is not running and keeps 0xC = 12 words from 3 downloads.

1.9 DT LUT Loading

- 1.9.1 SL/FA/MA/ACT_ACR/W/0x0003 => resets the Local & Global Address Counters in the FRONT_FPGAs.
- 1.9.2 (optional) SL/VM/MA/CSR_MF/R => 0x100C– the MFSM is running and keeps 0xC = 12 words from the previous LUT downloads; The MFSM expects LP/GE/GP or DT LUT to be loaded.
- 1.9.3 SL/FA/MA/DAT_DT/W/DAT [ADDR==0] => the MFSM detects DT LUT is being loaded. The MFSM stores the current LUT address as a 1st word into the MF. This LUT address serves as a model for VME cycles that follow. The MFSM stops only when (2¹⁹-1) more matching the model cycles have passed. For all matching cycles (including the first one) the CRC is calculated.
- 1.9.4 (optional) SL/VM/MA/CSR_MF/R => 0x100D– the MFSM is running and keeps 0xD = 13 words: 0xC = 12 words from the previous downloads, and 1 word from the current one.
- 1.9.5 SL/FA/MA/DAT_DT/W/DAT [ADDR==1]
- 1.9.6 ...
- 1.9.7 ...
- 1.9.8 SL/FA/MA/DAT_DT/W/DAT [ADDR==(2¹⁹-1)]
- 1.9.9 SL/FA/MA/DAT_DT/W/DAT [ADDR== 2¹⁹] => the MFSM detects the last LUT address is being loaded. The MFSM stores the last address data as a 2nd word in the MF, and calculated CRC as 3rd and 4th words.
- 1.9.10 (optional) SL/VM/MA/CSR_MF/R => 0x0010 => the MFSM is not running and keeps 0x10 = 16 words from 4 downloads.

1.10 PT LUT Loading

- 1.10.1 SL/SP/MA/ACT_ACR/W/0x0004 => resets the PT LUT Address Counter in the SP_FPGA.
- 1.10.2 (optional) SL/VM/MA/CSR_MF/R => 0x1010– the MFSM is running and keeps 0x10 = 16 words from the previous LUT downloads; The MFSM expects PT LUT is being loaded.
- 1.10.3 SL/SP/MA/DAT_PT/W/DAT [ADDR==0] => the MFSM detects PT LUT is being loaded. The MFSM stores the current LUT address as a 1st word into the MF. This LUT address serves as a model for VME cycles that follow. The MFSM stops only when (2²¹-1) more matching the model cycles have passed. For all matching cycles (including the first one) the CRC is calculated.

- 1.10.4 (optional) SL/VM/MA/CSR_MF/R => 0x1011– the MFSM is running and keeps 0x11 = 17 words: 0x10 = 16 words from the previous downloads, and 1 word from the current one.
- 1.10.5 SL/SP/MA/DAT_PT/W/DAT [ADDR==1]
- 1.10.6 ...
- 1.10.7 ...
- 1.10.8 SL/SP/MA/DAT_PT/W/DAT [ADDR== (2²¹-1)]
- 1.10.9 SL/SP/MA/DAT_PT/W/DAT [ADDR== 2²¹] => the MFSM detects the last LUT address is being loaded. The MFSM stores the last address data as a 2nd word in the MF, and calculated CRC as 3rd and 4th words.

2 MF Data Saving

- 2.1 SL/VM/MA/CSR_MF/R => 0x0014 => the MFSM is not running and keeps 0x14 = 20 words for 5 downloads.
- 2.2 Execute SL/VM/MA/DAT_MF/R (CSR_MF word count) times => 20 times => store LUT CRC in a SP”SL”_MF.dat file.

Now the MF LUT keeps CRC codes for all types of SP LUTs and LUT verification can be started...

3 LUT Verification

*Note. The Verification FIFO (VF) keeps info on verified LUTs as a 4-word record for each LUT. The Verification FSM (VFSM) picks a list of LUTs to be verified from the MF. If the 1st word in a record shows multicast addressing has been used for downloading, the VFSM runs sequentially through each LUT in the addressed group. **The verification passes if 2nd, 3rd and 4th words in the VF record match the corresponding words in the MF record.***

- 3.1 SL/VM/MA/ACT_LUT/W/0x0004 => starts LUT verification.
- 3.2 SL/VM/MA/CSR_VF/R => 0x100N => the VFSM is running and keeps N words. If executed periodically, the VF status shows the verification progress.
- 3.3 ...
- 3.4 ... Until found the VFSM is not running... any cycle to SP/F1/F2/F3/F4/F5 or DD_FPGA does not go through and terminates with bus error... VM/ACT_HR/W/0x001 or VM/ACT_XFR/W/0x0300 aborts the verification process and resets both the VF and MF... VM/ACT_XFR/W/0x0200 aborts the verification process and resets the VF...
- 3.5 ...
- 3.6 SL/VM/MA/CSR_VF/R => 0x20D8 => the verification process is over and the VF keeps 0xD8 = 216 words => 4 words x 54 LUTs. The LUTs are verified in the order they were downloaded:

The VFSM finds FA/MA/DAT_LP downloaded, so it verifies:
 F1/M1/DAT_LP, F1/M2/DAT_LP, F1/M3/DAT_LP,
 F2/M1/DAT_LP, F2/M2/DAT_LP, F2/M3/DAT_LP,
 F3/M1/DAT_LP, F3/M2/DAT_LP, F3/M3/DAT_LP,

F4/M1/DAT_LP, F4/M2/DAT_LP, F4/M3/DAT_LP,
F5/M1/DAT_LP, F5/M2/DAT_LP, F5/M3/DAT_LP,

then the VFSM finds FA/MA/DAT_GP downloaded, so it verifies:

F1/M1/DAT_GP, F1/M2/DAT_GP, F1/M3/DAT_GP,
F2/M1/DAT_GP, F2/M2/DAT_GP, F2/M3/DAT_GP,
F3/M1/DAT_GP, F3/M2/DAT_GP, F3/M3/DAT_GP,
F4/M1/DAT_GP, F4/M2/DAT_GP, F4/M3/DAT_GP,
F5/M1/DAT_GP, F5/M2/DAT_GP, F5/M3/DAT_GP,

then the VFSM finds FA/MA/DAT_GE downloaded, so it verifies:

F1/M1//DAT_GE, F1/M2//DAT_GE, F1/M3//DAT_GE,
F2/M1//DAT_GE, F2/M2//DAT_GE, F2/M3//DAT_GE,
F3/M1//DAT_GE, F3/M2//DAT_GE, F3/M3//DAT_GE,
F4/M1//DAT_GE, F4/M2//DAT_GE, F4/M3//DAT_GE,
F5/M1//DAT_GE, F5/M2//DAT_GE, F5/M3//DAT_GE,

then the VFSM finds FA/MA/DAT_DT downloaded, so it verifies:

F1/M1//DAT_DT, F1/M2//DAT_DT, F1/M3//DAT_DT,
F2/M1//DAT_DT, F2/M2//DAT_DT, F2/M3//DAT_DT,

finally, the VFSM finds SP/MA/DAT_PT downloaded, so it verifies:

SP/M1/DAT_PT, SP/M2/DAT_PT, SP/M3/DAT_PT.

4 VF Data Saving

- 4.1 Execute SL/VM/MA/DAT_VF/R (CSR_VF word count) times => 216 times => store verified LUT CRC in a file for analysis.

Verification procedure based of the previously saved monitor data

5 Loading MF Data

Note. LUT verification may be based on the previously saved MF data.

- 5.1 (optional) SL/VM/MA/ACT_HR/W/0x0001 => sends Soft Reset
- 5.2 SL/VM/CSR_FCC/W/0x0100 => sets SP under VME control
- 5.3 SL/VM/MA/ACT_XFR/W/0x0300 => resets MF & VF.
- 5.4 (optional) SL/VM/MA/CSR_MF/R/ => 0x4000 => checks the MF is empty
- 5.5 (optional) SL/VM/MA/CSR_VF/R/ => 0x4000 => checks the VF is empty
- 5.6 Execute SL/VM/MA/DAT_MF/W 20 times loading SP"SL"_MF.dat data

6 LUT Verification

Note. The Verification FIFO (VF) keeps info on verified LUTs as a 4-word record for each LUT. The list of LUTs to be verified the Verification FSM (VFMSM) picks from the MF. If the 1st word in a record shows multicast addressing has been used for downloading, the VFMSM runs sequentially through each LUT in the addressed group. **The verification passes if 2nd, 3rd and 4th words in the VF record match the corresponding words in the MF record.**

- 6.1 SL/VM/MA/ACT_LUT/W/0x0004 => starts LUT verification.
- 6.2 SL/VM/MA/CSR_VF/R => 0x100N => the VFMSM is running and keeps N words. If executed periodically, the VF status shows the verification progress.
- 6.3 ...
- 6.4 ... Until found the VFMSM is not running... any cycle to SP/F1/F2/F3/F4/F5 or DD_FPGA does not go through and terminates with bus error... VM/ACT_HR/W/0x001 or VM/ACT_XFR/W/0x0300 aborts the verification process and resets both the VF and MF... VM/ACT_XFR/W/0x0200 aborts the verification process and resets the VF...
- 6.5 ...
- 6.6 SL/VM/MA/CSR_VF/R => 0x20D8 => the verification process is over and the VF keeps 0xD8 = 216 words => 4 words x 54 LUTs. The LUTs are verified in the order they were downloaded:

The VFMSM finds FA/MA/DAT_LP downloaded, so it verifies:

F1/M1/DAT_LP, F1/M2/DAT_LP, F1/M3/DAT_LP,
 F2/M1/DAT_LP, F2/M2/DAT_LP, F2/M3/DAT_LP,
 F3/M1/DAT_LP, F3/M2/DAT_LP, F3/M3/DAT_LP,
 F4/M1/DAT_LP, F4/M2/DAT_LP, F4/M3/DAT_LP,
 F5/M1/DAT_LP, F5/M2/DAT_LP, F5/M3/DAT_LP,

then the VFMSM finds FA/MA/DAT_GP downloaded, so it verifies:

F1/M1/DAT_GP, F1/M2/DAT_GP, F1/M3/DAT_GP,
 F2/M1/DAT_GP, F2/M2/DAT_GP, F2/M3/DAT_GP,
 F3/M1/DAT_GP, F3/M2/DAT_GP, F3/M3/DAT_GP,
 F4/M1/DAT_GP, F4/M2/DAT_GP, F4/M3/DAT_GP,

F5/M1/DAT_GP, F5/M2/DAT_GP, F5/M3/DAT_GP,

then the VFMSM finds FA/MA/DAT_GE downloaded, so it verifies:

F1/M1//DAT_GE, F1/M2//DAT_GE, F1/M3//DAT_GE,
F2/M1//DAT_GE, F2/M2//DAT_GE, F2/M3//DAT_GE,
F3/M1//DAT_GE, F3/M2//DAT_GE, F3/M3//DAT_GE,
F4/M1//DAT_GE, F4/M2//DAT_GE, F4/M3//DAT_GE,
F5/M1//DAT_GE, F5/M2//DAT_GE, F5/M3//DAT_GE,

then the VFMSM finds FA/MA/DAT_DT downloaded, so it verifies:

F1/M1//DAT_DT, F1/M2//DAT_DT, F1/M3//DAT_DT,
F2/M1//DAT_DT, F2/M2//DAT_DT, F2/M3//DAT_DT,

finally, the VFMSM finds SP/MA/DAT_PT downloaded, so it verifies:

SP/M1/DAT_PT, SP/M2/DAT_PT, SP/M3/DAT_PT.

7 VF Data Saving

- 7.1 Execute SL/VM/MA/DAT_VF/R (CSR_VF word count) times => 216 times => store verified LUT CRC in a file for analysis.