**CSR_BID – Board Identifier Register**

**VME FPGA and SP FPGA**

This read-only register in the VME_FPGA and SP_FPGA keeps \{SP02, SP04/SP05\} and \{SP02_MC, SP04_MC\} board versions and board IDs. For SP02 and SP02_MC boards the BRD_ID is always zero.

**Table 1: CSR_BID Data Format for VME_FPGA and SP_FPGA**

<table>
<thead>
<tr>
<th>D15 D14 D13 D12 D11 D10 D9 D8</th>
<th>D7 D6 D5 D4 D3 D2 D1 D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0 0 0</td>
<td>0 0 0 0</td>
</tr>
<tr>
<td>BRD_VER[2:0]</td>
<td>BRD_ID[5:0]</td>
</tr>
</tbody>
</table>

Here:
- BRD_VER [2:0] = \{2, 4\} Boards Version: SP02 or SP04/SP05
- BRD_ID [5:0] = 1…31 Board number.

**FRONT FPGA**

This read-only register in the FRONT_FPGA keeps a MPC Link Identifier. On power-up the register defaults to all zeros. After an MPC-to-SP optical link has been successfully initialized by the TTC_L1RES command, the register keeps the MPC/Link number. Note, that the Link Number is hardware coded, while the MPC number is a value downloaded in the MPC CSR0 register. During TLK2501 loop back tests bit[15] = 1, Mx [1:0] (x=1,2,3) is a muon number, and Fy [2:0] (y=1,2,3,4,5) is a FRONT_FPGA number.

**Table 2: CSR_BID Data Format for FRONT_FPGA**

<table>
<thead>
<tr>
<th>D15 D14 D13 D12 D11 D10 D9 D8</th>
<th>D7 D6 D5 D4 D3 D2 D1 D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0 0 0</td>
<td>MPC # [5:0]</td>
</tr>
<tr>
<td>MPC_LINK_ID [7:0]</td>
<td>LINK # [1:0]</td>
</tr>
</tbody>
</table>

During SP Loop Back Tests

| 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0   |
| Fy | 0 0 | Mx[1:0] |

Here for MPC-to-SP links:
- MPC_LINK_ID [7:0] - MPC Link Identifier consists of:
  - LINK # [1:0] = 0 (default), 1,2,3 – MPC Link number;
  - MPC # [5:0] = 0 (default)…63 – MPC Crate number.

**DDU FPGA**

In the DDU_FPGA this downloadable register keeps information on the CSC side and sector number serviced by the SP and the SP current slot number. This data is passed to the DDU in the SP Event Record Header for unique identification of the readout stream.

**Table 3: CSR_BID Data Format for DDU_FPGA**

<table>
<thead>
<tr>
<th>D15 D14 D13 D12 D11 D10 D9 D8</th>
<th>D7 D6 D5 D4 D3 D2 D1 D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X X X X</td>
<td>SP_LADR [3:0]</td>
</tr>
<tr>
<td>SP_ERSV [2:0]</td>
<td>SP_PADR [4:0]</td>
</tr>
<tr>
<td>SP_LADR [3:0]</td>
<td>SP_ERSV [2:0]</td>
</tr>
<tr>
<td>SP_PADR [4:0]</td>
<td>SP_PADR [4:0]</td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit, reads back as zero;
- SP_LADR [3:0] – SP Logical Address (power-up default is 0 indicating a non-initialized register) consists of:
  - MEZ = 0 (-Z) / 1 (+Z) – EMU Side;
  - MES_ID [2:0] – EMU 60° Sector number;
- SP_ERSV [2:0] = 0,…,7 – SP Event Record Structure Version (Read-only)
  o SP_ERSV = 0 => Jun 14, 2006, Version 4.2;
  o SP_ERSV = 1 => Jul 06, 2007, Version 5.1;
  o SP_ERSV = 2 => TBD;
  o SP_ERSV = 3 => TBD;
  o SP_ERSV = 4 => TBD;
  o SP_ERSV = 5 => TBD;
  o SP_ERSV = 6 => TBD;
  o SP_ERSV = 7 => TBD;

- SP_PADR [4:0] = 6…11, 16…21 – SP Physical Address or Slot Number in the TF crate. The power-up default is 0 indicating a non-initialized register. SP_PADR gets initialized to the actual Slot Number on a write command to this register, which is supposed to load SP_LADR value – the only writable register field.

**ACT_LCR – Link Counter Reset**

**FRONT FPGA**

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 25 ns reset pulse to selected counter(s) described under the CSR_LNK, CSR_LEC and DAT_VPC headings.

**Table 4: ACT_LCR Data Format for FRONT_FPGA**

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VPR</td>
<td>TER</td>
<td>SLR</td>
<td>CER</td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit;
- EWR – TLK2501 Error Word Counter Reset in the CSR_LEC register (R XDV == HIGH, RXER == HIGH);
- CER – TLK2501 Carrier Extend Counter Reset in the CSR_LEC register (R XDV == LOW, RXER == HIGH);
- SLR – FINISAR optical receiver Signal Loss Counter Reset in the CSR_LEC register (RXSD goes LOW);
- TER – PRBS Test Error Counter Reset in the CSR_LNK register;
- VPR – Valid Pattern Counter Reset in the DAT_VPC register.

**SP FPGA**

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 25 ns reset pulse to selected counter(s) described under DAT_VPC heading.

**Table 5: ACT_LCR Data Format for SP_FPGA**

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>OCR</td>
<td>TCR</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VPR</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit;
- VPR – Valid Pattern Counter Reset in the DAT_VPC register;
− TCR – Track Counter\(^1\) Reset (readable via DAQ only);
− OCR – Orbit Counter Reset (readable via DAQ only).

\(^1\) Regarding Track Counter and Orbit Counter functionality details refer to:
http://www.phys.ufl.edu/~uvarov/SP05/LU-SP2DDU_Event_Record_Structure_v51.pdf