ACT_LUT – Calculate LUT CRC

VME write cycle to this write-only register starts the Verification FSM, which may run up to 10 sec. During that period of time, the VME access to all SP FPGA, except VME_FPGA is disabled: any VME command addressed to FA[F1,F2,F3,F4,F5]_FPGA, DD_FPGA, and SP_FPGA will terminate with VME Bus Error (BERR*).

The result of verification and Verification FSM status can be monitored or viewed via the CSR_VF or/and DAT_VF registers.

ACT_LUT Data Format for VME_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VER</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit;
- VER – Verify => runs Verification FSM that calculates and verifies LUT ID/CRC according to a LUT list picked from the Monitor FIFO. Note that DAT_MF register should be loaded or auto loaded with LUT ID/CRC patterns before executing this command.

ACT_XFR – FIFO Reset

Writing Logic ONE to a specified bit of this write-only register results in sending a reset pulse to the corresponding FIFO(s). The register address is applicable to the VME_FPGA, FRONT_FPGA, DDU_FPGA and SP_FPGA.

VME FPGA

ACT_XFR Data Format for VME_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
<td>VFR</td>
<td>MFR</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit;
- MFR – Monitor FIFO and Monitor FSM Reset (Init);
- VFR – Verification FIFO and Verification FSM Reset (Init).
FRONT FPGA

Table 4: ACT_XFR Data Format for FRONT_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>LFR</td>
<td>PFR</td>
<td>SFR</td>
<td>TFR</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit;
- TFR – All Test FIFOs Reset (Init);
- SFR – All Spy FIFOs Reset (Init);
- PFR – Pipeline FIFO Reset (Init);
- LFR – L1 Accept FIFO Reset (Init) is equivalent to FC_L1RES signal. It also resets Ring Buffer Read and Ring Buffer Write Pointers.

DDU FPGA

Table 5: ACT_XFR Data Format for DDU_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DFR</td>
<td>LFR</td>
<td>X</td>
<td>SFR</td>
<td>TFR</td>
<td>X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit;
- TFR – Test FIFO Reset (Init);
- SFR – Spy FIFO Reset (Init);
- LFR – L1 Accept FIFO Reset (Init) is equivalent to FC_L1RES signal. It also resets readout and FMM state machines;
- DFR – DAQ (VME) Readout FIFO Reset (Init).

SP FPGA

Table 6: ACT_XFR Data Format for SP_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>LFR</td>
<td>PFR</td>
<td>SFR</td>
<td>TFR</td>
<td>AFR</td>
<td></td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit;
- AFR – Barrel Alignment FIFO Reset (Init);
- TFR – All Test FIFOs Reset (Init);
- SFR – All Spy FIFOs Reset (Init);
- PFR – Pipeline FIFO Reset (Init);
- LFR – L1 Accept FIFO Reset (Init) is equivalent to FC_L1RES signal. It also resets the Ring Buffer Read and Ring Buffer Write Pointers.

CSR_AFD - Alignment FIFO Delay

FRONT FPGA

In the FRONT_FPGA this read/write register controls delaying of the AF read enable signal after an L1 Reset occurs. In fact, the total delay calculates as (96 + CSR_AFD Value) bunch crossings after an L1 Reset. The register is adjusted to minimize the overall MPC-to-SP data-path latency budget or during the SP link loop back tests.
Keeping in mind, MPC-to-SP fibers for ME1 chambers are shorter than for ME2, ME3, and ME4 ones, and that SP should deliver ME1 LCTs to the DT Track Finder with a minimal latency, the effective AFD is set different for ME2/ME3/ME4 and ME1 muons: for the latter the effective AFD is decreased by an OFF value.

**Table 7: CSR_AFD Data Format for FRONT_FPGA**

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>OFF3</th>
<th>OFF2</th>
<th>OFF1</th>
<th>OFF0</th>
<th>X</th>
<th>AFD6</th>
<th>AFD5</th>
<th>AFD4</th>
<th>AFD3</th>
<th>AFD2</th>
<th>AFD1</th>
<th>AFD0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ME1 Offset</td>
<td></td>
<td></td>
<td>ME Alignment FIFO Delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Here:
- X – don’t care bit for writes and zero for reads;
- AFD [6:0] = 0…127 – F3/F4/F5 (ME2/ME3/ME4) FRONT_FPGA Alignment FIFOs resume reads on (96+AFD) bunch crossing after an L1 Reset has been received. The register default value on power-up is 112, which gives the default delay of 208 bunch crossings.
- OFF [3:0] = 0…15 – ME1 Offset: F1/F2 (ME1) FRONT_FPGA Alignment FIFOs resume reads on (96+AFD-OFF) bunch crossings after an L1 Reset has been received, or OFF bunch crossings earlier than F3/F4/F5. The register default value on power-up is 0.

**SP FPGA**

In the SP_FPGA this read/write register controls the DT-to-SP data-path latency with MBAF settings for DT muons.

It also takes care of additional FRONT_FPGA-to-SP_FPGA data-path latency for ME1 muons to compensate for the difference in LCT delays introduced in the FRONT_FPGA.

**Note:** OFF [3:0] in the SP_FPGA (refer to Table 8) should always be set equal to OFF [3:0] in the FRONT_FPGA (refer to Table 7).

**Table 8: CSR_AFD Data Format for SP_FPGA**

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>OFF3</th>
<th>OFF2</th>
<th>OFF1</th>
<th>OFF0</th>
<th>X</th>
<th>MBAF3</th>
<th>MBAF2</th>
<th>MBAF1</th>
<th>MBAF0</th>
<th>X</th>
<th>MB AFIFO Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ME1 Offset</td>
<td></td>
<td></td>
<td>MB AFIFO Delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Here:
- X – don’t care bit for writes and zero for reads;
- OFF [3:0] = 0…15 – ME1 Offset: F1/F2 (ME1) muons get additionally delayed by “OFF” bunch crossings before getting to the SP core. The register default value on power-up is 0.
- MBAF [3:0] = 0…15 – additional delay for DT muons in bunch crossings. The register default value on power-up is 0.

**CSR_MF – Monitor FIFO Status**

This read-only register shows number of words currently sitting in the Monitor FIFO (MF), as well as Monitor FSM state. The MF should be loaded with LUT ID/CRC patterns before executing ACT_LUT command. Maximum available MF capacity is 128 16-bit words.
The MF can be reset either by a soft reset or executing a VM/MA/ACT_XFR/W/0x0100 VME cycle.

Table 9: CSR_MF Data Format for VME_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MFF</td>
<td>MFE</td>
<td>0</td>
<td></td>
<td>0</td>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>MFC</td>
<td>MFC</td>
<td>MFC</td>
<td>MFC</td>
<td>MFC</td>
</tr>
</tbody>
</table>

Here:
- MFC [6:0] = 0..127 – Monitor FIFO Word Count;
- MBSY – Monitor FSM is Busy (not Idle) => current LUT downloading sequence is not over yet;
- MFFF – Monitor FIFO Full Flag or 128 Word Count;
- MFEF – Monitor FIFO Empty Flag or 0 Word Count.

CSR_VF – Verification FIFO Status

This read-only register shows number of words currently sitting in the Verification FIFO (VF). The VF is loaded with LUT ID/CRC patterns upon executing ACT_LUT command. Maximum available VF capacity is 1024 16-bit words. The VF can be reset either with a soft reset or executing a VM/MA/ACT_XFR/W/0x0200 VME cycle.

The Verification FSM picks records of LUTs to be verified from the Monitor FIFO (MF). If the MF is loaded with a record that does not match either a predefined template or any actual SP LUT (the 1st word and all explicitly defined as “1” and “0” bits in other 3 words are checked) the Verification FSM skips this record.

Table 10: CSR_VF Data Format for VME_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>VFF</td>
<td>VFE</td>
<td>VEN</td>
<td>VBS</td>
<td>VF</td>
<td>0</td>
<td>VFC</td>
<td>VFC</td>
<td>VFC</td>
<td>VFC</td>
<td>VFC</td>
<td>VFC</td>
<td>VFC</td>
<td>VFC</td>
<td>VFC</td>
<td>VFC</td>
</tr>
</tbody>
</table>

Here:
- VFC [9:0] = 0..1023 – Verification FIFO Word Count;
- VBSY – Verification FSM is Busy (not Idle) => current verification process initiated by ACT_LUT is not over yet, any VME access to the SP IDTB (to SP_FPGA, DD_FPGA, F1_FPGA, F2_FPGA, F3_FPGA, F4_FPGA and/or F5_FPGA) will be denied;
- VEND – Verification done flag => current verification process is over;
- VFFF – Verification FIFO Full Flag or 1024 Word Count;
- VFEF – Verification FIFO Empty Flag or 0 Word Count;
- VFLD = 0 / 1 – Verification passed / failed (a cumulative flag for all non-skipped records).

DAT_MF – Monitor FIFO Data

The Monitor FIFO (MF) keeps LUT write records consisting of physical addresses, IDs and CRC patterns. Each LUT write record consists of 4 words, refer to Table 11 below. D [15:14] bits of each word identify the word number. The first word keeps physical LUT(s) address consisting of Chip Address, Muon Address and Register Address (LUT Type) that was used for LUT loading. The second word keeps a 12-bit LUT ID, which is supposed to be stored
in the highest LUT address. The third and forth words keep a 22-bit CRC code, which may be used for LUT verification.

The MF can be loaded either directly with proper data or auto loaded (preferred method) by monitoring the LUT download procedure. If the MF is loaded with a record that does not match any predefined template the Verification FSM skips this record.

For the auto-load procedure to work, it should start with a VM/MA/ACT_ACR write cycle followed by a “LUT_SIZE” number of write cycles, either single or in BLT mode.

The MF can be read back to VME to verify its contents. Reading is not destructive, since it utilizes a “read => write back” sequence.

The MF can be reset either by a soft reset or executing a VM/MA/ACT_XFR/W/0x0100 VME cycle.

**Table 11: DAT_MF Data Format for VME_FPGA**

<table>
<thead>
<tr>
<th>D15 D14 D13 D12</th>
<th>D11 D10 D9 D8</th>
<th>D7 D6 D5 D4</th>
<th>D3 D2 D1 D0</th>
<th>Word</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>CA</td>
<td>MA [1:0]</td>
<td>PT DT FLUT [1:0]</td>
<td>1st</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td></td>
<td></td>
<td>LUT ID = DATA [LAST ADDRESS]</td>
<td>2nd</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>PARL</td>
<td></td>
<td>CRC [10:0]</td>
<td>3rd</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>PARH</td>
<td></td>
<td>CRC [21:11]</td>
<td>4th</td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit;
- CA – Chip Address; Allowed values are either single chip, or and OR of Front FPGA chip addresses;
- MA [1:0] = {3,2,1,0} = {M3,M2,M1,MA} – Muon Address;
- LUT [3:0] = {8,4,3,2,1} = {PT, DT, FLUT};
- FLUT [1:0] = {3,2,1} = {GE, GP, LP};
- LUT ID = DATA from the Highest LUT Address;
- CRC [21:0] = Cyclic Redundancy Check code;
- PARL – CRC[10:0] Parity bit;

**DAT_VF – Verification FIFO Data**

The Verification FIFO (VF) keeps LUT read records consisting of physical addresses, IDs and CRC patterns. Each LUT read record consists of 4 words, refer to Table 12 below. D [15:14] bits of each word identify the word number. The first word keeps a physical LUT address consisting of Chip Address, Muon Address and Register Address (LUT Type) that was used for LUT verification. The second word keeps LUT ID, which has been read from the highest LUT address. The third and forth words keep a 22-bit CRC code, calculated during LUT verification process. The forth word also keeps a CRC error bit, which is set if the calculated during LUT verification CRC does not match the corresponding CRC from the Monitor FIFO.

The Verification FSM picks records of LUTs to be verified from the MF. If the MF is loaded with a record that does not match either a predefined template or any actual SP LUT (the 1st word and all explicitly defined as “1” and “0” bits in other 3 words are checked) the Verification FSM skips this record.
The VF can be reset either by a soft reset or executing a VM/MA/ACT_XFR/W/0x0200 VME cycle.

The DAT_VF is a read-only register, and its reading is destructive: the user can read out the Verification FIFO content only once.

Table 12: DAT_VF Data Format for VME_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Word</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>SP</td>
<td>F5</td>
<td>F4</td>
<td>F3</td>
<td>F2</td>
<td>F1</td>
<td>0</td>
<td>0</td>
<td>MA</td>
<td>[1:0]</td>
<td>PT</td>
<td>DT</td>
<td>FLUT</td>
<td>[1:0]</td>
<td>1st</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>ELID</td>
<td>LUT ID = DATA [LAST ADDRESS]</td>
<td>CA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2nd</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>PARL</td>
<td>CRC</td>
<td>[10:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3rd</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ECRC</td>
<td>PARH</td>
<td>CRC</td>
<td>[21:11]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>4th</td>
<td></td>
</tr>
</tbody>
</table>

Here:
- X – Don’t care bit;
- CA – Chip Address; Allowed values are only single chips;
- MA [1:0] = \{3,2,1\} = \{M3,M2,M1\} – Muon Address;
- LUT [3:0] = \{8,4,3,2,1\} = \{PT, DT, FLUT\};
- FLUT [1:0] = \{3,2,1\} = \{GE, GP, LP\};
- LUT ID = DATA from the Highest LUT Address;
- CRC [21:0] = Cyclic Redundancy Check code;
- PARL – CRC[10:0] Parity bit;
- ELID – LUT ID does not match the corresponding LUT ID value from MF;
- ECRC – LUT CRC does not match the corresponding CRC value from MF.

CSR_BID – Board Identifier Register

VME FPGA and SP FPGA

This read-only register in the VME_FPGA and SP_FPGA keeps \{SP02, SP04/SP05\} and \{SP02_MC, SP04_MC\} board versions and board IDs. For SP02 and SP02_MC boards the BRD_ID is always zero.

Table 13: CSR_BID Data Format for VME_FPGA and SP_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Word</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>BRD_VER [2:0]</td>
<td></td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>BRD_ID [5:0]</td>
</tr>
</tbody>
</table>

Here:
- BRD_VER [2:0] = \{2, 4\} Boards Version: SP02 or SP04/SP05
- BRD_ID [5:0] = 1…31 Board number.

FRONT FPGA

This read-only register in the FRONT_FPGA keeps a MPC Link Identifier. On power-up the register defaults to all zeros. After an MPC-to-SP optical link has been successfully initialized by the TTC_L1RES command, the register keeps the MPC/Link number. Note, that the Link Number is hardware coded, while the MPC number is a value downloaded in the MPC CSR0 register. During TLK2501 loop back tests bit[15] = 1, Mx [1:0] (x=1,2,3) is a muon number, and Fy [2:0] (y=1,2,3,4,5) is a FRONT_FPGA number.
Table 14: CSR_BID Data Format for FRONT_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

During SP Loop Back Tests

| 1   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | Fy  | 0   | 0   | Mx[1:0] |

Here for MPC-to-SP links:
- MPC_LINK_ID [7:0] - MPC Link Identifier consists of:
  - LINK # [1:0] = 0 (default), 1,2,3 – MPC Link number;
  - MPC # [5:0] = 0 (default)...63 – MPC Crate number.

DDU FPGA

In the DDU_FPGA this downloadable register keeps information on the SP configuration date, which is passed further to the TR1c / TR2a words of the Event Record Trailer (for Event Record Structure, version 5.2 and later).

The DD/CSR_BID should be loaded for the word HD2b to be initialized with the SP slot number and SP Trigger Sector (TS) Number (for Event Record Structure, version 5.2 and later). Non-initializes HD2b reports zero SP slot and TS numbers.

Table 15: CSR_BID Data Format for DDU_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
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</thead>
<tbody>
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</tbody>
</table>

Here:
- X – Don’t care bit, reads back as zero;
- YY [3:0] = 0,…,15 – Configuration Year = 2000 + BB*16 + YY;
- MM [3:0] = 0,…,12 – Configuration Month;
- DD [4:0] = 0…31 – Configuration Day;
- BB = 0 / 1 – Year Base = 0 / 16.

CSR_REQ – L1 Request Configuration

VME FPGA

This read/write register allows setting the delay for L1REQ, being sent by the SP to the backplane. The delay in implemented as a Synchronous FFO, so besides the delay setting, the register returns the actual delay as a REQ FIFO word count.

Table 16: CSR_REQ Data Format

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
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</tbody>
</table>

Here:
- X – don’t care bit for writes and zero for reads;
- LRD [6:0] = 0 (default)...127 – Additional delay for L1Request signal being sent to the Backplane;
- RFC [6:0] = 0 (default)...127 – Actual Request FIFO Word Count (actual additional delay set).
SP FPGA

This read/write register allows choosing the source of a L1 request signal to be sent by
the SP to the backplane. Normally, the L1 Request is an OR of tracks with non-zero Modes,
found by the SP core logic. The user can also chose the L1 Request to be generated on an OR of
Valid Pattern bit occurrences for enabled CSC muons and non-zero quality occurrences for
enabled DT muons.

Table 17: CSR_REQ Data Format

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CORE</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>MB1D</td>
<td>MB1A</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>ME4</td>
<td>ME3</td>
<td>ME2</td>
<td>ME1</td>
<td>ME1</td>
</tr>
</tbody>
</table>

L1 Request Enable

Here:
- X – don’t care bit for writes and zero for reads;
- ME1ABC = 0 (default) / 1 – Disable (default) / Enable VP-bits of ME1A, ME1B or
  ME1C muons (from F1) to be the source of L1 Request;
- ME1DEF = 0 (default) / 1 – Disable (default) / Enable VP-bits of ME1D, ME1E or
  ME1F muons (from F2) to be the source of L1 Request;
- ME2ABC = 0 (default) / 1 – Disable (default) / Enable VP-bits of ME2A, ME2B or
  ME2C muons (from F3) to be the source of L1 Request;
- ME3ABC = 0 (default) / 1 – Disable (default) / Enable VP-bits of ME3A, ME3B or
  ME3C muons (from F4) to be the source of L1 Request;
- ME4ABC = 0 (default) / 1 – Disable (default) / Enable VP-bits of ME4A, ME4B or
  ME4C muons (from F5) to be the source of L1 Request;
- MB1A = 0 (default) / 1 – Disable (default) / Enable non-zero quality of MB1A muons
to be the source of L1 Request;
- MB1D = 0 (default) / 1 – Disable (default) / Enable non-zero quality of MB1D muons
to be the source of L1 Request;
- CORE = 0 / 1 (default) – Disable / Enable (default) none-zero Mode output of the SP
core to be the source of L1 Request.