CSR_OSY – Out-of-Synch Control / Status

In the VME_FPGA the CSR_OSY register displays status of seven input and one output OSY lines. Besides, it carries eight mask bits, so each input or/and output can be either disabled (mask bit = 0) or enabled (mask bit = 1 => default):

\[
\text{OSY0} = (\text{OSY1} \cdot \text{OSM1} + \text{OSY2} \cdot \text{OSM2} + \text{OSY3} \cdot \text{OSM3} + \text{OSY4} \cdot \text{OSM4} + \text{OSY5} \cdot \text{OSM5} + \text{OSY6} \cdot \text{OSM6} + \text{OSY7} \cdot \text{OSM7}) \times \text{OSM0}
\]

Indexes 0…7 stand for chip numbers. By default all masks are set to enable state.

Table 1: CSR_OSY Data Format for VME_FPGA

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | Acc |
| OSM7| OSM6| OSM5| OSM4| OSM3| OSM2| OSM1| OSM0| X  | X  | X  | X  | X  | X  | X  | X  | X  | X  | WR |
| OSM7| OSM6| OSM5| OSM4| OSM3| OSM2| OSM1| OSM0| OSY7| OSY6| OSY5| OSY4| OSY3| OSY2| OSY1| OSY0| RD |

Here:
- X – Don’t care bit;
- OSM [7:0] – Out-of-Synch Chip mask for SP, DD, F5…F1 and VM chips;
- OSY [7:0] – Out-of-Synch status for SP, DD, F5…F1 and VM chips.

In the FRONT_FPGA, each MPC-to-SP link has a Bunch Crossing Counter (BXN) associated with it. On power-up and a FC_RSYNC command the BXN presets to a 0xDEC=3564 value. On every BC0 mark the BXN gets from the link after FC_RSYNC command it resets to 0 and then starts counting up to 3563. Normally, next BC0 should arrive exactly when the BXN is at 3563 and reset it back to 0. If BC0 comes later (longer orbit) or does not come at all, the BXN reaches its max value of 0xDEC=3564 and stays at it, until next BC0 is received. If BC0 comes earlier (shorter orbit) then the BXN resets to 0 earlier.

In between FC_RSYNC commands the following out-of-sync conditions are detected and reported:
- If link BX0 does not match BXN [0] for BX with VP=1, then the BXOC (Bunch-Xing Out-of-sync Counter) increments by 1;
- If link BC0 comes earlier or later, then the BCOC (Bunch Crossing zero Out-of-sync Counter) increments by 1;
- If link Alignment FIFO gets empty, then the AFOC (Alignment FIFO Out-of-sync Counter) increments by 1 for each BX read from the empty Alignment FIFO;

Any counter stops incrementing, when it reaches its maximum value of 15;

All counters are reset on power-up, with SOFT_RESET, FC_RSYNC and, individually, with ACT_LCR command.

Same register carries reporting threshold and enable bits for each out-of-sync condition. There is a separate CSR_OSY register for each link, 15 registers in 5 FRONT_FPGAs in total.

Table 2: CSR_OSY Data Format for FRONT_FPGA

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | Acc |
| X | X | X | X | X | X | X | X | X | X | X | X | MXRT| AFOS| BCOS| BXOS| WR |
| AFOC3| AFOC2| AFOC1| AFOC0| BCOC3| BCOC2| BCOC1| BCOC0| BXOC3| BXOC2| BXOC1| BXOC0| MXRT| AFOS| BCOS| BXOS| RD |
| AFIFO Out-of-sync Counter | BC0 Out-of-sync Counter | BX Out-of-sync Counter | Out-of-Sync reporting to FMM |

Here:
- X – Don’t care bit;
− AFOC [3:0] – Alignment FIFO Out-of-sync Counter;
− BCOC [3:0] – Bunch-Crossing zero Out-of-sync Counter;
− BXOC [3:0] – Bunch-Xing Out-of-sync Counter;
− MXRT = 0 (default) / 1 – set Minimum (1, default) / Maximum (15) number of out-of-sync occurrences as a Reporting Threshold;
− AFOS = 0 (default) / 1 – disable (default) / enable Alignment FIFO Out-of-Sync status reporting to FMM;
− BCOS = 0 (default) / 1 – disable (default) / enable Bunch-Crossing zero Out-of-Sync status reporting to FMM;
− BXOS = 0 (default) / 1 – disable (default) / enable Bunch-Xing Out-of-Sync status reporting to FMM;

In the DDU_FPGA the CSR_OSY register carries Out-of-Synch status for the SP_FPGA and FRONT_FPGAs. During readout process of each event the DDU_FPGA queries other FPGAs for their bunch counter and event counter values, compares them against templates and sets out-of-synch flags, if the comparison fails. The SP_FPGA provides a template for the bunch counter comparison, and the DDU_FPGA provides a template for the event counter comparison.

Table 3: CSR_OSY Data Format for DDU_FPGA

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>TRN</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSE7</td>
<td>0</td>
<td>OSE5</td>
<td>OSE4</td>
<td>OSE3</td>
<td>OSE2</td>
<td>OSE1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>OSB5</td>
<td>OSB4</td>
<td>OSB3</td>
<td>OSB2</td>
<td>OSB1</td>
<td>0</td>
<td>RD</td>
</tr>
</tbody>
</table>

Here:
− OSE [7:1] – SP_FPGA and FRONT_FPGA Event Counter Out-of-Synch bits;

**ACT_LCR – Link Counter Reset**

**FRONT FPGA**

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 25 ns reset pulse to selected counter(s) described under the CSR_LNK, CSR_LEC, DAT_VPC, and CSR_OSY headings.

Table 4: ACT_LCR Data Format for FRONT_FPGA

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | TRN |
|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|-----|
| X   | AFOCR | BCOCR | BXOCR | X   | X   | X   | X   | X   | X   | X   | VPR | TER | SLR | CER | EWR | WR  |

Here:
− X – Don’t care bit;
− AFOCR – Alignment FIFO Out-of-sync Counter Reset;
− BCOCR – Bunch-Crossing zero Out-of-sync Counter Reset;
− BXOCR – Bunch-Xing Out-of-sync Counter Reset;
− EWR – TLK2501 Error Word Counter Reset in the CSR_LEC register (RXdV == HIGH, RXER == HIGH);
− CER – TLK2501 Carrier Extend Counter Reset in the CSR_LEC register (RXdV == LOW, RXER == HIGH);
− SLR – FINISAR optical receiver Signal Loss Counter Reset in the CSR_LEC register (RXSD goes LOW);
− TER – PRBS Test Error Counter Reset in the CSR_LNK register;
− VPR – Valid Pattern Counter Reset in the DAT_VPC register.

**SP FPGA**

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 25 ns reset pulse to selected counter(s) described under DAT_VPC heading.

<table>
<thead>
<tr>
<th>D15</th>
<th>D14</th>
<th>D13</th>
<th>D12</th>
<th>D11</th>
<th>D10</th>
<th>D9</th>
<th>D8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>TRN</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>OCR</td>
<td>TCR</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VPR</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>WR</td>
</tr>
</tbody>
</table>

Here:
− X – Don’t care bit;
− VPR – Valid Pattern Counter Reset in the DAT_VPC register;
− TCR – Track Counter\(^1\) Reset (readable via DAQ only);
− OCR – Orbit Counter\(^1\) Reset (readable via DAQ only).

\(^1\) Regarding Track Counter and Orbit Counter functionality details refer to: [http://www.phys.ufl.edu/~uvarov/SP05/LU-SP2DDU_Event_Record_Structure_v52A.pdf](http://www.phys.ufl.edu/~uvarov/SP05/LU-SP2DDU_Event_Record_Structure_v52A.pdf)