SP02 Backplane Interfaces

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This doc matches with the vm_fa_dd_021210.evf and sp_031210.evf configuration files.
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CCB Interface

The CCB interface provides the SP02 with timing and trigger control signals distributed by the Clock and Control Board (CCB) over the backplane [i]. The backplane counts as many as 34 signal lines coming in and going out of the SP02. Table 1 groups backplane signals into four Groups. All GTLP lines are active LOW (negative bus logic).

The Clock Group includes a differential clock and clock_enable lines. For the TF prototype the enable line is expected to be always in a LOW state.

Table 1: SP02 CCB Interface Signals.

Signal	Lines	Direction	Type	Logic	Duration
Clock Group					
CCB_CLK	2	IN	Point-to-point	LVDS	40MHz
CCB_CLK_EN	1	IN	Bussed	GTLP	Pulse, n counts
Subtotal	**3**				
Fast Control Group					
CCB_CMD [5..0]	6	IN	Bussed	GTLP	Level
CCB_ECRES	1	IN	Bussed	GTLP	25ns
CCB_BCRES	1	IN	Bussed	GTLP	25ns
CCB_CMD_STR	1	IN	Bussed	GTLP	25ns
CCB_BX0	1	IN	Bussed	GTLP	25ns+ECL FP
CCB_L1ACC	1	IN	Bussed	GTLP	25ns+ECL FP
CCB_DAT [7..0]	8	IN	Bussed	GTLP	Level
CCB_DAT_STR	1	IN	Bussed	GTLP	25ns
CCB_RDY	1	IN	Bussed	GTLP	Static level
Subtotal	**21**				
Reload Group					
CCB_SP_HRES	1	IN	Bussed	GTLP	400ns
SP_CFG_DONE	1	OUT	Point-to-Point	GTLP	Level
Subtotal	**2**				
Reserved Group					
CCB_RSVD [3..0][#]	4	IN	Bussed	GTLP	25ns

[#] CCB_RSVD3 is assigned for CCB_L1RES – L1 Reset signal resets L1 buffers and resynchronizes optical links.

Signal	Lines	Direction	Type	Logic	Duration
SP_RSVD [3..0][*]	4	OUT	Bussed	GTLP	25ns
Subtotal	**8**				
Total	**34**				

The Fast Control Group includes a ccb_ready status line, TTCrx command and data busses accompanied with strobes, and a few TTCrx signals, decoded by CCB. The Fast Control Group signals are valid when and only when the ccb_ready is LOW.

The Reload Group includes a hard_reset signal for reconfiguration of the SP02 FPGAs. In turn, the SP02 returns a configuration_done status to the CCB.

The Reserved Group is partially specified at the moment, see footnotes to Table 1.

The VME_FPGA delivers fast control signals to each SP02 FPGA via a 5-bit Fast Control (FC) bus. Table 2 sets correspondence between the FC and the CCB signals.

Table 2: SP02 Internal Control Bus and configuration control/status lines

FC/CCB Command Description	CCB Backplane Signal or Command Code	FC/CCB Command Acronym	Fast Control Bus Command Code
No commands / Idle state		FC_NOCMD	fc_cmd[4:0]=5'b0_0000
L1 Accept	ccb_l1acc	FC_L1ACC CCB_L1ACC	fc_cmd[4:0]=5'h1_XXXX
Store Next Event into Spy FIFO, as determined by the CSR_SFC	Generated by VME_FPGA	FC_SFRUN	fc_cmd[4:0]=5'hX_1XXX
Bunch Counter Reset	ccb_bcres	FC_BCRES CCB_BCRES	fc_cmd[4:0]=5'hX_X001
Event Counter Reset	ccb_ecres	FC_ECRES CCB_ECRES	fc_cmd[4:0]=5'hX_X010
Bunch & Event Counter Reset	ccb_bcres & ccb_ecres	FC_BERES CCB_BCRES CCB_ECRES	fc_cmd[4:0]=5'hX_X011
Bunch Crossing Zero Mark	ccb_cmd[5:0]=0x01	FC_BC0 CCB_BC0	fc_cmd[4:0]=5'hX_X100
L1 Reset – Resets L1 Buffers and Resynchronizes Optical Links	ccb_cmd[5:0]=0x03	FC_L1RES CCB_L1RES	fc_cmd[4:0]=5'hX_X101
Start Data Taking	ccb_cmd[5:0]=0x06	FC_L1RUN CCB_L1STT	fc_cmd[4:0]=5'hX_X110
Stop Data Taking	ccb_cmd[5:0]=0x07	CCB_L1STP	Handled by VME_FPGA
Inject Test Pattern into SP. See details in CSR_TFC description	ccb_cmd[5:0]=0x2F	FC_TFRUN CCB_TPSP	fc_cmd[4:0]=5'hX_X111
Inject Test Pattern into MPC	ccb_cmd[5:0]=0x30	CCB_TPMPC	Handled by VME_FPGA
Inject Test Pattern into TMB	ccb_cmd[5:0]=0x24	CCB_TPTMB	Handled by VME_FPGA
Bunch Counter Reset	ccb_cmd[5:0]=0x32	FC_BCRES CCB_BXRES	fc_cmd[4:0]=5'hX_X001
Hard Reset – reconfigures SP02 FPGAs (as determined by a Configuration Mask Register)	ccb_sp_hard_res		cfg_prog_n[7:1]
Configuration Done – reports on successful completion of FPGA configuration (as determined by a	sp_cfg_done		cfg_done[7:1]

[*] SP_RSVD3 is assigned for SP_L1REQ – L1 request, local trigger generated by the SP_FPGA logic.

Done Mask Register)			

The FC bus has two dedicated lines, one for L1 Accepts and another to initiate storing data into Spy FIFOs. Three more lines encode all other fast control commands. Signals on dedicated lines may coincide in time with encoded commands, while encoded commands are mutually exclusive.

Note, that data taking is stopped on power-up, so backplane CCB_L1ACC signals don't pass to the FC_L1ACC line. A sequence of CCB_L1STT and CCB_BC0 commands should be issued to let L1 Accepts pass to the internal FC bus, see Figure 1 for details on the L1Accept State Machine (L1A_FSM). A CCB_L1STP command returns the L1A_FSM into the default L1A_STOP state from the L1A_RUN state. Besides, CCB_L1RES or CCB_BXRES commands return the L1A_FSM into the L1A_STOP state unconditionally. FRONT_FPGA passes link data to the SP02 LUTs and, hence, to the SP_FPGA only when the L1Accept FSM is in the L1A_RUN state, otherwise it selects LUT's zero address.

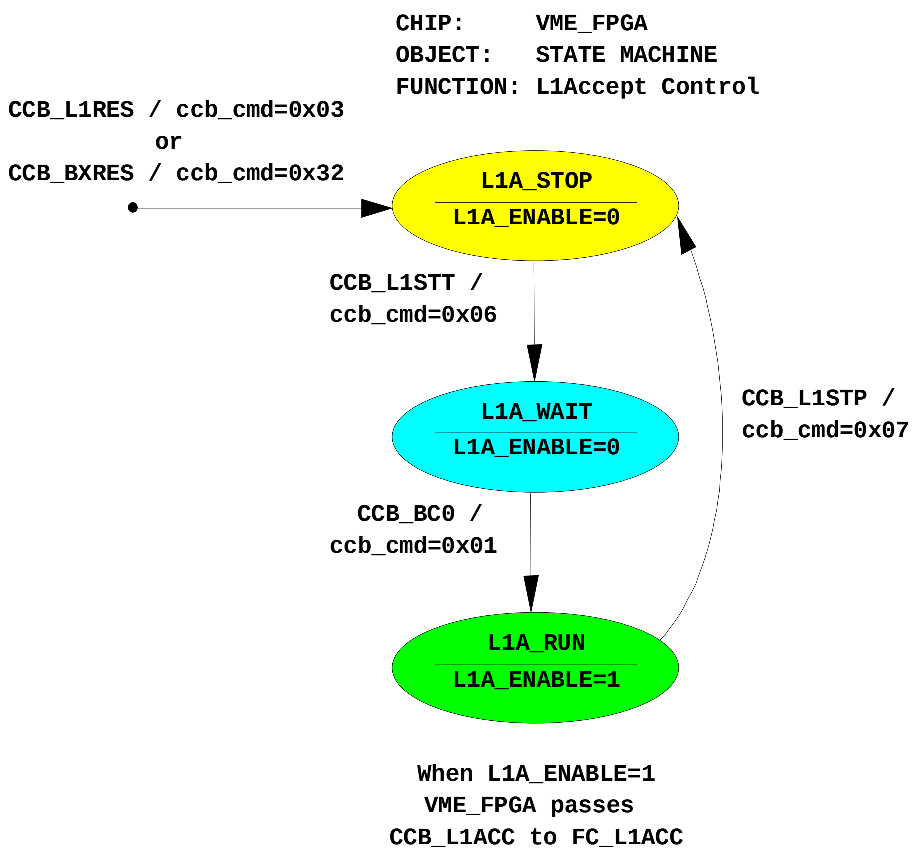

Figure 1 State Machine for L1Accept Control

An FC_SFRUN internal command requests storing next event into the Spy FIFO. See the CSR_SFC – Spy FIFO Configuration section for details.

Bunch counter on power-up and/or after CCB_BCRES, CCB_BXRES, or CCB_L1RES commands is preloaded with a 0xFFF=4095 value. It starts counting from 1 and up upon receiving a CCB_BC0 command. Bunch counter rolls over to zero count, when it reaches its maximum value, which is 923 for the beamtest at SPS and 3563 for LHC operations.

Summary of fast control commands:

- CCB_BCRES – resets Bunch counters to 0xFFF = 4095;
- CCB_ECRES – resets Event counters;
- CCB_L1RES – resets Bunch counters to 0xFFF = 4095, resynchronizes optical links, resets readout buffers, resets Event counters, and returns the L1Accept FSM into the L1A_STOP state.
- CCB_BXRES – resets Bunch counters to 0xFFF = 4095, and returns the L1Accept FSM into the L1A_STOP state.
- CCB_L1STT – counting of CCB_L1ACCs to be resumed on the next CCB_BC0 command.
- CCB_L1STP –returns the L1Accept FSM into the L1A_STOP state.
- CCB_BC0 – if preceded with the CCB_L1STT command, starts the Bunch counter from its offset value, as determined by the CSR_BCO register; otherwise serves as a timing mark to verify the Bunch counter synchronization to the control timing.

The current state of the SP02 logic can be monitored with four fast monitoring status signals: busy (FM_BSY), ready (FM_RDY), warning-of-overflow (FM_WOF), and out-of-synch (FM_OSY). Each SP02 FPGA reports its 4-bit status to the VME_FPGA. The VME_FPGA is capable of masking individual statuses when providing the SP02 overall status to the RJ45 connector and front panel indicators (LEDs).

For the summary of fast monitoring statuses see details into CSR_BSY – Busy Control/Status, CSR_RDY – Ready Control/Status, CSR_WOF – Warning-of-OverFlow Control/Status, and CSR_OSY – Out-of-Synch Control / Status sections below.

Table 3 SP02 LED panel

Description	Left LED Name	Left LED Color	Right LED Color	Right LED Name	Description
Busy	BSY	Red	Green	5.0V_OK	5.0V power is OK
Ready	RDY	Green	Green	3.3V_OK	3.3V power is OK
Warning-of-OverFlow	WOF	Red	Green	2.5V_OK	2.5V power is OK
Out-of-Synch	OSY	Red	Green	1.5V_OK	1.5V power is OK
Local Charged Trigger	LCT	Yellow	Yellow	L1ACC	L1 Accept

The LED indicators are located above the F5 link transceivers. The BSY, RDY, WOF, and OSY indicators display status of the corresponding signal lines. Power OK indicators are off, since the power-monitoring chip MAX6338BUB is missing on the board. The L1ACC LED blinks for 25 ms on each CCB_L1ACC. The LCT currently indicates RDY0_INT status of the VME_FPGA.

VME Interface

The SP02 card includes two A24D16 Slave interfaces [ii] implemented in VME_FPGA and CPLD_FPGA accordingly. Table 4 shows all address modifiers, the SP02 responds to during the VME Data Transfer Bus (DTB) cycles.

Table 4: SP02 Address Modifier Codes.

AM	Description		Interface Chip
39	A24 non privileged data access	Access tpo all locations, except the BLT Mapping Registers	VME_FPGA
3A	A24 non privileged program access	Access to BLT Mapping Registers	
3B	A24 non privileged block transfer (BLT)	BLT access using the BLT Mapping Registers	
3D	A24 supervisory data access		VME_CPLD
3E	A24 supervisory program access		
3F	A24 supervisory block transfer (BLT)		

Auxiliary VME Interface

The auxiliary VME_CPLD interface is intended for board configuration and provides access solely for the Bus Scan Controller (BSC). The BSC drives three chains of JTAG-compatible devices, see Table 5:

- Chain 0 consists of the MAIN_FPGA and its EEPROMs;
- Chain 1 includes the VME_FPGA with EEPROM, the FRONT_FPGAs with EEPROMs, and the DDU_FPGA with EEPROM;
- Chain 2 connects 45 SRAMs.

Table 5: SP02 Configuration Chains.

Chain No	Device No	Device Name	Device Type	Device ID Code	Bypass Switch
0	1	SP_EEPROM_1	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW2
0	2	SP_EEPROM_2	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW3
0	3	SP_EEPROM_3	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW4
0	4	SP_EEPROM_4	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW5
0	5	SP_EEPROM_5	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW6
0	6	SP_FPGA	XC2V4000-5FF1152C	VVVV 0001 0000 0101 0000 0000 1001 0011	MC_SW1
1	1	VME_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW4
1	2	VME_FPGA	XC2V1000-5FG456C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW5
1	3	FF5_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW2
1	4	FRONT_FPGA_5	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW3
1	5	FF4_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW14
1	6	FRONT_FPGA_4	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW15
1	7	FF3_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW19
1	8	FRONT_FPGA_3	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW20
1	9	DDU_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW10
1	10	DDU_FPGA	XC2V1000-5FG456C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW11
1	11	FF2_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW12
1	12	FRONT_FPGA_2	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW13
1	13	FF1_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW17
1	14	FRONT_FPGA_1	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW18

Chain No	**Device No**	**Device Name**	**Device Type**	**Device ID Code**	**Bypass Switch**
2	1	ME4C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	2	ME4C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	3	ME4C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	4	ME4B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	5	ME4B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW7
2	6	ME4B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	7	ME4A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	8	ME4A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	9	ME4A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	10	ME3C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	11	ME3C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	12	ME3C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	13	ME3B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	14	ME3B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW9
2	15	ME3B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	16	ME3A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	17	ME3A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	18	ME3A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	19	ME2C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	20	ME2C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	21	ME2C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	22	ME2B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	23	ME2B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW8
2	24	ME2B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	25	ME2A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	26	ME2A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	27	ME2A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	28	ME1F_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	29	ME1F_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	30	ME1F_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	31	ME1E_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	32	ME1E_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW6
2	33	ME1E_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	34	ME1D_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	35	ME1D_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	36	ME1D_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	37	ME1C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	38	ME1C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	39	ME1C_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	40	ME1B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	41	ME1B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW16
2	42	ME1B_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	43	ME1A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	44	ME1A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	45	ME1A_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	

Alex M. is to determine the VME address mapping for the auxiliary VME interface.

Main VME Interface

A24 Non Privileged Data Access

An A24 non privileged data access (AM=0x39) to the main VME_FPGA interface utilizes a 5-bit geographical addressing scheme [ii] and provides for the VME Data Transfer Bus (DTB) multicast ***write*** cycles by partitioning the address space into the following fields, see Table 6.

Table 6 Address Space for Non Privileged Data Access

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA					CA							X	MA		RA							X	0

Here:

- X – Don't care address line;
- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- CA – Chip Address. Positional coding provides simultaneous write access to any combination of SP02 FPGAs (except VME_FPGA), see Table 7;
- MA – Muon Address. Each FRONT_FPGA processes data for 3 muons, and the SP_FPGA services 3 PT LUTs. A 2-bit MA field provides write access either to a single muon-related register or to all three such registers simultaneously, see Table 8 for details.
- RA – Register Address inside FPGA(s). There are 4 groups of registers in total, see Table 9 for details:
    - Action Register Group. Writing to these write-only registers causes pulses, like reset or test pulse, to be generated and/or operations, like start or stop L1ACC processing, to be performed.
    - Control/Status Register Group. These registers carry 2 groups of bits: read-only status bits to monitor, and read/write bits to control behavior of the SP02 logic.
    - Address Register Group. These registers provide access to LUT and Eta Window address counters.
    - Data Register Group. The group provides access to LUT , Eta Window and FIFO data inputs/outputs.

Full Address (FA) of the register is defined as:

FA = (SA << 19) + (CA << 12) + (MA << 9) + (RA << 2).

Table 7 Chip Address Field for Non Privileged Data Access

Chip	CA, binary	Description
VM	000_0000	VME_FPGA Access
F1	000_0001	FRONT_FPGA_1 Access
F2	000_0010	FRONT_FPGA_2 Access
F3	000_0100	FRONT_FPGA_3 Access
F4	000_1000	FRONT_FPGA_4 Access
F5	001_0000	FRONT_FPGA_5 Access
DD	010_0000	DDU_FPGA Access
SP	100_0000	SP_FPGA Access

Table 8 Muon Address Field for Non Privileged Data Access

Label	Muon in FPGA	MA, binary	Description
MA	ALL	00	Access to all three muon-related registers
M1	A/D/1	01	Access to a First (A or D or 1) muon-related register
M2	B/F/2	10	Access to a Second (B or E or 2) muon-related register
M3	C/E/3	11	Access to a Third (C or F or 3) muon-related register

Note, that only ***write*** access is defined to a group of registers, while ***read*** access may only be executed to a single register at any time.

Table 9 Storage Address Field, Non Privileged Data Access

RA, hex	Register Label	Description	Destination / Valid MA			
			SP	DD	Fx	VM
Action Register Group						
0x00	ACT_HR	Hard Resets	-	-	-	MA
0x01	ACT_CMR	Clock Managers Resets	MA	MA	MA	MA
0x02	ACT_LCR	Link Counters Resets	-	MA	MA/M1/M2/M3	-
0x03	ACT_XFR	FIFOs Resets	MA	MA	MA	-
0x04	ACT_ACR	Address Counters Resets	MA	-	MA	-
0x05						
0x06						
0x07						
0x08	ACT_TST	Run Tests		-	-	-
Control/Status Register Group						
0x10	STS_CCB	Fast Control Status		MA	MA	?MA
0x11	STS_ANA	CCB Logic Analyzer				MA
0x12	STS_VPC	Valid Pattern bit Counter			M1/M2/M3	
0x20	CSR_CID	Chip ID	TBD	MA	MA	MA
0x21	CSR_CLK	System CLK Control/Status		MA	MA	-
0x22	CSR_CM1	Clock Manager_1 Control/Status	TBD	MA	MA	MA
0x23	CSR_CM2	Clock Manager_2 Control/Status	TBD	MA	MA	MA
0x24	CSR_HR	Hard Reset Mask		-	-	MA
0x25	CSR_CFG	Configuration Done Status		-	-	MA
0x26	CSR_INI	Init Status		-	-	MA
0x27	CSR_CHP	Chip Presence Mask		-	-	MA
0x28	CSR_BSY	Busy Mask/Status		-	-	MA
0x29	CSR_RDY	Ready Mask/Status		-	-	MA
0x2A	CSR_WOF	WarningOfOverflow Mask/Status			-	MA
0x2B	CSR_OSY	OutOfSynch Mask/Status			MA/M1/M2/M3	MA
0x2C	CSR_LCT	LCT Control/Status	TBD	-	TBD	MA
0x2D	*CSR_CCD*	*CCB Command Delay - obsolete*	-	-	-	-

RA, hex	Register Label	Description	Destination / Valid MA			
			SP	DD	Fx	VM
0x2D	CSR_BCO	Bunch Counter Offset		MA	MA	-
0x2E	CSR_L1D	L1 Accept Delay		-	-	MA
0x30	CSR_LEC	Link Error Counters		MA	M1/M2/M3	-
0x31	CSR_AF	Alignment FIFO Status	TBD	-	M1/M2/M3	-
0x32	CSR_TF	Test FIFO Status	TBD	MA	M1/M2/M3	-
0x33	CSR_SF	Spy FIFO Status	TBD	MA	M1/M2/M3	-
0x34	CSR_PF	Pipeline FIFO Status	TBD	-	MA	-
0x35	CSR_DF	DAQ FIFO Status	TBD	MA	MA	-
0x36	CSR_BF	Barrel FIFO Status				
0x37	CSR_LF	L1 FIFO Status		MA	MA	-
0x38	CSR_RBW	Ring Buffer Writer Pointer		-	MA	-
0x39	CSR_RBR	Ring Buffer Read Pointer		-	MA	-
0x40	CSR_LNK	Link Control/Status		MA	MA/M1/M2/M3	-
0x41	CSR_AFD	Alignment FIFO Read Delay		-	MA	-
0x42	CSR_TFC	Test FIFO Configuration	TBD	MA	MA	-
0x43	CSR_SFC	Spy FIFO Configuration	TBD	MA	MA	MA
0x44	CSR_PFD	Pipeline FIFO Read Delay	TBD	-	MA	-
0x45	CSR_DFC	DAQ FIFO Configuration		MA	MA	-
Address Counter Group						
0x50	CNT_LPL	Local Phi LUT Address Low	-	-	MA	-
0x51	CNT_LPH	Local Phi LUT Address High	-	-	MA	-
0x52	CNT_GLL	Global_Eta/Phi/DT LUT Address Low	-	-	MA	-
0x53	CNT_GLH	Global_Eta/Phi/DT LUT Address High	-	-	MA	-
0x56	CNT_PTL	PT LUT Address Low	MA	-	-	-
0x57	CNT_PTH	PT LUT Address High	MA	-	-	-
0x58	CNT_EW	Eta Window Address	MA	-	-	-
Data Register Group						
0x60	DAT_LP	Local Phi LUT Data	-	-	MA/M1/M2/M3	-
0x62	DAT_GP	Global Phi LUT Data	(Data MA/M1/M2/M3)[1]	-	Address MA/M1/M2/M3	-
0x63	DAT_DT	DT LUT Data	-	-	MA/M1/M2/M3	-
0x64	DAT_GE	Global Eta LUT Data	(Data MA/M1/M2/M3)[2]	-	Address MA/M1/M2/M3	-
0x66	DAT_PT	PT LUT Data	MA/M1/M2/M3	-	-	-
0x68	DAT_EW	Eta Window Data	TBD	-	-	-
0x72	DAT_TF	Test FIFO Data	TBD	MA	MA/M1/M2/M3	-
0x73	DAT_SF	Spy FIFO Data	TBD	MA	M1/M2/M3	-
0x75	DAT_DF	DAQ FIFO Data	TBD		MA	-
0x76	DAT_BF	Barrel FIFO Data				
0x7F	DAT_RW	Read / Write Data	MA	MA	MA	MA

The main VME_FPGA interface distributes VME control all over the board via the Internal Data Transfer Bus (IDTB). IDTB is a synchronous parallel bus that is used by the

[1] User addresses only FRONT_FPGA, data is routed to the SP_FPGA automatically
[2] User addresses only FRONT_FPGA, data is routed to the SP_FPGA automatically

VME_FPGA to transfer data to or from other SP02 FPGA(s): SP_FPGA, 5 FRONT_FPGAs, and DDU_FPGA.

The IDTB bus lines are grouped into 4 categories:

– Address Lines:	A[11:2]	see Table 10
– Data Lines:	D[15:0]	Bi-directional
– Control Lines:	/CS[7:1]	Chip Select, active LOW
	/ACK[7:1]	Acknowledge, active LOW
	/WR	Write, active LOW
– Auxiliary Lines:	VMB_WR	Buffer Write
	VMB_/OE	Buffer Output Enable, active LOW

Table 10 IDTB Address Lines

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2
RV	MA		RA						
RV	IA								

- IA – Internal DTB Address, defines storage location inside FPGA
- RV – Reserved line

To prevent data lines from being too long they are split into two segments: the SP segment and the FRONT/DDU segment, with bi-directional buffers in between. The SP segment connects directly to the VME_FPGA pins. The FRONT/DDU segment is located behind the buffers. Two auxiliary lines: Buffer Write (data direction) and Buffer Output Enable, - are used to control data flow through the buffers.

The IDTB transfer is a sequence of level states on the signal lines that results in the transfer of an address and two bytes of data between the VME_FPGA and other SP02 FPGA(s).

Each IDTB cycle is an inherent part of the backplane DTB cycle, when DTB addresses FPGA(s), other than VME_FPGA. Chip Select (/CS) plays role of the DS* strobe and Acknowledge (/ACK) plays role of the DTACK*. The major difference between backplane DTB and IDTB is that IDTB is a synchronous bus, i.e. both /CS and /ACK handshake signals should be asserted on the rising edge of the system clock at source, and sensed with the next rising edge of the system clock at destination.

The VME_FPGA initiates two types of IDTB cycles:

- **IDTB Write cycle** transfers data from the VME_FPGA to one or more destination FPGA(s). The cycle begins when the VME_FPGA sets address, data, Write and optionally Buffer Write and Buffer Output Enable on the corresponding lines and issues one or more Chip Selects. Selected FPGA(s) captures the address and checks to see if it is to respond to the cycle. If so, sensing Write in a LOW state, it stores the data and acknowledges the transfer. The VME_FPGA then terminates the cycle.
- **IDTB Read cycle** transfers data from the source FPGA to the VME_FPGA. The cycle begins when the VME_FPGA sets address and optionally a Buffer Output Enable and issues a Chip Select. Selected FPGA captures and the address and checks to see if it is to respond to the cycle. If so, sensing Write in a HIGH state, it retrieves the data from the corresponding storage, places it on the data lines and acknowledges the transfer. The VME_FPGA then terminates the cycle.

Normally the VME_FPGA would terminate the DTB transfer with the Data Transfer Acknowledge (DTACK*) asserted low. If during the DTB cycle the addressable SP02 detects that the VME Master either addresses a non-existed location, or tries to write to a read-only location, the VME_FPGA terminates the cycle with a Bus Error (BERR*) asserted low. The VME_FPGA is not aware of the DTB outcome, when it passed the DTB cycle to the IDTB. If the expected IDTB Acknowledge(s) is (are) not received after a time-out period has expired, the VME_FPGA terminates the cycle driving BERR* low. The VME_FPGA time-out period is set to 8 system clocks.

A24 Non Privileged Program Access

An A24 non privileged program access (AM=0x3A) is used to load four mapping locations in the VME FPGA, see Table 11 for valid address fields

Table 11 Address Space for Non Privileged Program Access

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA					X													PA				X	0

Here:

- X – Don't care address line(s);
- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- PA – Program Address, defines 16 register locations in the non privileged program space, see Table 12 for valid addresses.

Table 12 Storage Address for Non Privileged Program Access

PA, hex	Register Label	Description
BLT Mapping Control/Status Register Group		
0x0		
0x1	CPA_BF1	BLT Mapping FIFO_1 Control/Status
0x2	CPA_BF2	BLT Mapping FIFO_2 Control/Status
0x3	CPA_BF3	BLT Mapping FIFO_3 Control/Status
0x4		Reserved
0x5		Reserved
0x6		Reserved
0x7		Reserved
BLT Mapping Data Register Group		
0x8	DPA_BLT	BLT Mapping Data
0x9	DPA_BF1	BLT Mapping FIFO_1 Data
0xA	DPA_BF2	BLT Mapping FIFO_2 Data
0xB	DPA_BF3	BLT Mapping FIFO_3 Data
0xC		Reserved
0xD		Reserved
0xE		Reserved
0xF		Reserved

Details on the above registers can be found in the Register Detail section under the register labels. During BLT transfers, mapping registers substitute the DTB address with a 16-bit address, used to access storage location(s) in the non privileged data space. The format of the mapping data/address is shown below:

Table 13 BLT Mapping Location Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CA							MA		RA						

Here CA, MA, and RA are address fields, described in the A24 Non Privileged Data Access section above.

A24 Non Privileged Block Transfer (BLT)

Any storage location, accessible via the A24 Non Privileged Data Access, can also be accessed via an A24 non privileged block transfer (BLT), when AM=0x3B. The BLT, prior to executing, should be initialized by loading a mapping location with one or more destination addresses. The BLT mapping locations are listed in Table 12. During the BLT DTB cycle the VME_FPGA, depending on the value in the BA field, uses one of the preloaded mapping locations to substitute the current DTB address with the address stored in the mapping location, see Table 14. Table 13 shows the BLT mapping location data format and Table 15 lists 4 128Kbyte windows for block transfers.

Table 14 BLT Mapping Location Data Format for Non Privileged Block Transfers

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA					BA		X																0

Here:

- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- BA – BLT Address. Defines one out of four BLT Mapping locations inside the VME_FPGA to substitute the current VMA backplane address with the preloaded one.
- X – Don’t care address lines;

Table 15 BLT Address Field for Non Privileged Block Transfers

BA, binary	Register Name	First D16 Transfer Address, hex	Last D16 Transfer Address, hex	Address Space
00	BLT Mapping Register	0x00000	0x1FFFE	64 Kwords = 128 Kbytes
01	BLT Mapping FIFO_1	0x20000	0x3FFFE	64 Kwords = 128 Kbytes
10	BLT Mapping FIFO_2	0x40000	0x5FFFE	64 Kwords = 128 Kbytes
11	BLT Mapping FIFO_3	0x60000	0x7FFFE	64 Kwords = 128 Kbytes

Register Detail

Action Register Group

ACT_HR – FPGA Hard Reset Register

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 400 ns Hard Reset pulse to the selected FPGA(s) onboard. Hard Reset is applied to the /PROG_B pin of the corresponding FPGA. A VME-generated Hard Reset is ORed with a CCB backplane hard reset. This register address is applicable to the VME_FPGA only.

Sensing a hard reset on its input, the FPGA reloads its configuration from the associated configuration EPROM. The user may use the ACT_HR transfer cycle to verify chip presence on the board. To make sure all FPGA chips are present on the board, the CSR_CFG read transfer cycle should be executed twice after the ACT_HR: first time when chips are engaged in the configuration process and second time after a 5 sec pause, when the configuration is definitely completed. If there is a missing FPGA chip on the board (a mezzanine card is not installed, for example) then the corresponding Configuration Done line remains floating, and can be sensed by the VME_FPGA as being either in HIGH (Logic ONE) or LOW (Logic ZERO) state. But in any case, Configuration Done line for a missing chip would retain its state, while the one for a successfully configured FPGA will be LOW on the first read and HIGH on the second read. See Table 52 for chip mapping.

Table 16

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	SPHR	DDHR	F5HR	F4HR	F3HR	F2HR	F1HR	X

Here:
- X – Don't care bit
- F1HR – FRONT_FPGA_1 Hard Reset
- F2HR – FRONT_FPGA_2 Hard Reset
- F3HR – FRONT_FPGA_3 Hard Reset
- F4HR – FRONT_FPGA_4 Hard Reset
- F5HR – FRONT_FPGA_5 Hard Reset
- DDHR – DDU_FPGA Hard Reset
- SPHR - SP_FPGA Hard Reset

ACT_CMR – Clock Manager Reset

Writing Logic ONE to specified bit(s) of this write-only register results in sending 50 ns reset pulse(s) to selected DCM(s). Reset pulse resets also DCM error counters described under CSR_CM1 – System Clock Manager 1 Status and CSR_CM2 – System Clock Manager 2 Status headings. The register address is applicable to all FPGAs.

Table 17

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	CMR2	CMR1	X

Here:
- X – Don't care bit
- CMR1 – Clock Manager 1 Reset
- CMR2 – Clock Manager 2 Reset

ACT_LCR – Link Counters Resets

Writing Logic ONE to specified bit(s) of this write-only register results in sending 25 ns reset pulse(s) to selected error counter(s) described under STS_VPC – Valid Pattern Counter, CSR_LNK – Link Control/Status and CSR_LEC – Link Error Counters headings. The register address is applicable to the FRONT_FPGA.

Table 18

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	VPR	TER	SLR	CER	EWR

Here:

- EWR – TLK2501 Error Word Counter (RXDV == HIGH, RXER == HIGH) Reset
- CER – TLK2501 Carrier Extend Counter (RXDV == LOW, RXER == HIGH) Reset
- SLR – FINISAR optical receiver Signal Loss Counter (RXSD goes LOW) Reset
- TER – PRBS Test Error Counter Reset
- VPR – Valid Pattern Counter Reset

ACT_XFR – FIFO Resets

Writing Logic ONE to a specified bit of this write-only register results in sending a 25 ns reset pulse to corresponding FIFO(s). The register address is applicable to the FRONT_FPGA, DDU_FPGA, and SP_FPGA.

Table 19

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	BFR	DFR	PFR	SFR	TFR	X

Here:

- TFR – Test FIFO Reset (Init);
- SFR – Spy FIFO Reset (Init);
- PFR – Pipeline FIFO Reset (Init);
- DFR – DAQ FIFO Reset (Init). It also resets L1 Accept FIFO, ring buffer read/write pointers, and event builder FSM;
- BFR – Barrel FIFO Reset.

ACT_ACR – Address Counters Reset(s)

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 25 ns reset pulse to a corresponding address counter. The register address is applicable to FRONT_FPGA and SP_FPGA.

Table 20

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	PTR	GLR	LPR

Here:

- LPR – Local Phi LUT Address Counter Reset in FRONT_FPGAs;
- GLR – Global Phi/Eta/DT LUT Address Counter Reset in FRONT_FPGAs;
- PTR – PT LUT Address Counter Reset in SP_FPGA;

ACT_TST – Run Tests

Writing “1” to specified bit(s) of this write-only register initiates test pulse train(s), preloaded in test FIFOs.

Table 21

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	RBT	X	X	X	X	X

Here:

- RBT – Run Barrel interface test. The DT_BC0 line becomes HI and stays HI, until the Barrel FIFO (BF) empties.

Control/Status Register Group

STS_CCB – Status of the Backplane CCB command bus.

This read-only register remembers previous and displays current state of the CCB command bus. The register address is valid for the VME_FPGA only.

Table 22

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		CMD5	CMD4	CMD3	CMD2	CMD1	CMD0			CML5	CML4	CML3	CML2	CML1	CML0
		CCB_CMD Current State								CCB_CMD Last Command					

Here:

- CMD [5:0] – current state of the backplane CCB command bus (positive logic)
- CML [5:0] – latched state of the previous CCB command (positive logic)

STS_ANA – CCB Analyzer

This register stores a sequence of up to 64 CCB commands. The analyzer content is reset on power-up and on any write cycle addressed to this register.

Table 23

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L1ACC	BC0	ANA5	ANA4	ANA3	ANA2	ANA1	ANA0	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0	ECRES	BCRES
		Analyzer Word Count						CCB Command							

Here:

- L1ACC – L1 Accept
- BC0 – Decoded by CC B the BC0 command
- CMD [5:0] –CCB command code
- ECRES – Event Counter Reset
- BCRES – Bunch Counter Reset
- ANA [5:0] – Analyzer Word Count after the current word has been read out.

STS_VPC – Valid Pattern Counter

This read-only register is intended to monitor incoming muon rate for each link by counting the number of Valid Pattern bits at the Alignment FIFO output. The counter control follows that of the event counter: it is reset on the CCB_L1RES, and CCB_ECRES commands and enabled, when data taking state machine is in an L1A_RUN state, see Figure 1 for details on L1Accept control. The STS_VPC address is applicable to FRONT_FPGAs.

Table 24

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VP15	VP14	VP13	VP12	VP11	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
Valid Pattern Counter															

CSR_CID – Chip ID Register

This read-only register keeps a firmware release date in the format shown in the table below. Register address is applicable to all FPGAs.

Table 25

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
YY				MM				NN			DD				

Here:

- DD – Day Code (01…31)
- NN – FPGA Number (0...7), which corresponds to 8 FPGA chips, numbered in the following order: VM, F1, F2, F3, F4, F5, DD, SP.
- MM – Month Code (01…12)
- YY – Year Code (00…15)

CSR_CLK – System Clock Control/Status

This read/write register controls the source of the TLK2501 80.1574 MHz reference clock, which could be either external VCXO clock (default) or FRONT_FPGA DCM2 clock. The CSR_CLK address is applicable to FRONT_FPGAs.

Table 26

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RCS	R
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	RCS	W

Here:

- X – Don't care bit
- RCS – TLK2501 Reference Clock Select bit.
  "0" selects the DCM2 clock
  "1" selects the VCXO clock (default value).

CSR_CM1 – System Clock Manager 1 Status

This read-only register keeps history of Digital Clock Manager 1 behavior after the last ACT_CMR command. Its default value is 0x0004, which means that all enabled DCM1 features locked and there were no errors since last reset. For all FPGAs DCM1 is a DCM with internal feedback, distributing system clock all over the chip, including link clocking for FRONT_FPGA and DDU_FPGA.

Table 27

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LCK1 Counter				CST1 Counter				0	0	0	0	0	LCK1	CST1	PSO1

Here:

- PSO1 – Phase Shift Overflow, should be LOW for normal operation

- CST1 – Input Clock Stopped Toggling
- CST1 Counter – “loss of input clock” counter. It counts number of “CST2 go HIGH” after last DCM1 reset. Counter stops when reaches its maximum value of 15.
- LCK1 – All enabled DCM features locked
- LCK1 Counter – “loss of lock” counter. It counts number of “LCK2 go LOW” after last DCM1 reset. Counter stops when reaches its maximum value of 15.

CSR_CM2 – System Clock Manager 2 Status

This read-only register keeps history of Digital Clock Manager 2 behavior after the last ACT_CMR command. Its default value is 0x0004, which means that all enabled DCM2 features locked and there were no errors since last reset. For VME_FPGA DCM2 is a DCM with external feedback, distributing system clock all over the board. In FRONT_FPGA(s) DCM2 multiplies by 2 system clock.

Table 28

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LCK2 Counter				CST2 Counter				0	0	0	0	0	LCK2	CST2	PSO2

Here:

- PSO2 – Phase Shift Overflow, should be LOW for normal operation
- CST2 – Input Clock Stopped Toggling
- CST2 Counter – “loss of input clock” counter. It counts number of “CST2 go HIGH” after last DCM2 reset. Counter stops when reaches its maximum value of 15.
- LCK2 – All enabled DCM features locked
- LCK2 Counter – “lost of lock” counter. It counts number of “LCK2 go LOW” after last DCM2 reset. Counter stops when reaches its maximum value of 15.

CSR_BSY – Busy Control/Status

In the VME_FPGA the CSR_BSY register displays status of seven input and one output BSY lines. Besides, it carries eight mask bits, so each input or/and VME_FPGA output can be either disabled or enabled:

BSY0 = (BSY1*BSC1 + BSY2*BSC2 + BSY3*BSC3 + BSY4*BSC4 + BSY5*BSC5 + BSY6*BSC6 + BSY7 *BSC7 + BSY0_INT) * BSC0

Indexes 0…7 stand for chip numbers; see Table 7 and/or Table 25 for chip numbering scheme, and BSY0_INT is an internal busy status o the VME_FPGA, which is “1” when counting of CCB_L1ACCs is stopped (disabled).

The FRONT_FPGA sets BSY to “1”, when either the Bunch counter carries 0xFFF=4095 value, or link resynch on CCB_L1RES failed (the AF word count remains zero).

Table 29

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
BSC7	BSC6	BSC5	BSC4	BSC3	BSC2	BSC1	BSC0	BSY7	BSY6	BSY5	BSY4	BSY3	BSY2	BSY1	BSY0	R
BSC7	BSC6	BSC5	BSC4	BSC3	BSC2	BSC1	BSC0	X	X	X	X	X	X	X	X	W

Here:

- X – Don’t care bit
- BSC [7:0] – Busy Chip mask for SP, DD, F5…F1, and VM chips
- BSY [7:0] – Busy status for SP, DD, F5…F1, and VM chips

CSR_RDY – Ready Control/Status

In the VME_FPGA the CSR_RDY register displays status of seven input and one output RDY lines. Besides, it carries eight mask bits, so each input or/and VME_FPGA output can be either disabled or enabled:

RDY0 = (RDY1*RDC1 + RDY2*RDC2 + RDY3*RDC3 + RDY4*RDC4 + RDY5*RDC5 + RDY6*RDC6 + RDY7 *RDC7) * RDY0_INT *RDC0

Indexes 0…7 stand for chip numbers; see Table 7 and/or Table 25 for chip numbering scheme, and RDY0_INT is an internal ready status of the VME_FPGA, which is “1” when passing of CCB_L1ACCs to the FC bus is enabled.

The FRONT_FPGA sets RDY to “1”, when link resynchronization initiated by CCB_L1RES completed a success (the Alignment FIFO is neither empty, nor full). Only links with enabled TLK2501 receivers contribute to the chip’s RDY status; see CSR_LNK – Link Control/Status register for a DVEN bit description.

Table 30

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
RDC7	RDC6	RDC5	RDC4	RDC3	RDC2	RDC1	RDC0	RDY7	RDY6	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	R
RDC7	RDC6	RDC5	RDC4	RDC3	RDC2	RDC1	RDC0	X	X	X	X	X	X	X	X	W

Here:

- X – Don’t care bit
- RDC [7:0] – Ready Chip mask for SP, DD, F5…F1, and VM chips
- RDY [7:0] – Ready status for SP, DD, F5…F1, and VM chips

CSR_WOF – Warning-of-OverFlow Control/Status

In the VME_FPGA the CSR_WOF register displays status of seven input and one output WOF lines. Besides, it carries eight mask bits, so each input or/and VME_FPGA output can be either disabled or enabled:

WOF0 = (WOF1*WOC1 + WOF2*WOC2 + WOF3*WOC3 + WOF4*WOC4 + WOF5*WOC5 + WOF6*WOC6 + WOF7 *WOC7) * WOC0

Indexes 0…7 stand for chip numbers; see Table 7 and/or Table 25 for chip numbering scheme.

The FRONT_FPGA sets WOF to “1”, when either the DAQ FIFO or the Ring Buffer are full. It drops WOF to “0” when both buffers become empty.

Table 31

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
WOC7	WOC6	WOC5	WOC4	WOC3	WOC2	WOC1	WOC0	WOF7	WOF6	WOF5	WOF4	WOF3	WOF2	WOF1	WOF0	R
WOC7	WOC6	WOC5	WOC4	WOC3	WOC2	WOC1	WOC0	X	X	X	X	X	X	X	X	W

Here:

- X – Don’t care bit
- WOC [7:0] – Warning-of-OverFlow Chip mask for SP, DD, F5…F1, and VM chips
- WOF [7:0] – Warning-of-OverFlow status for SP, DD, F5…F1, and VM chips

CSR_OSY – Out-of-Synch Control / Status

In the FRONT_FPGA this register shows a timing offset between BC0 marks, sent by the MPC and coming out of the Alignment FIFO, and the local bunch crossing counter (BXN) value. The BC0 mark strobes the BXN value into the offset register.

If the offset register content is not equal to zero for a given link, an Out-of-Synch status is generated. Bit D12 of the Out-of-Synch register allows masking the out-of-synch status individually for each link before the combined fast monitoring OSY signal is sent over to the VME_FPGA. Besides, link OSY status is reported only if the corresponding TLK2501 device is enabled, i.e. bit DVEN=1, see the CSR_LNK – Link Control/Status register description.

See the CSR_BCO register description on how to adjust the BXN offset value to bring the control and data timing to synch.

In the VME_FPGA the CSR_OSY register displays status of seven input and one output OSY lines. Besides, it carries eight mask bits, so each input or/and output can be either disabled or enabled:

OSY0 = (OSY1*OSC1 + OSY2*OSC2 + OSY3*OSC3 + OSY4*OSC4 + OSY5*OSC5 + OSY6*OSC6 + OSY7 *OSC7) * OSC0

Indexes 0…7 stand for chip numbers; see Table 7 and/or Table 25 for chip numbering scheme.

Table 32 FRONT_FPGA CSR_OSY register bit assignment, one register per muon.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
OSM	0	0	0	OFF11	OFF10	OFF9	OFF8	OFF7	OFF6	OFF5	OFF4	OFF3	OFF2	OFF1	OFF0	R
OSM	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	W

Here:

- X – Don’t care bit
- OFF [10:0] = offset register, default value on power-up is 0x7FF.
- OSM – Out-of-Synch link Mask, default value is “1” – The Out-of-Synch condition, if exists, is sent to the chip output.

Table 33 VME_FPGA CSR_OSY register bit assignment

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
OSC7	OSC6	OSC5	OSC4	OSC3	OSC2	OSC1	OSC0	OSY7	OSY6	OSY5	OSY4	OSY3	OSY2	OSY1	OSY0	R
OSC7	OSC6	OSC5	OSC4	OSC3	OSC2	OSC1	OSC0	X	X	X	X	X	X	X	X	W

Here:

- X – Don’t care bit
- OSC [7:0] – Out-of-Synch Chip mask for SP, DD, F5…F1, and VM chips
- OSY [7:0] – Out-of-Synch status for SP, DD, F5…F1, and VM chips

CSR_CCD – CCB Command Delay – obsolete for Firmware Versions after 25-Aug-2003

This read/write register controls the CCB command timing inside the SP02. Writing non-zero values into this register introduces additional delay for all CCB commands, so that the entire SP02 timing gets shifted. Using this register is the only way to adjust the SP02 timing to the input link timing.

Table 34

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	CDS6	CDS5	CDS4	CDS3	CDS2	CDS1	CDS0	0	0	CCD5	CCD4	CCD3	CCD2	CCD1	CCD0	R

X	X	X	X	X	X	X	X	X	X	CCD5	CCD4	CCD3	CCD2	CCD1	CCD0	W

Here:

- X – Don't care bit
- CCD [5:0] = 0…63 delays CCB commands by 1…64 bunch crossings before passing them to the internal Fast Control bus.
- CDS [6:0] = 1…64 Command Delay Status, reports an actual delay setting.

CSR_BCO – Bunch Counter Offset

This read/write register controls the Bunch Counter Offset value. The whole idea of loading the bunch counter with an offset value arises from the need to match two timings in the FRONT_FPGA: the CCB control timing and the optical data-link timing. The bunch counter starts counting on the first CCB_BC0 after the CCB_L1STT command, i.e. on the control timing. But its job is to monitor BC0 marks in the data path, i.e. the data timing. The requirement is that the bunch counter be adjusted to the data timing, since the bunch counter value is an intrinsic part of the event format. An offset between the two timings may be either positive or negative. The offset is positive, if the CCB_BC0 command comes later than the BC0 mark. We would need to download a small positive value in the CSR_BCO register to compensate for such an offset. The offset is negative, if the CCB_BC0 command comes earlier than the BC0 mark. We would need to download a slightly less than the maximum bunch crossing value in the CSR_BCO register to compensate for such an offset. A maximum bunch crossing value equals to 923 for the test beam at SPS and 3563 for LHC operations. On the contrary, in the CSR_OSY register uncompensated positive offsets would be seen as large values, while uncompensated negative offsets would be seen as small values.

The CSR_BCO adjustment makes sense to perform only after the Alignment FIFO has been adjusted. Use the following procedure to make an adjustment:

- ⇒ Set the CSR_BCO = 0 (default value);
- ⇒ Start data taking;
- ⇒ Read the CSR_OSY registers for each active link. If timing in the Peripheral Crate has been set correctly and link alignment procedure has been performed correctly, the CSR_OSY values for all active links should be the same; If this value is not zero, the red OSY LED should be ON.
- ⇒ Find a complement to the CSR_OSY value (with respect to a maximum bx number);
- ⇒ Stop data taking;
- ⇒ Load the found value in the CSR_BCO register;
- ⇒ Start data taking;
- ⇒ Read the CSR_OSY registers for each active link. All links should show zero offset, and the red OSY LED should go OFF.

Table 35

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
BCM	0	0	0	BCO11	BCO10	BCO9	BCO08	BCO7	BCO6	BCO5	BCO4	BCO3	BCO2	BCO1	BCO0	R
BCM	X	X	X	BCO11	BCO10	BCO9	BCO08	BCO7	BCO6	BCO5	BCO4	BCO3	BCO2	BCO1	BCO0	W

Here:

- X – Don't care bit

- BCO [11:0] = 0…4095 Bunch Counter Offset value. Valid values are 0...923 for the test beam at SPS and 0...3563 for LHC operations.
- BCM = 1/0 – SPS beam/LHC beam or 923/3563 bunch crossings per turn.

CSR_L1D – L1 Accept Delay

This read/write register controls the L1 Accept timing inside the SP02. Writing non-zero values into this register introduces an additional delay for L1 Accepts. Using this register is the only way to adjust for a "negative" timing, when L1 Accept trigger arrives earlier than data.

Table 36

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
L1S7	L1S6	L1S5	L1S4	L1S3	L1S2	L1S1	L1S0	0	L1D6	L1D5	L1D4	L1D3	L1D2	L1D1	L1D0	R
X	X	X	X	X	X	X	X	X	L1D6	L1D5	L1D4	L1D3	L1D2	L1D1	L1D0	W

Here:

- X – Don't care bit
- L1D [6:0] = 0…127 delays L1 Accept by 1…128 bunch crossings before passing it to the internal logic.
- L1S [7:0] = 1…128 L1 Accept Delay Status, reports an actual delay setting.

CSR_LEC – Link Error Counters

This read-only register monitors all possible link errors. The TLK2501 synchronization procedure, when the MPC switches TLK2501 transmitters into idle mode for 128 bunch crossings, always precedes the normal operation. Normal receiving operation assumes RXSD and RXDV to be High and RXER to be Low. To facilitate monitoring of error conditions, any combination of RXSD, RXDV and RXER other than normal is detected and countered. Error conditions are accumulated over time, starting from the previous synchronization procedure. Counter stops when it reaches its maximum value. The counters are reset on L1_Reset and begin count errors after Alignment FIFO has been enabled for writing. Addressing the ACT_LER register provides an alternative reset option.

Table 37

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SLC3	SLC2	SLC1	SLC0	CEC3	CEC2	CEC1	CEC0	EWC7	EWC6	EWC5	EWC4	EWC3	EWC2	EWC1	EWC0
Signal Loss Counter				Carrier Extend Counter				Error Word Counter							

Here:

- EWC [7:0] – TLK2501 Error Word Counter (RXDV == High, RXER == High)
- CEC [3:0] – TLK2501 Carrier Extend Counter (RXDV == Low, RXER == High)
- SLC [3:0] – FINISAR optical receiver Signal Loss Counter (RXSD goes Low)

CSR_AF – Alignment FIFO Status

This read-only register shows the number of words currently sitting in the Alignment FIFO (AF). After a link synchronization procedure has been performed, Alignment FIFOs for different links may show different word counts. Dispersion of word count values corresponds to the dispersion of link latencies. Adjusting the CCB clock in the Track-Finder crate, so that a minimum word count would be equal to 1, minimizes the overall time required to align all muon links. Register address is applicable to FRONT_FPGA (3 each) and to SP_FPGA (2 each – MA = 0|1|2). The maximum available value is 31.

Table 38

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AFFF	AFEF	0	0	0	0	0	AFC8	AFC7	AFC6	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0
Flags							Alignment FIFO Word Count								

Here:

- AFC [8:0] – Alignment FIFO Read Word Count
- AFFF – Alignment FIFO Full Flag
- AFEF – Alignment FIFO Empty Flag

CSR_TF – Test FIFO Status

This read-only register shows the number of words currently loaded to the Test FIFO (TF) and FIFO Flags. The maximum available TF capacity is 1024 16-bit words. Register address is applicable to FRONT_FPGA (3 each), DDU_FPGA (1 each) and SP_FPGA (3 each).

Table 39

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFFF	TFEF	0	0	0	TFC10	TFC9	TFC8	TFC7	TFC6	TFC5	TFC4	TFC3	TFC2	TFC1	TFC0
Flags					Test FIFO Word Count										

Here:

- TFC [10:0] – Test FIFO Word Count
- TFFF – Test FIFO Full Flag
- TFEF – Test FIFO Empty Flag

CSR_SF – Spy FIFO Status

This read-only register shows the number of words currently sitting in the Spy FIFO (SF). One would probably want to know this value before setting up the BLT read cycle to read out the SF content. Maximum available SF capacity is 1024 16-bit words. Register address is applicable to FRONT_FPGA (3 each), DDU_FPGA (1 each) and SP_FPGA (3 each).

Table 40

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFFF	SFEF	RXDV	RXER	0	SFC10	SFC9	SFC8	SFC7	SFC6	SFC5	SFC4	SFC3	SFC2	SFC1	SFC0
Flags		RX Status			Spy FIFO Word Count										

Here:

- SFC [10:0] – Spy FIFO Word Count
- SFFF – Spy FIFO Full Flag
- SFEF – Spy FIFO Empty Flag
- RXDV, RXER – TLK2501 Receiver Status for the last data read out from the Spy FIFO

CSR_PF – Pipeline FIFO Status

This read-only register shows the number of words currently loaded to the Pipeline FIFO (PF) and FIFO Flags. The maximum available PF capacity is 1024 18-bit words. Register address is applicable to FRONT_FPGA.

Table 41

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PFFF	PFEF	0	0	0	PFC10	PFC9	PFC8	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0
Flags					Pipeline FIFO Word Count										

Here:
- PFC [10:0] – Pipeline FIFO Word Count
- PFFF – Pipeline FIFO Full Flag
- PFEF – Pipeline FIFO Empty Flag

CSR_DF – DAQ FIFO Status

This read-only register shows the number of words currently loaded to the DAQ FIFO (DF) and link error status for muon data words. The maximum available DF capacity is 4096 18-bit words. Register address is applicable to FRONT_FPGA. In the readout event format, see Table 63, the Synchronization Error (SE) bit resides in the second data frame. To provide for error analysis, the CSR_DF register retrieves Receive Error flags for both data frames, making them available after the second frame has been read out.

Table 42

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
PFRE	CFRE	0	DFC12	DFC11	DFC10	DFC9	DFC8	DFC7	DFC6	DFC5	DFC4	DFC3	DFC2	DFC1	DFC0
Link Errors			DAQ FIFO Word Count												

Here:
- DFC [12:0] – DAQ FIFO Word Count
- CFRE – Current Frame Receive Error Flag
- PFRE – Previous Frame Receive Error Flag

CSR_LF – L1 Accept FIFO Status

This read-only register shows the number of words currently loaded to the L1 Accept FIFO (LF) and FIFO Flags. The maximum available LF capacity is 1024 54-bit words. Register address is applicable to FRONT_FPGA.

Table 43

D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
LFFF	LFEF	0	0	0	LFC10	LFC9	LFC8	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
Flags					L1 Accept FIFO Word Count										

Here:
- LFC [10:0] – L1 Accept FIFO Word Count
- LFFF – L1 Accept FIFO Full Flag
- LFEF – L1 Accept FIFO Empty Flag

CSR_RBW – Ring Buffer Write Pointer

This read-only register shows the current position of the Ring Buffer Write Pointer. Ring Buffer is a 54 bit x 1024 word temporary storage for muon data, before they are get reformatted and put in the DAQ FIFO for readout. The register is used for firmware debugging.

Table 44

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	RBW9	RBW8	RBW7	RBW6	RBW5	RBW4	RBW3	RBW2	RBW1	RBW0
						Ring Buffer Write Pointer									

Here:

– RBW [9:0] – Ring Buffer Write Pointer

CSR_RBR – Ring Buffer Read Pointer

This read-only register shows the current position of the Ring Buffer Read Pointer. Ring Buffer is a 54 bit x 1024 word temporary storage for muon data, before they are get reformatted and put in the DAQ FIFO for readout. The register is used for firmware debugging.

Table 45

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	RBR9	RBR8	RBR7	RBR6	RBR5	RBR4	RBR3	RBR2	RBR1	RBR0
						Ring Buffer Read Pointer									

Here:

– RBR [9:0] – Ring Buffer Read Pointer

CSR_LNK – Link Control/Status

This register provides static link control and status directly to and from both Finisar and TLK2501 transceivers' pins. Read-only upper byte shows receiver status, while lower byte provides access to control pins. Under the normal operational conditions register value equals to 0x0511 for a receiving link and equals to 0x0014 for a transmitting link. When TSEN is asserted High, results of pseudorandom bit stream tests can be monitored on the RXER output. A High on this terminal indicates that valid PRBS is being received. The PRBS test counter counts (RXER goes Low) events, when TSEN is High. It stops, when reaches its maximum value of 31. Counter reset is provided through addressing to the ACT_LER register.

When the TLK2501 device is disabled (DVEN is set to "0") the corresponding ready/busy link status is masked off and does not contribute to the overall FRONT_FPGA fast monitoring status.

Table 46

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
TEC4	TEC3	TEC2	TEC1	TEC0	RXDV	RXER	RXSD	0	TSEN	LPEN	DVEN	RFDI	TXEN	TXER	TXDI	R
X	X	X	X	X	X	X	X	X	TSEN	LPEN	DVEN	RFDI	TXEN	TXER	TXDI	W

Here:

– X – Don't care bit;

– TXDI = 1/0 – Disable/Enable the FINISAR optical Transmitter;

– {TXEN, TXER} = {Transmit Enable, Error Coding} – Transmit Data Control:

  - {TXEN,TXER} = {0,0} – Transmit Idle Character (0xC5BC or 0x50BC);

    - {TXEN,TXER} = {0,1} – Transmit Carrier Extend (0xF7F7);
    - {TXEN,TXER} = {1,0} – Transmit Normal Data Character;
    - {TXEN,TXER} = {1,1} – Transmit Error Propagation (0xFEFE);
- RFDI = 1/0 – Disable/Enable the TLK2501 Reference clock;
- DVEN = 1/0 – Enable/Disable the TLK2501 Device;
- LPEN = 1/0 – Enable/Disable the TLK2501 Loop mode;
- TSEN = 1/0 – Enable/Disable the TLK2501 Pseudorandom Bit Stream (PRBS) Test ;
- RXSD = 1/0 – Signal Detect/No Signal from FINISAR optical receiver;
- { RXDV, RXER} = { Receive Data Valid, Receive Error} – Receive Status Signals
    - {RXDV, RXER} = {0,0} – Receive Idle Character (0xC5BC or 0x50BC);
    - {RXDV, RXER} = {0,1} – Receive Carrier Extend (0xF7F7);
    - {RXDV, RXER} = {1,0} – Receive Normal Data Character;
    - {RXDV, RXER} = {1,1} – Receive Error Propagation (0xFEFE);
- TEC [4:0] – PRBS Test Error Counter;

CSR_AFD - Alignment FIFO Read Delay

This read/write register controls delaying of AF reads after an L1 Reset occurred. It can be used to optimize a muon alignment budget. The register resides in the FRONT_FPGA.

Table 47

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	0	0	0	0	0	AFD7	AFD6	AFD5	AFD4	AFD3	AFD2	AFD1	AFD0	R
X	X	X	X	X	X	X	X	AFD7	AFD6	AFD5	AFD4	AFD3	AFD2	AFD1	AFD0	W
								Alignment FIFO Read Delay								

Here:

- AFD = 0…255 – AF resumes reads on the 1st... 256th clock after L1 Reset has been received. Default value on power-up is 176.

CSR_SFC – Spy FIFO Configuration

In the VME_FPGA this register defines the delay inserted between the CCB test commands and the FC_SFRUN command on the internal FC bus, see Table 2. The delay is intended to compensate for the time required for the corresponding test data to reach the Spy FIFO input. The delay is not applicable to the CCB_L1ACC command. The register also determines if request for data is one-time or persistent. Power-up default state for this register is 0x0000.

Table 48 VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
SFM	SFRL	SFRS	SFRM	SFRT	0	SFD9	SFD8	SFD7	SFD6	SFD5	SFD4	SFD3	SFD2	SFD1	SFD0	R
SFM	SFRL	SFRS	SFRM	SFRT	X	SFD9	SFD8	SFD7	SFD6	SFD5	SFD4	SFD3	SFD2	SFD1	SFD0	W
Mode	Requests					Spy FIFO Delay Setting										

Here:

- SFD [9:0] = 0…1023 - Spy FIFO starts writing data, when 1…1024 bunch crossings have passed after the requested event.
- SFRT = 1/0 – store/don't store data on the next CCB_TPTMB command

- SFRM = 1/0 – store/don’t store data on the next CCB_TPMPC command
- SFRS = 1/0 – store/don’t store data on the next CCB_TPSP command
- SFRL = 1/0 – store/don’t store data on the next CCB_L1ACC command
- SFM = 1/0 – persistent/one-time request. Persistent request stores data on all events that followed. One-time request stores data on the next event only and self-resets after that.

In the FRONT_FPGA this register defines the data source for the Spy FIFO input and the number of beam crossings to be stored upon receiving the FC_SFRUN command. Note that the actual number of 16-bit words, saved in the Spy FIFO is twice as big, since each beam crossing data consists of two frames. Moreover, each event stored upon L1 Accept command has a two-word header: an L1 Accept counter value and a Beam Crossing Counter value, which are added to the number of bunch crossings specified by the register → to be implemented!!

Table 49 FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
SFS	0	0	0	0	0	0	SFB8	SFB7	SFB6	SFB5	SFB4	SFB3	SFB2	SFB1	SFB0	R
SFS	X	X	X	X	X	X	SFB8	SFB7	SFB6	SFB5	SFB4	SFB3	SFB2	SFB1	SFB0	W
Source							Spy FIFO Bunch Crossing Count									

Here:
- X – Don’t care bit;
- SFB [8:0] = 0…511 - FRONT_FPGA Spy FIFO grabs data from 1…512 bunch crossings
- SFS – FRONT_FPGA Spy FIFO data source:
  ”1” – Pipeline FIFO output
  ”0” – Alignment FIFO output

CSR_PFD – Pipeline FIFO Data Delay

This read/write register controls data delay in the Pipeline FIFO to compensate for L1 Accept latency. Default value on power-up is 128.

Table 50

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	0	0	0	0	0	PFD7	PFD6	PFD5	PFD4	PFD3	PFD2	PFD1	PFD0	R
X	X	X	X	X	X	X	X	PFD7	PFD6	PFD5	PFD4	PFD3	PFD2	PFD1	PFD0	W
								Pipeline FIFO Data Delay								

Here:
- X – Don’t care bit;
- PFD = 0…255 – PF delays data for 1... 256 bunch crossings or up to 6.4 µsec.

CSR_DFC – DAQ FIFO Configuration

This read/write register controls event size or the number of bunch crossing to be saved into the DAQ FIFO upon receiving an L1 Accept. When a zero DFB value is loaded, no muon data is saved on L1 Accept, and each event consists only of a Header block, see Table 63 for details. Default event size on power-up is 2.

Table 51

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	0	0	0	0	0	0	0	0	DFB4	DFB3	DFB2	DFB1	DFB0	R
X	X	X	X	X	X	X	X	X	X	X	DFB4	DFB3	DFB2	DFB1	DFB0	W
											DAQ FIFO Bunch Crossings Count					

Here:

- X – Don't care bit;
- DFB [4:0] = 0…31 – DAQ FIFO stores data from 0…31 bunch crossings.

CSR_CFG – FPGA Configuration Done Status

Addressing to this read-only register allows verifying the Configuration Done status of the FRONT_FPGAs, DDU_FPGA, and SP_FPGA after hard resets. The register address is applicable to the VME_FPGA only. Register's default value is 0xFE, when all, including the mezzanine card's chips are in place. Being Low during configuration, Configuration Done High indicates completion of the configuration.

To make sure all FPGA chips are present on board, the CSR_CFG command should be executed twice: first, when chips are engaged in the configuration process, i.e. immediately after the ACT_HR command, and second, after a 5 sec pause, when the configuration is definitely completed. If there is a missing FPGA chip on board (a mezzanine card not installed, for example), then the corresponding Configuration Done line remains floating, and could be sensed by the VME_FPGA either as a logic ONE or logic ZERO. But in any case, Configuration Done line for a missing chip would retain its state, while the one for a successfully configured FPGA will be LOW on the first read and HIGH on the second read.

Table 52

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	SPCD	DDCD	F5CD	F4CD	F3CD	F2CD	F1CD	0
								Configuration Done Status							

Here:

- F1CD – FRONT_FPGA_1 Configuration Done
- F2CD – FRONT_FPGA_2 Configuration Done
- F3CD – FRONT_FPGA_3 Configuration Done
- F4CD – FRONT_FPGA_4 Configuration Done
- F5CD – FRONT_FPGA_5 Configuration Done
- DDCD – DDU_FPGA Configuration Done
- SPCD - SP_FPGA Configuration Done

CSR_INI – FPGA Init Status

Addressing to this read-only register allows verifying the INIT_B pin status of FRONT_FPGAs, DDU_FPGA, and SP_FPGA after hard resets. The register address is applicable to the VME_FPGA only. Default register value is 0xF7. INIT_B Low indicates memory is being cleared. The INIT_B pin transitions HIGH when the clearing of configuration memory is complete. INIT_B LOW during configuration indicates an error.

Table 53

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	SPIN	DDIN	F5IN	F4IN	F3IN	F2IN	F1IN	0
								Init_B or Config Error Status							

Here:
- F1IN – FRONT_FPGA_1 Configuration error if Low
- F2IN – FRONT_FPGA_2 Configuration error if Low
- F3IN – FRONT_FPGA_3 Configuration error if Low
- F4IN – FRONT_FPGA_4 Configuration error if Low
- F5IN – FRONT_FPGA_5 Configuration error if Low
- DDIN – DDU_FPGA Configuration error if Low
- SPIN - SP_FPGA Configuration error if Low

Address Counter Register Group

CNT_LPL, CNT_LPH – Local Phi LUT Address Counter

This read/write registers carry current value of the local phi LUT address counter, as shown in Table 54 and Table 55. Default register value on power-up is zero. The counter is common for all local LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_LP register in the chip. The counter can be reset with ACT_ACR command.

Table 54 Local Phi LUT Address Counter, Lower Bits

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LA15	LA14	LA13	LA12	LA11	LA10	LA9	LA8	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0
Local Phi LUT Address Counter															

Table 55 Local Phi LUT Address Counter, Higher Bits

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	LA18	LA17	LA16
													Local Phi LUT AC		

Here:
- X – Don’t care bit;
- LA [18:0] = 0…524287 – Local Phi LUT Address Counter.

CNT_GLL, CNT_GLH – Global LUTs Address Counter

This read/write registers carry current value of the global LUTs address counter, as shown in Table 56 and Table 57. Default register value on power-up is zero. The counter is common for all global LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_GP/DAT_DT/DAT_GE register in the chip. The counter can be reset with ACT_ACR command.

Table 56 Global LUTs Address Counter, Lower Bits

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GA15	GA14	GA13	GA12	GA11	GA10	GA9	GA8	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0
Global LUTs Address Counter															

Table 57 Global LUTs Address Counter, Higher Bits

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	GA18	GA17	GA16
													Global LUTs AC		

Here:

- X – Don’t care bit;
- GA [18:0] = 0…524287 – Global LUTs Address Counter.

Data Register Group

DAT_LP – Local Phi LUT Data

This read/write registers provides access to the Local Phi LUT content. The LP LUT data format is shown in Table 58. Read/write transfers are performed on the LP LUT current address defined by the CNT_LPL and CNT_LPH values; after that the counter auto-increments. Note, that the local phi LUT address counter is common to all three muons, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

Table 58 Local Phi LUT Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LPB5	LPB4	LPB3	LPB2	LPB1	LPB0	LP9	LP8	LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0
Local Phi Bend						Local Phi									

Here:

- LP [9:0] = 0…1023 – Local Phi.
- LPB [5:0] = 0…31 – Local Phi Bend.

DAT_GP – Global Phi LUT Data

This read/write registers provides access to the Global Phi LUT content. The GP LUT data format is shown in Table 59. Read/write transfers are performed on the GP LUT current address defined by the CNT_GLL and CNT_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

Table 59 Global Phi LUT Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
				Global Phi											

Here:

- X – don’t care bit, returns zero on reads
- GP [11:0] = 0…4095 – Global Phi.

DAT_DT – Drift Tube Global Phi LUT Data

This read/write registers provides access to the Drift Tube Global Phi LUT content. The DT LUT data format is shown in Table 60. Read/write transfers are performed on the DT LUT current address defined by the CNT_GLL and CNT_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

Table 60 Drift Tube Global Phi LUT Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	DT11	DT10	DT9	DT8	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
				Drift Tube Global Phi											

Here:
- X – don't care bit, returns zero on reads
- DT [11:0] = 0…4095 – Global Phi.

DAT_GE – Global Eta LUT Data

This read/write registers provides access to the Global Eta LUT content. The GE LUT data format is shown in Table 61. Read/write transfers are performed on the GE LUT current address defined by the CNT_GLL and CNT_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

Table 61 Global Phi LUT Data

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	GE11	GE10	GE9	GE8	GE7	GE6	GE5	GE4	GE3	GE2	GE1	GE0
				Global Eta											

Here:
- X – don't care bit, returns zero on reads
- GE [11:0] = 0…4095 – Global Phi.

DAT_TF – Test FIFO Data

VME cycles addressed to this write-only register load data in the Test FIFO (TF). Preferred method for loading TF with data is setting up a BLT write cycle. Address is valid for FRONT_FPGA (3 each), DDU_FPGA (1 each), and SP_FPGA (3 each).

The output of the FRONT_FPGA TF is normally connected to the TLK2501 transmitter to provide a source of data patterns for link tests. Alternatively, during data taking phase TF data may be injected in the data steam, substituting the Alignment FIFO output for one or more bunch crossings. TF destination is defined by the CSR_TFC register. CCB fast control signals (TBD) are responsible for test pattern injection. Table 62 shows the TF data format, which, in fact, exactly follows the MPC – SP two-frame data format.

Data loaded into the TF cannot be verified by reading it back, since FIFO reads are destructive. Addressing to the CSR_TF register provides an indirect verification method of the current TF word count.

Table 62

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							FR1
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								FR2

Here:

- VP – Valid Pattern flag
- Quality - the more hits the higher track Quality
- CLCT Pattern # - the 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit.
- Wire Group ID - the 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111.
- CSC ID - the 4-bit CSC ID indicates the chamber # and runs from 1 to 9.
- BC0 - the Bunch Crossing Zero flag marks bunch zero data
- BX0 - the least significant bit of Bunch Crossing Number (BXN ranges from 0 to 3563).
- SE - Synchronization Error bit
- L/R - the Left/Right bend bit indicates whether the track is heading towards lower or higher strip number
- CLCT Pattern ID - For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber.

DDU_FPGA and SP_FPGA data formats TBD later.

DAT_SF – Spy FIFO Data

VME cycles addressed to this read-only register return data from the Spy FIFO (SF). Preferred method of reading the SF content is setting up BLT read cycles. Addressing to the CSR_SF register returns the current SF word count. Address is valid for FRONT_FPGA (3 each), DDU_FPGA (1 each), and SP_FPGA (3 each).

The FRONT_FPGA SF input could be connected to one of two signal sources: the Alignment FIFO output, and the Pipeline FIFO output, as defined by the CSR_TSC register. Data format of each source is identical to the one shown in Table 62. The process of collecting data into the SF is regulated by fast control commands.

DAT_DF – DAQ FIFO Data

VME cycles addressed to this read-only register retrieve event data from the DAQ FIFO (DF). The data format has a header followed by a specified number of data blocks. Each block is composed of 3 muons, 2 frames per muon, see Table 63 for details. The SP header structure follows the DMB header structure and starts with the number of data blocks or, in other words, the number of bunch crossings for which the muon data is presented. Two next words carry the L1 Accept or event number, and, finally, the fourth word is the bunch crossing counter reading for the first data block in the event. The header carries a specific signature of hexadecimal 0xF values to facilitate the separation of events. The data block format exactly follows the MPC-SP link format.

Table 63 Event Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word	Block
0xF				0xF				BC# – # of Bunch Crossings in Event								HD1	Header
0xF				EC [11:0] – Event Counter 12 Less Significant Bits												HD2	
0xF				EC [23:12] – Event Counter 12 Most Significant Bits												HD3	
0xF				BC [11:0] – Bunch Crossing Counter value for data block 1												HD4	
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							M1FR1	Data Block 1
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								M1FR2	
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							M2FR1	
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								M2FR2	
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							M3FR1	
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								M3FR2	
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							M1FR1	Data Block BC#
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								M1FR2	
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							M2FR1	
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								M2FR2	
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							M3FR1	
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								M3FR2	

Here:

- VP – Valid Pattern flag
- Quality - the more hits the higher track Quality
- CLCT Pattern # - the 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit.
- Wire Group ID - the 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111.
- CSC ID - the 4-bit CSC ID indicates the chamber # and runs from 1 to 9.
- BC0 - the Bunch Crossing Zero flag marks bunch zero data
- BX0 - the least significant bit of Bunch Crossing Number (BXN ranges from 0 to 3563 in LHC mode and from 0 to 923 in SPS mode).
- SE - Synchronization Error bit
- L/R - the Left/Right bend bit indicates whether the track is heading towards lower or higher strip number
- CLCT Pattern ID - For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber.

DAT_RW – Data Transfer Bus Read/Write Register

This register is used for backplane and internal data bus validation. It allows write/read cycles to be performed to/from each FPGA chip without affecting SP02 functionality in any way.

Table 64

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Validation Data Word															

History

Version 5.0 – Sep 01, 2003

1. Clock routing changed due to patches:
   - Eliminated the osc_clk input in the VME_FPGA;
   - Eliminated the clk_sel input in the VME_FPGA;
   - Returned two DCMs: internal and external to the VME_FPGA;
   - Eliminated the CSR_CLK register in the VME_FPGA;
   - Changed default value of the CSR_CLK register in the FRONT_FPGA from DCM to VCXO clock;
2. Changed the CCB_BC0 to DATA_BC0 adjustment scheme:
   - Eliminated the CSR_CCB register in the VME_FPGA;
   - Added the CSR_BCO register in the FRONT_FPGA (with the same access address);
   - Changed format of the CSR_OSY registers in the FRONT_FPGA, now it displays the latched bunch counter value without calculating positive/negative offsets;
3. Added data taking state diagrams in the interface description;
4. Added the STS_VPC (Valid Pattern Counter) register for each link in the FRONT_FPGA;
5. Renamed ACT_LER – Link Error Counters Resets to ACT_LCR – Link Counter Resets, added the VPR bit to reset the STS_VPC counter;
6. Fake L1Accept generated by CCB_TPxxx commands is ORed with the CCB_L1A line BEFORE the L1Accept delay, not AFTER;
7. Added intercept of the CCB_TPTMB(0x24) command;
8. Changed the CSR_SFC format in the VME_FPGA;

Version 5.1 – Nov 25, 2003

1. Changed the usage of the 39 and 3A access codes, Table 4. Previously identical data and program access is now split according to its function.
2. Changed the IDTB protocol from synchronous with a handshake to synchronous with a predetermined timing.
3. Added the CSR_BF(0x36) and DAT_BF(0x76) registers for the Barrel FIFO, Table 9;
4. Added the BF reset bit in the ACT_XFR, Table 19;
5. Added the ACT_ACR register;
6. Changed the CSR_LF address from 0x36 to 0x37, Table 9;

7. Changed the CSR_RBW address from 0x37 to 0x38, Table 9;
8. Changed the CSR_RBR address from 0x38 to 0x39, Table 9;
9. Eliminated the CNT_GEL/CNT_GEH/CNT_GPL/CNT_GPH registers;
10. Added the CNT_GLL/CNT_GLH registers;

Version 5.2 – Dec 10, 2003

1. Added DAT_GP register description
2. Added DAT_DT register description
3. Added DAT_GE register description

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[i] CSC Track Finder Crate Specification, created by Mike Matveev and updated by Alex Madorsky, December 12, 2002; http://www.phys.ufl.edu/~madorsky/TrackFinder/TF_backplane_v4.doc
[ii] ANSI/VITA 1.1-1997, American National Standard for VME64 Extensions.