SP02 Backplane Interfaces

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March 8, 2004
Version 5.6

This doc matches the vm_fa_dd_040308.evf and sp_0400308.evf configuration files.

CCB Interface

The CCB interface provides the SP02 with timing and trigger control signals distributed by the Clock and Control Board (CCB) over the backplane [i]. The backplane counts as many as 34 signal lines coming in and going out of the SP02. Table 1 groups backplane signals into four Groups. All GTLP lines are active LOW (negative bus logic).

The Clock Group includes a differential clock and clock_enable lines. For the TF prototype the enable line is expected to be always in a LOW state.

Table 1: SP02 CCB Interface Signals.

Signal	Lines	Direction	Type	Logic	Duration
Clock Group					
CCB_CLK	2	IN	Point-to-point	LVDS	40MHz
CCB_CLK_EN	1	IN	Bussed	GTLP	Pulse, n counts
Subtotal	**3**				
Fast Control Group					
CCB_CMD [5..0]	6	IN	Bussed	GTLP	Level
CCB_ECRES	1	IN	Bussed	GTLP	25ns
CCB_BCRES	1	IN	Bussed	GTLP	25ns
CCB_CMD_STR	1	IN	Bussed	GTLP	25ns
CCB_BX0	1	IN	Bussed	GTLP	25ns+ECL FP
CCB_L1ACC	1	IN	Bussed	GTLP	25ns+ECL FP
CCB_DAT [7..0]	8	IN	Bussed	GTLP	Level
CCB_DAT_STR	1	IN	Bussed	GTLP	25ns
CCB_RDY	1	IN	Bussed	GTLP	Static level
Subtotal	**21**				
Reload Group					
CCB_SP_HRES	1	IN	Bussed	GTLP	400ns
SP_CFG_DONE	1	OUT	Point-to-Point	GTLP	Level
Subtotal	**2**				
Reserved Group					
CCB_RSVD [3..0][#]	4	IN	Bussed	GTLP	25ns
SP_RSVD [3..0][*]	4	OUT	Bussed	GTLP	25ns
Subtotal	**8**				
Total	**34**				

[#] CCB_RSVD3 is assigned for CCB_L1RES – L1 Reset signal resets L1 buffers and resynchronizes optical links.
[*] SP_RSVD3 is assigned for SP_L1REQ – L1 request, local trigger generated by the SP_FPGA logic.

The Fast Control Group includes a ccb_ready status line, TTCrx command and data busses accompanied with strobes, and a few TTCrx signals, decoded by CCB. The Fast Control Group signals are valid when and only when the ccb_ready is LOW.

The Reload Group includes a hard_reset signal for reconfiguration of the SP02 FPGAs. In turn, the SP02 returns a configuration_done status to the CCB.

The Reserved Group is partially specified at the moment, see footnotes to Table 1.

The VME_FPGA delivers fast control signals to each SP02 FPGA via a 5-bit Fast Control (FC) bus. Table 2 sets correspondence between the FC and the CCB signals.

Table 2: SP02 Internal Control Bus and configuration control/status lines

FC/CCB Command Description	CCB Backplane Signal or Command Code	TTCvi Broadcast command data	FC/CCB Command Acronym	Fast Control Bus Command Code
No commands / Idle state			FC_NOCMD	fc_cmd[4:0]=5'b0_0000
L1 Accept	ccb_l1acc		FC_L1ACC CCB_L1ACC	fc_cmd[4:0]=5'h1_XXXX
Store Next Event into Spy FIFO, as determined by the CSR_SFC	Generated by the VME_FPGA		FC_SFRUN	fc_cmd[4:0]=5'hX_1XXX
Bunch Counter Reset	ccb_bcres	0x01	FC_BCRES CCB_BCRES	fc_cmd[4:0]=5'hX_X001
Event Counter Reset	ccb_ecres	0x02	FC_ECRES CCB_ECRES	fc_cmd[4:0]=5'hX_X010
Bunch & Event Counter Reset	ccb_beres	0x03	FC_BERES CCB_BERES	fc_cmd[4:0]=5'hX_X011
Bunch Crossing Zero Mark	ccb_cmd[5:0]=0x01	0x04	FC_BC0 CCB_BC0	fc_cmd[4:0]=5'hX_X100
L1 Reset – Resets L1 Buffers and Resynchronizes Optical Links	ccb_cmd[5:0]=0x03	0x0C	FC_L1RES CCB_L1RES	fc_cmd[4:0]=5'hX_X101
Start Data Taking	ccb_cmd[5:0]=0x06	0x18	FC_L1RUN CCB_L1STT	fc_cmd[4:0]=5'hX_X110
Stop Data Taking	ccb_cmd[5:0]=0x07	0x1C	CCB_L1STP	Handled by the VME_FPGA
Inject Test Pattern into SP. See details in CSR_TFC description	ccb_cmd[5:0]=0x2F	0xBC	FC_TFRUN CCB_TPSP	fc_cmd[4:0]=5'hX_X111
Inject Test Pattern into MPC	ccb_cmd[5:0]=0x30	0xC0	CCB_TPMPC	Handled by the VME_FPGA
Inject Test Pattern into TMB	ccb_cmd[5:0]=0x24	0x90	CCB_TPTMB	Handled by the VME_FPGA
Bunch Counter Reset	ccb_cmd[5:0]=0x32	0xC8	FC_BCRES CCB_BXRES	fc_cmd[4:0]=5'hX_X001
Hard Reset – reconfigures the SP02 FPGAs (as determined by the Configuration Mask register)	ccb_sp_hard_res			cfg_prog_n[7:1]
Configuration Done – reports on successful completion of the FPGA configuration (as determined by the Done Mask register)	sp_cfg_done			cfg_done[7:1]

The FC bus has two dedicated lines, one for L1 Accepts and another to initiate storing data into Spy FIFOs. Three more lines encode all other fast control commands. Signals on dedicated lines may coincide in time with encoded commands, while encoded commands are mutually exclusive.

Note, that data taking is stopped on power-up, so backplane CCB_L1ACC signals don't pass to the FC_L1ACC line. A sequence of CCB_L1STT and CCB_BC0 commands should be issued to let L1 Accepts pass to the internal FC bus, see Figure 1 for details on the L1Accept

State Machine (L1A_FSM). A CCB_L1STP command returns the L1A_FSM into the default L1A_STOP state from the L1A_RUN state. Besides, CCB_L1RES or CCB_BXRES commands return the L1A_FSM into the L1A_STOP state unconditionally. FRONT_FPGA passes link data to the SP02 LUTs and, hence, to the SP_FPGA only when the L1Accept FSM is in the L1A_RUN state, otherwise it selects LUT's zero address.

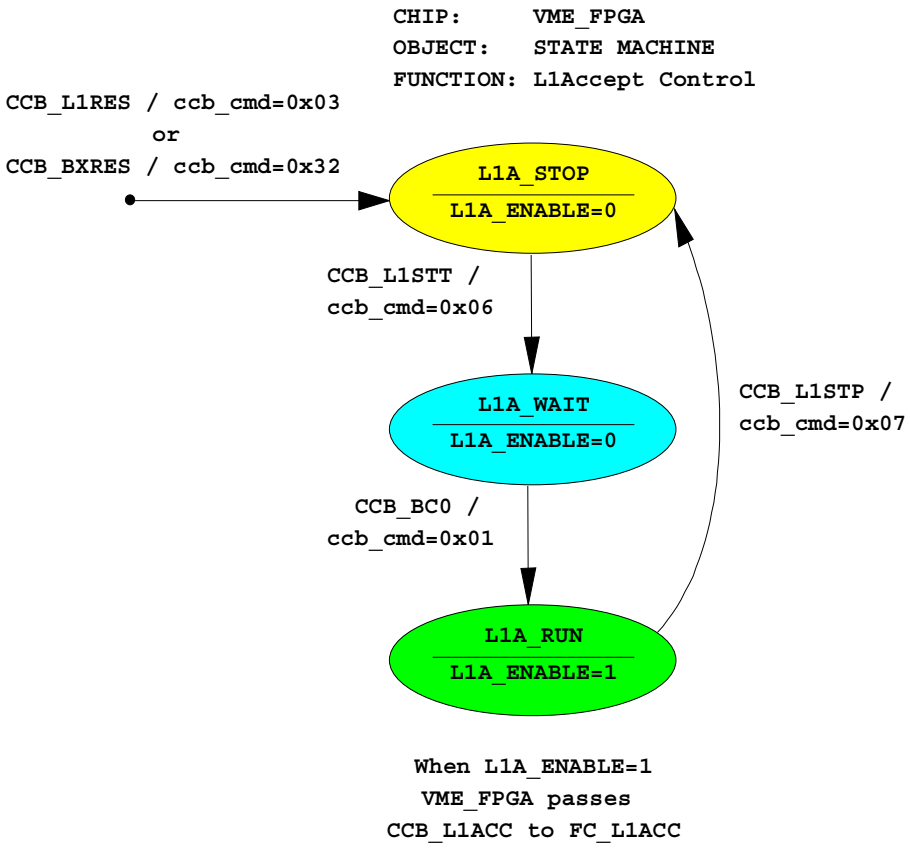

Figure 1 State Machine for L1Accept Control

An FC_SFRUN internal command requests storing next event into the Spy FIFO.

Bunch counter on power-up and/or after CCB_BCRES, CCB_BXRES, or CCB_L1RES commands is preloaded with a 0xFFF=4095 value. It starts counting from 1 and up upon receiving a CCB_BC0 command. Bunch counter rolls over to zero count, when it reaches its maximum value, which is 923 for the beamtest at SPS and 3563 for LHC operations.

Summary of fast control commands:

- CCB_BCRES – resets Bunch counters to 0xFFF = 4095;
- CCB_ECRES – resets Event counters;
- CCB_L1RES – resets Bunch counters to 0xFFF = 4095, resynchronizes optical links, resets readout buffers, resets Event counters, and returns the L1Accept FSM into the L1A_STOP state.

- CCB_BXRES – resets Bunch counters to 0xFFF = 4095, and returns the L1Accept FSM into the L1A_STOP state.
- CCB_L1STT – counting of CCB_L1ACCs to be resumed on the next CCB_BC0 command.
- CCB_L1STP –returns the L1Accept FSM into the L1A_STOP state.
- CCB_BC0 – if preceded with the CCB_L1STT command, starts the Bunch counter from its offset value, as determined by the CSR_BCO register; otherwise serves as a timing mark to verify the Bunch counter synchronization to the control timing.

The current state of the SP02 logic can be monitored with four fast monitoring status signals: busy (FM_BSY), ready (FM_RDY), warning-of-overflow (FM_WOF), and out-of-synch (FM_OSY). Each SP02 FPGA reports its 4-bit status to the VME_FPGA. The VME_FPGA is capable of masking individual statuses when providing the SP02 overall status to the RJ45 connector and front panel indicators (LEDs).

For the summary of fast monitoring statuses see details into the CSR_BSY – Busy Control/Status, CSR_RDY – Ready Control/Status, CSR_WOF – Warning-of-OverFlow Control/Status, and CSR_OSY – Out-of-Synch Control / Status sections below.

Table 3: SP02 LED Panel

Description	Left LED Name	Left LED Color	Right LED Color	Right LED Name	Description
Busy	BSY	Red	Green	5.0V_OK	5.0V power is OK
Ready	RDY	Green	Green	3.3V_OK	3.3V power is OK
Warning-of-OverFlow	WOF	Red	Green	2.5V_OK	2.5V power is OK
Out-of-Synch	OSY	Red	Green	1.5V_OK	1.5V power is OK
Local Charged Trigger	LCT	Yellow	Yellow	L1ACC	L1 Accept

The LED indicators are located above the F5 link transceivers. The BSY, RDY, WOF, and OSY indicators display status of the corresponding signal lines. Power OK indicators are off, since the power-monitoring chip MAX6338BUB is missing on the board. The L1ACC LED blinks for 25 ms on every CCB_L1ACC. The LCT blinks for 25 ms on every LCT found by the SP_FPGA. Just temporarily, the power OK indicators visualize the L1 Accept FSM states:

- 2.5V_OK => FSM is in L1_STOP state;
- 3.3V_OK => FSM is in L1_WAIT state;
- 5.0V_OK => FSM is in L1_RUN state.

VME Interface

The SP02 card includes two A24D16 Slave interfaces [ii] implemented in VME_FPGA and CPLD_FPGA accordingly. Table 4 shows all address modifiers, the SP02 responds to during the VME Data Transfer Bus (DTB) cycles.

Table 4: SP02 Address Modifier Codes.

AM	AM Description	Access Description	Interface Chip
39	A24 non privileged data access	Access to all locations, except the BLT Mapping Registers	VME_FPGA
3A	A24 non privileged program access	Access to the BLT Mapping Registers	
3B	A24 non privileged block transfer (BLT)	BLT access using the BLT Mapping Registers	
3D	A24 supervisory data access		VME_CPLD
3E	A24 supervisory program access		
3F	A24 supervisory block transfer (BLT)		

Auxiliary VME Interface

The auxiliary VME_CPLD interface is intended for board configuration and provides access solely for the Bus Scan Controller (BSC). The BSC drives three chains of JTAG-compatible devices, see Table 5:

- Chain 0 consists of the MAIN_FPGA and its EEPROMs;
- Chain 1 includes the VME_FPGA with EEPROM, the FRONT_FPGAs with EEPROMs, and the DDU_FPGA with EEPROM;
- Chain 2 connects 45 SRAMs.

Table 5: SP02 Configuration Chains.

Chain No	Device No	Device Name	Device Type	Device ID Code	Bypass Switch
0	1	SP_EEPROM_1	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW2
0	2	SP_EEPROM_2	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW3
0	3	SP_EEPROM_3	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW4
0	4	SP_EEPROM_4	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW5
0	5	SP_EEPROM_5	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	MC_SW6
0	6	SP_FPGA	XC2V4000-5FF1152C	VVVV 0001 0000 0101 0000 0000 1001 0011	MC_SW1
1	1	VME_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW4
1	2	VME_FPGA	XC2V1000-5FG456C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW5
1	3	FF5_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW2
1	4	FRONT_FPGA_5	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW3
1	5	FF4_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW14
1	6	FRONT_FPGA_4	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW15
1	7	FF3_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW19
1	8	FRONT_FPGA_3	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW20
1	9	DDU_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW10
1	10	DDU_FPGA	XC2V1000-5FG456C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW11
1	11	FF2_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW12
1	12	FRONT_FPGA_2	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW13
1	13	FF1_EEPROM	XC18V04VQ44C	VVVV 0101 0000 0010 0110 0000 1001 0011	SW17
1	14	FRONT_FPGA_1	XC2V1000-5FF896C	VVVV 0001 0000 0010 1000 0000 1001 0011	SW18

Chain No	Device No	Device Name	Device Type	Device ID Code	Bypass Switch
2	1	ME4C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	2	ME4C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	3	ME4C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	4	ME4B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	5	ME4B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW7
2	6	ME4B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	7	ME4A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	8	ME4A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	9	ME4A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	10	ME3C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	11	ME3C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	12	ME3C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	13	ME3B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	14	ME3B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW9
2	15	ME3B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	16	ME3A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	17	ME3A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	18	ME3A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	19	ME2C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	20	ME2C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	21	ME2C_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	22	ME2B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	23	ME2B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW8
2	24	ME2B_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	25	ME2A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	26	ME2A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	27	ME2A_GP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	28	ME1F_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	29	ME1F_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	30	ME1F_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	31	ME1E_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	32	ME1E_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW6
2	33	ME1E_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	34	ME1D_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	35	ME1D_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	36	ME1D_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	37	ME1C_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	38	ME1C_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	39	ME1C_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	40	ME1B_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	41	ME1B_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	SW16
2	42	ME1B_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	
2	43	ME1A_LP	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	44	ME1A_GE	GS881Z18AT	1VVV 0000 0000 0000 1010 0001 1011 0011	
2	45	ME1A_GP	GS8161Z36AT	VVVV 0000 0000 0000 1000 0001 1011 0011	

Alex M. is to determine the VME address mapping for the auxiliary VME interface.

Main VME Interface

A24 Non Privileged Data Access

An A24 non privileged data access (AM=0x39) to the main VME_FPGA interface utilizes a 5-bit geographical addressing scheme [ii] and provides for the VME Data Transfer Bus (DTB) multicast ***write*** cycles by partitioning the address space into the following fields, see Table 6.

Table 6: Address Format for Non Privileged Data Access

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA					CA							0	MA		RA							0	0

Here:

- 0 – Zero value address line;
- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- CA – Chip Address. Positional coding provides simultaneous write access to any combination of SP02 FPGAs (except VME_FPGA), see Table 7;
- MA – Muon Address. Each FRONT_FPGA processes data for 3 muons, and the SP_FPGA services 3 PT LUTs. A 2-bit MA field provides write access either to a single muon-related register or to all three such registers simultaneously, see Table 8 for details.
- RA – Register Address inside FPGA(s). There are 4 groups of registers in total, see Table 9 for details:
    - Action Register Group. Writing to these write-only registers causes pulses, like reset or test pulse, to be generated and/or operations, like start or stop L1ACC processing, to be performed.
    - Control/Status Register Group. These registers carry 2 groups of bits: read-only status bits to monitor, and read/write bits to control behavior of the SP02 logic.
    - Address Register Group. These registers provide access to LUT and Eta Window address counters.
    - Data Register Group. The group provides access to LUT , Eta Window and FIFO data inputs/outputs.

Full Address (FA) of the register is defined as:
FA = (SA << 19) + (CA << 12) + (MA << 9) + (RA << 2).

Table 7: Chip Address Field Format for Non Privileged Data Access

Chip	CA, binary	Description
VM	000_0000	VME_FPGA Access
F1	000_0001	FRONT_FPGA_1 Access
F2	000_0010	FRONT_FPGA_2 Access
F3	000_0100	FRONT_FPGA_3 Access
F4	000_1000	FRONT_FPGA_4 Access
F5	001_0000	FRONT_FPGA_5 Access
DD	010_0000	DDU_FPGA Access
SP	100_0000	SP_FPGA Access

Table 8: Muon Address Field Format for Non Privileged Data Access

Label	Muon in FPGA	MA, binary	Description
MA	ALL	00	Access to all three muon-related registers
M1	A/D/1	01	Access to a First (A or D or 1) muon-related register
M2	B/F/2	10	Access to a Second (B or E or 2) muon-related register
M3	C/E/3	11	Access to a Third (C or F or 3) muon-related register

Note, that only ***write*** access is defined to a group of registers, while ***read*** access may only be executed to a single register at any time.

Table 9: Register Address Field Format for Non Privileged Data Access

RA, hex	Register Label	Description	Destination / Valid MA				Page
			SP	DD	Fx	VM	
Action Register Group							
0x00	ACT_HR	Hard Resets	-	-	-	MA	13
0x01	ACT_CMR	Clock Managers Resets	MA	MA	MA	MA	14
0x02	ACT_LCR	Link Counters Resets	-	MA	MA/M1/M2/M3	-	14
0x03	ACT_XFR	FIFOs Resets	MA	MA	MA	-	15
0x04	ACT_ACR	Address Counters Resets	MA	-	MA	-	15
0x05	ACT_FCC	Fast Control Command	-	-	-	MA	16
Control/Status Register Group							
0x10	STS_CCB	Fast Control Status	-	-	MA	-	16
0x11	STS_ANA	CCB Logic Analyzer				MA	17
0x1F	CSR_SID	SP Core ID	MA	-	-	-	17
0x20	CSR_CID	Chip ID	MA	MA	MA	MA	17
0x22	CSR_CM1	Clock Manager_1 Control/Status	MA	MA	MA	MA	18
0x23	CSR_CM2	Clock Manager_2 Control/Status	MA	MA	MA	MA	18
0x24	CSR_HR	Hard Reset Mask	-	-	-	MA	19
0x25	CSR_CFG	Configuration Done Status	-	-	-	MA	19
0x26	CSR_INI	Init Status	-	-	-	MA	19
0x28	CSR_BSY	Busy Mask/Status		-	-	MA	20
0x29	CSR_RDY	Ready Mask/Status		-	-	MA	20
0x2A	CSR_WOF	WarningOfOverflow Mask/Status	TBD	TBD	TBD	MA	21
0x2B	CSR_OSY	OutOfSynch Mask/Status	TBD	TBD	MA/M1/M2/M3	MA	21
0x2D	CSR_FCC	Fast Control Configuration/Status	TBD	TBD	MA	MA	22

RA, hex	Register Label	Description	Destination / Valid MA				Page
			SP	DD	Fx	VM	
0x30	CSR_LEC	Link Error Counters		MA	M1/M2/M3	-	23
0x31	CSR_AF	Alignment FIFO Status	TBD	-	M1/M2/M3	-	23
0x32	CSR_TF	Test FIFO Status	M1/M2/M3	MA	M1/M2/M3	-	24
0x33	CSR_SF	Spy FIFO Status	M1/M2/M3	MA	M1/M2/M3	-	24
0x34	CSR_PF	Pipeline FIFO Status	TBD	-	MA	-	24
0x35	CSR_DF	DAQ FIFO Status	TBD	MA	MA	-	25
0x36	CSR_BF	Barrel FIFO Status	TBD	-	-	-	-
0x37	CSR_LF	L1 FIFO Status	TBD	TBD	MA	-	25
0x38	CSR_RBW	Ring Buffer Write Pointer	TBD	-	MA	-	25
0x39	CSR_RBR	Ring Buffer Read Pointer	TBD	-	MA	-	26
0x3A	CSR_SF1	F1 Spy FIFO Status	M1/M2/M3	-	-	-	26
0x3B	CSR_SF2	F2 Spy FIFO Status	M1/M2/M3	-	-	-	26
0x3C	CSR_SF3	F3 Spy FIFO Status	M1/M2/M3	-	-	-	27
0x3D	CSR_SF4	F4 Spy FIFO Status	M1/M2/M3	-	-	-	27
0x3E	CSR_SF5	F5 Spy FIFO Status	M1/M2/M3	-	-	-	27
0x3F	CSR_SFE	EMU Spy FIFO Status	MA	-	-	-	28
0x40	CSR_LNK	Link Control/Status	-	MA	MA/M1/M2/M3	-	28
0x41	CSR_AFD	Alignment FIFO Read Delay	-	-	MA	-	29
0x42	CSR_TFC	Test FIFO Configuration	MA	TBD	MA	-	29
0x43	CSR_SFC	Spy FIFO Configuration	MA	MA	MA	MA	31
0x44	CSR_PFD	Pipeline FIFO Read Delay	MA	-	MA	-	32
0x45	CSR_DFC	DAQ FIFO Configuration	MA	MA	MA	-	32
0x46	CSR_SCC	SP Core Configuration	MA	-	-	-	32
0X47	CSR_TFB	Barrel Test FIFO Status	M1/M2	-	-	-	-
0x48	CSR_SFB	Barrel Spy FIFO Status	M1/M2	-	-	-	-
0x49	CSR_SFM	Muon Sorter Spy FIFO Status	M1/M2/M3	-	-	-	33
0x4A	CSR_TF1	F1 Test FIFO Status	M1/M2/M3	-	-	-	33
0x4B	CSR_TF2	F2 Test FIFO Status	M1/M2/M3	-	-	-	33
0x4C	CSR_TF3	F3 Test FIFO Status	M1/M2/M3	-	-	-	34
0x4D	CSR_TF4	F4 Test FIFO Status	M1/M2/M3	-	-	-	34
0x4E	CSR_TF5	F5 Test FIFO Status	M1/M2/M3	-	-	-	34
0x4F	CSR_TFE	EMU Test FIFO Status	MA	-	-	-	35
Address Counter Group							
0x50	CNT_LPL	Local Phi LUT Address Low	-	-	MA	-	35
0x51	CNT_LPH	Local Phi LUT Address High	-	-	MA	-	36
0x52	CNT_GLL	Global_Eta/Phi/DT LUT Address Low	-	-	MA	-	36
0x53	CNT_GLH	Global_Eta/Phi/DT LUT Address High	-	-	MA	-	37
0x56	CNT_PTL	PT LUT Address Low	MA	-	-	-	37
0x57	CNT_PTH	PT LUT Address High	MA	-	-	-	37
0x58	CNT_ETA	Eta Address	MA	-	-	-	37

RA, hex	Register Label	Description	Destination / Valid MA				Page
			SP	DD	Fx	VM	
Data Register Group							
0x5A	DAT_TF1	F1 Test FIFO Data	M1/M2/M3	-	-	-	38
0x5B	DAT_TF2	F2 Test FIFO Data	M1/M2/M3	-	-	-	38
0x5C	DAT_TF3	F3 Test FIFO Data	M1/M2/M3	-	-	-	38
0x5D	DAT_TF4	F4 Test FIFO Data	M1/M2/M3	-	-	-	39
0x5E	DAT_TF5	F5 Test FIFO Data	M1/M2/M3	-	-	-	39
0x5F	DAT_TFE	EMU Test FIFO Data	MA	-	-	-	40
0x60	DAT_LP	Local Phi LUT Data	-	-	MA/M1/M2/M3	-	40
0x62	DAT_GP	Global Phi LUT Data	-	-	MA/M1/M2/M3	-	40
0x63	DAT_DT	DT LUT Data	-	-	MA/M1/M2/M3	-	41
0x64	DAT_GE	Global Eta LUT Data	-	-	MA/M1/M2/M3	-	41
0x66	DAT_PT	PT LUT Data	MA/M1/M2/M3	-	-	-	42
0x68	DAT_ETA	Eta Data	MA	-	-	-	42
0x69	DAT_VPC	Valid Pattern Counter Data	M1/M2/M3	-	M1/M2/M3	-	43
0x6A	DAT_SF1	F1 Spy FIFO Data	M1/M2/M3	-	-	-	43
0x6B	DAT_SF2	F2 Spy FIFO Data	M1/M2/M3	-	-	-	44
0x6C	DAT_SF3	F3 Spy FIFO Data	M1/M2/M3	-	-	-	44
0x6D	DAT_SF4	F4 Spy FIFO Data	M1/M2/M3	-	-	-	44
0x6E	DAT_SF5	F5 Spy FIFO Data	M1/M2/M3	-	-	-	45
0x6F	DAT_SFE	EMU Spy FIFO Data	MA	-	-	-	45
0x72	DAT_TF	Test FIFO Data	MA/M1/M2/M3	MA	MA/M1/M2/M3	-	46
0x73	DAT_SF	Spy FIFO Data	M1/M2/M3	MA	M1/M2/M3	-	47
0x75	DAT_DF	DAQ FIFO Data	MA	MA	MA	-	48
0x76	DAT_TFB	Barrel Test FIFO Data	MA/M1/M2	-	-	-	-
0x77	DAT_SFB	Barrel Spy FIFO Data	M1/M2	-	-	-	-
0x78	DAT_SFM	Muon Sorter Spy FIFO Data	M1/M2/M3	-	-	-	49
0x7F	DAT_RW	Read / Write Data	MA	MA	MA	MA	49

The main VME_FPGA interface distributes VME control all over the board via the Internal Data Transfer Bus (IDTB). IDTB is a synchronous parallel bus that is used by the VME_FPGA to transfer data to or from other SP02 FPGA(s): SP_FPGA, 5 FRONT_FPGAs, and DDU_FPGA.

The IDTB bus lines are grouped into 4 categories:

- Address Lines: A[11:2] see Table 10;
- Data Lines: D[15:0] Bi-directional;
- Control Lines: /CS[7:1] Chip Select, active LOW;
  /ACK[7:1] Acknowledge, active LOW;
  /WR Write, active LOW;
- Auxiliary Lines: VMB_WR Buffer Write;
  VMB_/OE Buffer Output Enable, active LOW.

Table 10: IDTB Address Format

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2
RV	MA		RA						
RV	IA								

- IA – Internal DTB Address, defines storage location inside FPGA

- RV – Reserved line

To prevent data lines from being too long they are split into two segments: the SP segment and the FRONT/DDU segment, with bi-directional buffers in between. The SP segment connects directly to the VME_FPGA pins. The FRONT/DDU segment is located behind the buffers. Two auxiliary lines: Buffer Write (data direction) and Buffer Output Enable, - are used to control data flow through the buffers.

The IDTB transfer is a sequence of level states on the signal lines that results in the transfer of an address and two bytes of data between the VME_FPGA and other SP02 FPGA(s).

Each IDTB cycle is an inherent part of the backplane DTB cycle, when DTB addresses FPGA(s), other than VME_FPGA. Chip Select (/CS) plays role of the DS* strobe and Acknowledge (/ACK) plays role of the DTACK*. The major difference between backplane DTB and IDTB is that IDTB is a synchronous bus, i.e. both /CS and /ACK handshake signals should be asserted on the rising edge of the system clock at source, and sensed with the next rising edge of the system clock at destination.

The VME_FPGA initiates two types of IDTB cycles:

- **IDTB Write cycle** transfers data from the VME_FPGA to one or more destination FPGA(s). The cycle begins when the VME_FPGA sets address, data, Write and optionally Buffer Write and Buffer Output Enable on the corresponding lines and issues one or more Chip Selects. Selected FPGA(s) captures the address and checks to see if it is to respond to the cycle. If so, sensing Write in a LOW state, it stores the data and acknowledges the transfer. The VME_FPGA then terminates the cycle.
- **IDTB Read cycle** transfers data from the source FPGA to the VME_FPGA. The cycle begins when the VME_FPGA sets address and optionally a Buffer Output Enable and issues a Chip Select. Selected FPGA captures and the address and checks to see if it is to respond to the cycle. If so, sensing Write in a HIGH state, it retrieves the data from the corresponding storage, places it on the data lines and acknowledges the transfer. The VME_FPGA then terminates the cycle.

Normally the VME_FPGA would terminate the DTB transfer with the Data Transfer Acknowledge (DTACK*) asserted low. If during the DTB cycle the addressable SP02 detects that the VME Master either addresses a non-existed location, or tries to write to a read-only location, the VME_FPGA terminates the cycle with a Bus Error (BERR*) asserted low. The VME_FPGA is not aware of the DTB outcome, when it passed the DTB cycle to the IDTB. If the expected IDTB Acknowledge(s) is (are) not received after a time-out period has expired, the VME_FPGA terminates the cycle driving BERR* low. The VME_FPGA time-out period is set to 8 system clocks.

A24 Non Privileged Program Access

An A24 non privileged program access (AM=0x3A) is used to load four mapping locations in the VME FPGA, see Table 11 for valid address fields

Table 11: Address Format for Non Privileged Program Access

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA					X													PA				0	0

Here:

- X – Don't care bit;
- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- PA – Program Address, defines 16 register locations in the non privileged program space, see Table 12 for valid addresses.

Table 12: Register Address Field Format for Non Privileged Program Access

PA, hex	Register Label	Description
BLT Mapping Control/Status Register Group		
0x0		
0x1	CPA_BF1	BLT Mapping FIFO_1 Control/Status
0x2	CPA_BF2	BLT Mapping FIFO_2 Control/Status
0x3	CPA_BF3	BLT Mapping FIFO_3 Control/Status
0x4		Reserved
0x5		Reserved
0x6		Reserved
0x7		Reserved
BLT Mapping Data Register Group		
0x8	DPA_BLT	BLT Mapping Data
0x9	DPA_BF1	BLT Mapping FIFO_1 Data
0xA	DPA_BF2	BLT Mapping FIFO_2 Data
0xB	DPA_BF3	BLT Mapping FIFO_3 Data
0xC		Reserved
0xD		Reserved
0xE		Reserved
0xF		Reserved

Details on the above registers can be found in the Register Detail section under the register labels. During BLT transfers, mapping registers substitute the DTB address with a 16-bit address, used to access storage location(s) in the non privileged data space. The format of the mapping data/address is shown below:

Table 13: BLT Mapping Location Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CA							MA		RA						

Here CA, MA, and RA are address fields, described in the A24 Non Privileged Data Access section above.

A24 Non Privileged Block Transfer (BLT)

Any storage location, accessible via the A24 Non Privileged Data Access, can also be accessed via an A24 non privileged block transfer (BLT), when AM=0x3B. The BLT, prior to executing, should be initialized by loading a mapping location with one or more destination addresses. The BLT mapping locations are listed in Table 12. During the BLT DTB cycle the VME_FPGA, depending on the value in the BA field, uses one of the preloaded mapping

locations to substitute the current DTB address with the address stored in the mapping location, see Table 14. Table 13 shows the BLT mapping location data format and Table 15 lists 4 128Kbyte windows for block transfers.

Table 14: Address Format for Non Privileged Block Transfers

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
SA					BA		X																0

Here:

- SA – Slot Address, could be either Slot Geographical Address (GA), or Slot Multicast Address (30);
- BA – BLT Address. Defines one out of four BLT Mapping locations inside the VME_FPGA to substitute the current VMA backplane address with the preloaded one;
- X – Don't care bit.

Table 15: BLT Address Field Format for Non Privileged Block Transfers

BA, binary	Register Name	First D16 Transfer Address, hex	Last D16 Transfer Address, hex	Address Space
00	BLT Mapping Register	0x00000	0x1FFFE	64 Kwords = 128 Kbytes
01	BLT Mapping FIFO_1	0x20000	0x3FFFE	64 Kwords = 128 Kbytes
10	BLT Mapping FIFO_2	0x40000	0x5FFFE	64 Kwords = 128 Kbytes
11	BLT Mapping FIFO_3	0x60000	0x7FFFE	64 Kwords = 128 Kbytes

Register Detail

Action Register Group

ACT_HR – FPGA Hard Reset Register

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 400 ns Hard Reset pulse to the selected FPGA(s) onboard. Hard Reset is applied to the /PROG_B pin of the corresponding FPGA. A VME-generated Hard Reset is ORed with a CCB backplane hard reset. This register address is applicable to the VME_FPGA only.

Sensing a hard reset on its input, the FPGA reloads its configuration from the associated configuration EPROM. The user may use the ACT_HR transfer cycle to verify chip presence on the board. To make sure all FPGA chips are present on the board, the CSR_CFG read transfer cycle should be executed twice after the ACT_HR: first time when chips are engaged in the configuration process and second time after a 5 sec pause, when the configuration is definitely completed. If there is a missing FPGA chip on the board (a mezzanine card is not installed, for example) then the corresponding Configuration Done line remains floating, and can be sensed by the VME_FPGA as being either in HIGH (Logic ONE) or LOW (Logic ZERO) state. But in any case, Configuration Done line for a missing chip would retain its state, while the one for a successfully configured FPGA will be LOW on the first read and HIGH on the second read. See Table 32 for chip mapping.

Table 16: ACT_HR Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	SPHR	DDHR	F5HR	F4HR	F3HR	F2HR	F1HR	X

Here:

- X – Don't care bit;
- F1HR – FRONT_FPGA_1 Hard Reset;
- F2HR – FRONT_FPGA_2 Hard Reset;
- F3HR – FRONT_FPGA_3 Hard Reset;
- F4HR – FRONT_FPGA_4 Hard Reset;
- F5HR – FRONT_FPGA_5 Hard Reset;
- DDHR – DDU_FPGA Hard Reset;
- SPHR - SP_FPGA Hard Reset.

ACT_CMR – Clock Manager Reset

Writing Logic ONE to specified bit(s) of this write-only register results in sending 50 ns reset pulse(s) to selected DCM(s). Reset pulse resets also DCM error counters described under CSR_CM1 – System Clock Manager 1 Status and CSR_CM2 – System Clock Manager 2 Status headings. The register address is applicable to all FPGAs.

Table 17: ACT_CMR Data Format for VM_FPGA, FRONT_FPGA, DDU_FPGA, and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	CMR2	CMR1	X

Here:

- X – Don't care bit;
- CMR1 – Clock Manager 1 Reset;
- CMR2 – Clock Manager 2 Reset.

ACT_LCR – Link Counters Resets

Writing Logic ONE to specified bit(s) of this write-only register results in sending 25 ns reset pulse(s) to selected error counter(s) described under the CSR_LNK, CSR_LEC and DAT_VPC headings. The register address is applicable to the FRONT_FPGA and to the SP_FPGA.

Table 18: ACT_LCR Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	VPR	TER	SLR	CER	EWR

Here:

- X – Don't care bit;
- EWR – TLK2501 Error Word Counter Reset in the CSR_LEC register (RXDV == HIGH, RXER == HIGH);
- CER – TLK2501 Carrier Extend Counter Reset in the CSR_LEC register (RXDV == LOW, RXER == HIGH);
- SLR – FINISAR optical receiver Signal Loss Counter Reset in the CSR_LEC register (RXSD goes LOW);

- TER – PRBS Test Error Counter Reset in the CSR_LNK register;
- VPR – Valid Pattern Counter Reset in the DAT_VPC register.

Table 19: ACT_LCR Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	VPR	X	X	X	X

Here:

- X – Don't care bit;
- VPR – Valid Pattern Counter Reset in the DAT_VPC register.

ACT_XFR – FIFO Resets

Writing Logic ONE to a specified bit of this write-only register results in sending a 25 ns reset pulse to corresponding FIFO(s). The register address is applicable to the FRONT_FPGA, DDU_FPGA, and SP_FPGA.

Table 20: ACT_XFR Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	BFR	DFR	PFR	SFR	TFR	X

Here:

- X – Don't care bit;
- TFR – All Test FIFOs Reset (Init);
- SFR – All Spy FIFOs Reset (Init);
- PFR – Pipeline FIFO Reset (Init);
- DFR – DAQ FIFO Reset (Init). It also resets L1 Accept FIFO, ring buffer read/write pointers, and event builder FSM;
- BFR – Barrel FIFO Reset;

Table 21: ACT_XFR Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	BFR	DFR	PFR	SFR	TFR	X

Here:

- X – Don't care bit;
- TFR – All Test FIFOs Reset (Init);
- SFR – All Spy FIFOs Reset (Init);
- PFR – Pipeline FIFO Reset (Init);
- DFR – DAQ FIFO Reset (Init). It also resets L1 Accept FIFO, ring buffer read/write pointers, and event builder FSM;
- BFR – Barrel FIFO Reset;

ACT_ACR – Address Counters Reset(s)

Writing Logic ONE to specified bit(s) of this write-only register results in sending a 25 ns reset pulse to a corresponding address counter. The register address is applicable to FRONT_FPGA and SP_FPGA.

Table 22: ACT_ACR Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	GLR	LPR

Here:

- X – Don't care bit;
- LPR – Local Phi LUT Address Counter Reset;
- GLR – Global Phi/Eta/DT LUT Address Counter Reset.

Table 23: ACT_ACR Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	ETR	PTR	X	X

Here:

- X – Don't care bit;
- PTR – PT LUT Address Counter Reset;
- ETR – Eta Min/Max/Window Address Counter Reset.

ACT_FCC – Fast Control Command

VME write cycle to this write-only register is equivalent to getting the same fast control command from the CCB over the backplane. The difference is that the CCB commands are available to all modules in the crate, while this command affects only the addressable SP02. Note, that ACT_FCC commands are enabled only when the CSR_FCM register is configured to a local fast control mode.

Table 24: ACT_FCC Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L1A	X	X	X	X	X	X	X	FCC7	FCC6	FCC5	FCC4	FCC3	FCC2	FCC1	FCC0

Here:

- X – Don't care bit;
- FCC[7:0] – The Fast Control Command,
  the data format matches the TTC $C4 register and the CCB CSR2 register formats;
- L1A – L1Accept Command.

Control/Status Register Group

STS_CCB – Fast Control Command bus Status.

This read-only register returns current state of the SP02 internal Fast Control Command bus. The register address is valid for the FRONT_FPGA. The current bus state should always be zero, if there no shorts on the board. See the CCB Interface section for a list of Fast Control Commands.

Table 25: STS_CCB Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	FCC4	FCC3	FCC2	FCC1	FCC0	0	0	0	FCP4	FCP3	FCP2	FCP1	FCP0
			Current FC State								Previous FC Command				

Here:

- FCC [4:0] – current state of the Fast Control Command bus;

– FCP [4:0] – previous Fast Control Bus Command;

STS_ANA – CCB Analyzer

This analyzer allows to record timing of the CCB command strobe with respect to the SP02 system clock, as well as the CCB command itself. The SP02 system clock is a deskewed CCB_CLK that drives every SP02 FPGA chip. The contents of the analyzer is reset on power-up and on any write command (data value is irrelevant) to this register. After reset, it starts recording non-zero data, if the SP02 is under the CCB fast control; see the CSR_FCC register description on how to set the SP02 under the CCB control. Read command returns recorded data in the format shown below. The analyzer keeps up to 64 data words. If the analyzer is empty, the read command returns bus error to the VME Master. Typical position of the CCB2001 command strobe is shown below:

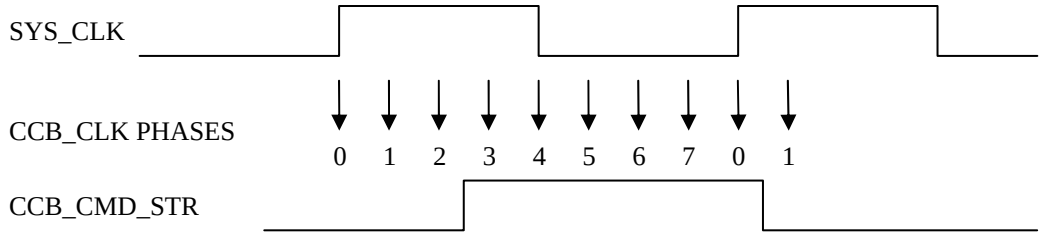

Figure 2: CCB2001 Command Strobe typical position

Table 26: STS_ANA Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
CSTR7	CSTR6	CSTR5	CSTR4	CSTR3	CSTR2	CSTR1	CSTR0	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	ECRES	BCRES
CCB Command Strobe								CCB command							

Here:

– CSTR[7:0] – CCB command strobe registered by eight different phases of the CCB_CLK clock (7/8, 6/8, 5/8, 4/8, 3/8, 2/8, 1/8, and 0/8 of the CCB_CLK period);
– CMD [7:2] –CCB command code;
– ECRES – Event Counter Reset;
– BCRES – Bunch Counter Reset.

CSR_SID – SP Core ID Register

This SP_FPGA read-only register keeps an SP core code release date in the following format:

Table 27: CSR_SID Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
YY				MM				1	1	1	DD				

Here:

– DD – Day Code (01…31);
– MM – Month Code (01…12);
– YY – Year Code (00…15) = Year - 2000.

CSR_CID – Chip ID Register

This read-only register keeps a firmware release date in the format shown in the table below. Register address is applicable to all FPGAs.

Table 28: CSR_CID Data Format for all FPGAs

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
YY				MM				NN			DD				

Here:

- DD – Day Code (01…31);
- NN – FPGA Number (0...7), which corresponds to 8 FPGA chips, numbered in the following order: VM, F1, F2, F3, F4, F5, DD, SP;
- MM – Month Code (01…12);
- YY – Year Code (00…15) = Year - 2000.

CSR_CM1 – System Clock Manager 1 Status

This read-only register keeps history of Digital Clock Manager 1 behavior after the last ACT_CMR command. Its default value is 0x0004, which means that all enabled DCM1 features locked and there were no errors since last reset. DCM1 is a DCM with internal feedback, distributing the 40.078 MHz system clock in the chip.

Table 29: CSR_CM1 Data Format for all FPGAs

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LCK1 Counter				CST1 Counter				0	0	0	0	0	LCK1	CST1	PSO1

Here:

- PSO1 – Phase Shift Overflow, should be LOW for normal operation;
- CST1 – Input Clock Stopped Toggling;
- CST1 Counter – “loss of input clock” counter. It counts number of “CST1 go HIGH” after last DCM1 reset. The counter stops when it reaches its maximum value of 15;
- LCK1 – All enabled DCM features locked;
- LCK1 Counter – “loss of lock” counter. It counts number of “LCK1 go LOW” after last DCM1 reset. The counter stops when it reaches its maximum value of 15.

CSR_CM2 – System Clock Manager 2 Status

This read-only register keeps history of Digital Clock Manager 2 behavior after the last ACT_CMR command. Its default value is 0x0004, which means that all enabled DCM2 features locked and there were no errors since last reset. For the VME_FPGA, DCM2 is a DCM with external feedback, distributing system clock all over the board. For the FRONT_FPGA, DDU_FPGA and SP_FPGA, the DCM2 distributes the 80.156 MHz clock in the chip.

Table 30: CSR_CM2 Data Format for all FPGAs

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LCK2 Counter				CST2 Counter				0	0	0	0	0	LCK2	CST2	PSO2

Here:

- PSO2 – Phase Shift Overflow, should be LOW for normal operation;
- CST2 – Input Clock Stopped Toggling;

- CST2 Counter – "loss of input clock" counter. It counts number of "CST2 go HIGH" after last DCM2 reset. The counter stops when it reaches its maximum value of 15;
- LCK2 – All enabled DCM features locked;
- LCK2 Counter – "lost of lock" counter. It counts number of "LCK2 go LOW" after last DCM2 reset. The counter stops when it reaches its maximum value of 15.

CSR_HR – Hard Reset Mask

In the VME_FPGA the CSR_HR register masks the CCB Hard Reset signal. By default the CCB hard reset is disabled for all SP02 chips.

Table 31: CSR_HR Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	HRM7	HRM6	HRM5	HRM4	HRM3	HRM2	HRM1	X

Here:

- X – Don't care bit, reads back as zero;
- HRM [7:1] = 0x00 (default) – Hard Reset mask for SP, DD, F5…F1 chips.

CSR_CFG – FPGA Configuration Done Status

Addressing to this read-only register allows verifying the Configuration Done status of the FRONT_FPGAs, DDU_FPGA, and SP_FPGA after hard resets. The register address is applicable to the VME_FPGA only. Register's default value is 0xFE, when all chips, including the mezzanine card's chip, are in place. Being Low during configuration, Configuration Done High indicates completion of the configuration.

To make sure all FPGA chips are present on board, the CSR_CFG command should be executed twice: first, when chips are engaged in the configuration process, i.e. immediately after the ACT_HR command, and second, after a 5 sec pause, when the configuration is definitely completed. If there is a missing FPGA chip on board (a mezzanine card not installed, for example), then the corresponding Configuration Done line remains floating, and could be sensed by the VME_FPGA either as a logic ONE or logic ZERO. But in any case, Configuration Done line for a missing chip would retain its state, while the one for a successfully configured FPGA will be LOW on the first read and HIGH on the second read.

Table 32: CSR_CFG Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	CFG7	CFG6	CFG5	CFG4	CFG3	CFG2	CFG1	0
								Configuration Done Status							

Here:

- CFG [7:1] = 0xFE (default) – Configuration Done Status bits for the SP, DD, F5, F4, F3, F2, and F1 FPGAs accordingly.

CSR_INI – FPGA Init Status

Addressing to this read-only register allows verifying the INIT_B pin status of the FRONT_FPGAs, DDU_FPGA, and SP_FPGA after hard resets. The register address is applicable to the VME_FPGA only. The default register value is 0xFE. INIT_B Low indicates

memory is being cleared. The INIT_B pin transitions HIGH when the clearing of configuration memory is complete. INIT_B LOW during configuration indicates an error.

Table 33: CSR_INI Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	INI7	INI6	INI5	INI4	INI3	INI2	INI1	0
								Init_B Status							

Here:

- INI [7:1] = 0xFE (default) – Init_B Status bits for the SP, DD, F5, F4, F3, F2, and F1 FPGAs accordingly.

CSR_BSY – Busy Control/Status

In the VME_FPGA the CSR_BSY register displays status of seven input and one output BSY lines. Besides, it carries eight mask bits, so each input or/and the VME_FPGA output can be either disabled or enabled:

BSY0 = (BSY1*BSC1 + BSY2*BSC2 + BSY3*BSC3 + BSY4*BSC4 + BSY5*BSC5 + BSY6*BSC6 + BSY7 *BSC7 + BSY0_INT) * BSC0

Indexes 0…7 stand for chip numbers; see Table 7 and/or Table 28 for chip numbering scheme, and BSY0_INT is an internal busy status o the VME_FPGA, which is "1" when counting of CCB_L1ACCs is stopped (disabled).

The FRONT_FPGA sets BSY to "1", when either the Bunch counter carries 0xFFF=4095 value, or link resynch on CCB_L1RES failed (the AF word count remains zero).

Table 34: CSR_BSY Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
BSM7	BSM6	BSM5	BSM4	BSM3	BSM2	BSM1	BSM0	BSY7	BSY6	BSY5	BSY4	BSY3	BSY2	BSY1	BSY0	R
BSM7	BSM6	BSM5	BSM4	BSM3	BSM2	BSM1	BSM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- BSM [7:0] – Busy Chip mask for SP, DD, F5…F1, and VM chips;
- BSY [7:0] – Busy status for SP, DD, F5…F1, and VM chips.

CSR_RDY – Ready Control/Status

In the VME_FPGA the CSR_RDY register displays status of seven input and one output RDY lines. Besides, it carries eight mask bits, so each input or/and VME_FPGA output can be either disabled or enabled:

RDY0 = (RDY1*RDM1 + RDY2*RDM2 + RDY3*RDM3 + RDY4*RDM4 + RDY5*RDM5 + RDY6*RDM6 + RDY7 *RDM7) * RDY0_INT *RDM0

Indexes 0…7 stand for chip numbers; see Table 7 and/or Table 28 for chip numbering scheme, and RDY0_INT is an internal ready status of the VME_FPGA, which is "1" when passing of CCB_L1ACCs to the FC bus is enabled.

The FRONT_FPGA sets RDY to "1", when link resynchronization initiated by CCB_L1RES completed a success (the Alignment FIFO is neither empty, nor full). Only links with enabled TLK2501 receivers contribute to the chip's RDY status; see the CSR_LNK register for a DVEN bit description.

Table 35: CSR_RDY Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
RDM7	RDM6	RDM5	RDM4	RDM3	RDM2	RDM1	RDM0	RDY7	RDY6	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	R
RDM7	RDM6	RDM5	RDM4	RDM3	RDM2	RDM1	RDM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- RDM [7:0] – Ready Chip mask for SP, DD, F5…F1, and VM chips;
- RDY [7:0] – Ready status for SP, DD, F5…F1, and VM chips.

CSR_WOF – Warning-of-OverFlow Control/Status

In the VME_FPGA the CSR_WOF register displays status of seven input and one output WOF lines. Besides, it carries eight mask bits, so each input or/and VME_FPGA output can be either disabled or enabled:

WOF0 = (WOF1*WOM1 + WOF2*WOM2 + WOF3*WOM3 + WOF4*WOM4 + WOF5*WOM5 + WOF6*WOM6 + WOF7 *WOM7) * WOM0

Indexes 0…7 stand for chip numbers; see Table 7 and/or Table 28 for chip numbering scheme.

The FRONT_FPGA sets WOF to "1", when either the DAQ FIFO or the Ring Buffer are full. It drops WOF to "0" when both buffers become empty.

Table 36: CSR_WOF Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
WOM7	WOM6	WOM5	WOM4	WOM3	WOM2	WOM1	WOM0	WOF7	WOF6	WOF5	WOF4	WOF3	WOF2	WOF1	WOF0	R
WOM7	WOM6	WOM5	WOM4	WOM3	WOM2	WOM1	WOM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- WOM [7:0] – Warning-of-OverFlow Chip mask for SP, DD, F5…F1, and VM chips;
- WOF [7:0] – Warning-of-OverFlow status for SP, DD, F5…F1, and VM chips.

CSR_OSY – Out-of-Synch Control / Status

In the FRONT_FPGA this register shows a timing offset between BC0 marks, sent by the MPC and coming out of the Alignment FIFO, and the local bunch crossing counter (BXN) value. The BC0 mark strobes the BXN value into the offset register.

If the offset register content is not equal to zero for a given link, an Out-of-Synch status is generated. Bit D12 of the Out-of-Synch register allows masking the out-of-synch status individually for each link before the combined fast monitoring OSY signal is sent over to the VME_FPGA. Besides, link OSY status is reported only if the corresponding TLK2501 device is enabled, i.e. bit DVEN=1, see the register description.

See the CSR_BCO register description on how to adjust the BXN offset value to bring the control and data timing to synch.

In the VME_FPGA the CSR_OSY register displays status of seven input and one output OSY lines. Besides, it carries eight mask bits, so each input or/and output can be either disabled or enabled:

OSY0 = (OSY1*OSM1 + OSY2*OSM2 + OSY3*OSM3 + OSY4*OSM4 + OSY5*OSM5 + OSY6*OSM6 + OSY7 *OSM7) * OSM0

Indexes 0…7 stand for chip numbers; see Table 7 and/or Table 28 for chip numbering scheme.

Table 37 CSR_OSY Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
OSM7	OSM6	OSM5	OSM4	OSM3	OSM2	OSM1	OSM0	OSY7	OSY6	OSY5	OSY4	OSY3	OSY2	OSY1	OSY0	R
OSM7	OSM6	OSM5	OSM4	OSM3	OSM2	OSM1	OSM0	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- OSM [7:0] – Out-of-Synch Chip mask for SP, DD, F5…F1, and VM chips;
- OSY [7:0] – Out-of-Synch status for SP, DD, F5…F1, and VM chips.

Table 38 CSR_OSY Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
OSM	0	0	0	OFF11	OFF10	OFF9	OFF8	OFF7	OFF6	OFF5	OFF4	OFF3	OFF2	OFF1	OFF0	R
OSM	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- OFF [10:0] = offset register, default value on power-up is 0x7FF;
- OSM – Out-of-Synch link Mask, default value is "1" – The Out-of-Synch condition, if exists, is sent to the chip output.

CSR_FCC – Fast Control Configuration / Status

This read/write register sets the SP02 fast control modes and shows the status of the L1Accept control state machine. The FCM bit switches the source of fast control commands, which could be either from the local VME interface (default on power-up), or from the CCB over the TF crate backplane. The FCL bit controls if Local Charged Triggers (LCT) from the SP_FPGA are being sent to the backplane. The LCT is defines as Mode > 0 for the SP core output. The FCB bit controls the maximum value for the bunch counter to roll over. The L1Accept state machine is one-hot coded, so only one state bit could be equal to logical 1 at any time. For further details on the L1Accept state machine see Figure 1. There is also a copy of the L1Accept state machine in every other FPGAs, which is used for gating the Valid Pattern Counters.

Table 39: CSR_FCC Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	FCB	0	0	0	FCM	0	0	0	FCL	0	L1R	L1W	L1S	R
X	X	X	FCB	X	X	X	FCM	X	X	X	FCL	X	X	X	X	W

Here:

- X – Don't care bit;
- FCM = 1 (default) / 0 – VME (default) / CCB Fast Control Mode;
- FCB = 1 / 0 (default) – LHC->3563 / SPS->923 (default) BX counter mode;
- FCL = 1 / 0 (default) – enable / disable (default) Local Charge Trigger;
- L1S = 1 – L1Accept state machine is in the L1A_STOP state;
- L1W = 1 – L1Accept state machine is in the L1A_WAIT state;
- L1R = 1 – L1Accept state machine is in the L1A_RUN state.

Table 40: CSR_FCC Data Format for FRONT_FPGA, DDU_FPGA and SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
0	0	0	FCB	0	0	0	0	0	0	0	0	0	L1R	L1W	L1S	R
X	X	X	FCB	X	X	X	X	X	X	X	X	X	X	X	X	W

Here:

- X – Don't care bit;
- FCB = 1 / 0 (default) – LHC->3563 / SPS->923 (default) BX counter mode;
- L1S = 1 – L1A_STOP state of the L1Accept state machine;
- L1W = 1 – L1A_WAIT state of the L1Accept state machine;
- L1R = 1 – L1A_RUN state of the L1Accept state machine.

CSR_LEC – Link Error Counters

This read-only register monitors all possible link errors. The TLK2501 synchronization procedure, when the MPC switches TLK2501 transmitters into idle mode for 128 bunch crossings, always precedes the normal operation. Normal receiving operation assumes RXSD and RXDV to be High and RXER to be Low. To facilitate monitoring of error conditions, any combination of RXSD, RXDV and RXER other than normal is detected and countered. Error conditions are accumulated over time, starting from the previous synchronization procedure. Counter stops when it reaches its maximum value. The counters are reset on L1_Reset and begin count errors after Alignment FIFO has been enabled for writing. Addressing the ACT_LER register provides an alternative reset option.

Table 41: CSR_LEC Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SLC3	SLC2	SLC1	SLC0	CEC3	CEC2	CEC1	CEC0	EWC7	EWC6	EWC5	EWC4	EWC3	EWC2	EWC1	EWC0
Signal Loss Counter				Carrier Extend Counter				Error Word Counter							

Here:

- EWC [7:0] – TLK2501 Error Word Counter (RXDV == High, RXER == High);
- CEC [3:0] – TLK2501 Carrier Extend Counter (RXDV == Low, RXER == High);
- SLC [3:0] – FINISAR optical receiver Signal Loss Counter (RXSD goes Low).

CSR_AF – Alignment FIFO Status

This read-only register shows the number of words currently sitting in the Alignment FIFO (AF). After a link synchronization procedure has been performed, Alignment FIFOs for different links may show different word counts. Dispersion of word count values corresponds to the dispersion of link latencies. Adjusting the CCB clock in the Track-Finder crate, so that a minimum word count would be equal to 1, minimizes the overall time required to align all muon links. Register address is applicable to FRONT_FPGA (3 each) and to SP_FPGA (2 each – MA = 0|1|2). The maximum available value is 31.

Table 42: CSR_AF Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AFFF	AFEF	0	0	0	0	0	AFC8	AFC7	AFC6	AFC5	AFC4	AFC3	AFC2	AFC1	AFC0
Flags							Alignment FIFO Word Count								

Here:

- AFC [8:0] = 0...511 – Alignment FIFO Read Word Count;
- AFFF – Alignment FIFO Full Flag or AFC = 511;
- AFEF – Alignment FIFO Empty Flag.

CSR_TF – Test FIFO Status

This read-only register shows word count currently loaded into the Test FIFO (TF) and FIFO Flags. The maximum available TF capacity is 1024 16-bit words. Register address is applicable to FRONT_FPGA (3 each), DDU_FPGA (1 each) and SP_FPGA (3 each).

Table 43: CSR_TF Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFFF	TFEF	0	0	0	TFC10	TFC9	TFC8	TFC7	TFC6	TFC5	TFC4	TFC3	TFC2	TFC1	TFC0
Flags					Test FIFO Word Count										

Here:

- TFC [10:0] = 0...1024 – Test FIFO Word Count;
- TFFF – Test FIFO Full Flag or TFC = 1024;
- TFEF – Test FIFO Empty Flag.

CSR_SF – Spy FIFO Status

This read-only register shows the number of words currently sitting in the Spy FIFO (SF). One would probably want to know this value before setting up the BLT read cycle to read out the SF content. Maximum available SF capacity is 1024 16-bit words. Register address is applicable to FRONT_FPGA (3 each), DDU_FPGA (1 each) and SP_FPGA (3 each).

Table 44: CSR_SF Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFFF	SFEF	RXDV	RXER	0	SFC10	SFC9	SFC8	SFC7	SFC6	SFC5	SFC4	SFC3	SFC2	SFC1	SFC0
Flags		RX Status			Spy FIFO Word Count										

Here:

- SFC [10:0] = 0..1024 – Spy FIFO Word Count;
- SFFF – Spy FIFO Full Flag or 1024 Word Count;
- SFEF – Spy FIFO Empty Flag;
- RXDV, RXER – TLK2501 Receiver Status for the last data read out from the Spy FIFO.

CSR_PF – Pipeline FIFO Status

This read-only register shows the number of words currently loaded to the Pipeline FIFO (PF) and FIFO Flags. The maximum available PF capacity is 512 72-bit words. Register address is applicable to FRONT_FPGA. The PF content is not available for direct reads. Use Spy FIFO to grab data of interest at SF inputs or outputs.

Table 45: CSR_PF Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PFFF	PFEF	0	0	0	0	PFC9	PFC8	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0
Flags						Pipeline FIFO Word Count									

Here:

- PFC [9:0] = 0…512 – Pipeline FIFO Word Count;
- PFFF – Pipeline FIFO Full Flag or PFC = 512;
- PFEF – Pipeline FIFO Empty Flag.

CSR_DF – DAQ FIFO Status

This read-only register shows the number of words currently loaded to the DAQ FIFO (DF) and link error status for muon data words. The maximum available DF capacity is 4096 18-bit words. Register address is applicable to FRONT_FPGA. In the readout event format, see Table 105, the Synchronization Error (SE) bit resides in the second data frame. To provide for error analysis, the CSR_DF register retrieves Receive Error flags for both data frames, making them available after the second frame has been read out.

Table 46: CSR_DF Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DFFF	DFEF	0	DFC12	DFC11	DFC10	DFC9	DFC8	DFC7	DFC6	DFC5	DFC4	DFC3	DFC2	DFC1	DFC0
Flags			DAQ FIFO Word Count												

Here:

- DFC [12:0] = 0…4096 – DAQ FIFO Word Count;
- DFFF – Pipeline FIFO Full Flag or DFC = 4096;
- DFEF – Pipeline FIFO Empty Flag;
- CFRE – Current Frame Receive Error Flag;
- PFRE – Previous Frame Receive Error Flag.

CSR_LF – L1 Accept FIFO Status

This read-only register shows the number of words currently loaded to the L1 Accept FIFO (LF) and FIFO Flags. The maximum available LF capacity is 1024 54-bit words. Register address is applicable to FRONT_FPGA.

Table 47: CSR_LF Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LFFF	LFEF	0	0	0	LFC10	LFC9	LFC8	LFC7	LFC6	LFC5	LFC4	LFC3	LFC2	LFC1	LFC0
Flags					L1 Accept FIFO Word Count										

Here:

- LFC [10:0] = 0…1024 – L1 Accept FIFO Word Count;
- LFFF – L1 Accept FIFO Full Flag or LFC = 1024;
- LFEF – L1 Accept FIFO Empty Flag.

CSR_RBW – Ring Buffer Write Pointer

This read-only register shows the current address of the Ring Buffer Write Pointer. Ring Buffer is a 54 bit x 1024 word temporary storage for muon data, before they are get reformatted and put in the DAQ FIFO for readout. The register is valid for FRONT_FPGA and used for firmware debugging.

Table 48: CSR_RBW Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	RBW9	RBW8	RBW7	RBW6	RBW5	RBW4	RBW3	RBW2	RBW1	RBW0
						Ring Buffer Write Pointer Address									

Here:

– RBW [9:0] = 0...1023– Ring Buffer Write Pointer Address.

CSR_RBR – Ring Buffer Read Pointer

This read-only register shows the current position of the Ring Buffer Read Pointer. Ring Buffer is a 54 bit x 1024 word temporary storage for muon data, before they are get reformatted and put in the DAQ FIFO for readout. The register is valid for FRONT_FPGA and used for firmware debugging.

Table 49: CSR_RBR Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	RBR9	RBR8	RBR7	RBR6	RBR5	RBR4	RBR3	RBR2	RBR1	RBR0
						Ring Buffer Read Pointer Address									

Here:

– RBR [9:0] = 0…1023 – Ring Buffer Read Pointer.

CSR_SF1 – F1 Spy FIFO Status

This read-only registers, one register per F1 EMU muon, return the F1 Spy FIFO (SF1) Flags and the SF1 Word Count. The maximum available SF1 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 50: CSR_SF1 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF1FF	SF1EF	0	0	0	SF1C10	SF1C9	SF1C8	SF1C7	SF1C6	SF1C5	SF1C4	SF1C3	SF1C2	SF1C1	SF1C0
Flags					F1 Spy FIFO Word Count										

Here:

– SF1C [10:0] = 0…1024 – F1 Spy FIFO Word Count;
– SF1FF – F1 Spy FIFO Full Flag or SF1C = 1024;
– SF1EF – F1 Spy FIFO Empty Flag.

CSR_SF2 – F2 Spy FIFO Status

This read-only registers, one register per F2 EMU muon, return the F2 Spy FIFO (SF2) Flags and the SF2 Word Count. The maximum available SF2 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 51: CSR_SF2 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF2FF	SF2EF	0	0	0	SF2C10	SF2C9	SF2C8	SF2C7	SF2C6	SF2C5	SF2C4	SF2C3	SF2C2	SF2C1	SF2C0
Flags					F2 Spy FIFO Word Count										

Here:

- SF2C [10:0] = 0…1024 – F2 Spy FIFO Word Count;
- SF2FF – F2 Spy FIFO Full Flag or SF2C = 1024;
- SF2EF – F2 Spy FIFO Empty Flag.

CSR_SF3 – F3 Spy FIFO Status

This read-only registers, one register per F3 EMU muon, return the F3 Spy FIFO (SF3) Flags and the SF3 Word Count. The maximum available SF3 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 52: CSR_SF3 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF3FF	SF3EF	0	0	0	SF3C10	SF3C9	SF3C8	SF3C7	SF3C6	SF3C5	SF3C4	SF3C3	SF3C2	SF3C1	SF3C0
Flags					F3 Spy FIFO Word Count										

Here:

- SF3C [10:0] = 0…1024 – F3 Spy FIFO Word Count;
- SF3FF – F3 Spy FIFO Full Flag or SF3C = 1024;
- SF3EF – F3 Spy FIFO Empty Flag.

CSR_SF4 – F4 Spy FIFO Status

This read-only registers, one register per F4 EMU muon, return the F4 Spy FIFO (SF4) Flags and the SF4 Word Count. The maximum available SF4 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 53: CSR_SF4 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF4FF	SF4EF	0	0	0	SF4C10	SF4C9	SF4C8	SF4C7	SF4C6	SF4C5	SF4C4	SF4C3	SF4C2	SF4C1	SF4C0
Flags					F4 Spy FIFO Word Count										

Here:

- SF4C [10:0] = 0…1024 – F4 Spy FIFO Word Count;
- SF4FF – F4 Spy FIFO Full Flag or SF4C = 1024;
- SF4EF – F4 Spy FIFO Empty Flag.

CSR_SF5 – F5 Spy FIFO Status

This read-only registers, one register per F5 EMU muon, return the F5 Spy FIFO (SF5) Flags and the SF5 Word Count. The maximum available SF5 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 54: CSR_SF5 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SF5FF	SF5EF	0	0	0	SF5C10	SF5C9	SF5C8	SF5C7	SF5C6	SF5C5	SF5C4	SF5C3	SF5C2	SF5C1	SF5C0
Flags					F5 Spy FIFO Word Count										

Here:

- SF5C [10:0] = 0…1024 – F5 Spy FIFO Word Count;

- SF5FF – F5 Spy FIFO Full Flag or SF5C = 1024;
- SF5EF – F5 Spy FIFO Empty Flag.

CSR_SFE – EMU Spy FIFO Status

This read-only register, common for all EMU muons, returns the FE Spy FIFO (SFE) Flags and the SFE Word Count. The maximum available SFE capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA.

Table 55: CSR_SFE Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFEFF	SFEEF	0	0	0	SFEC10	SFEC9	SFEC8	SFEC7	SFEC6	SFEC5	SFEC4	SFEC3	SFEC2	SFEC1	SFEC0
Flags					FE Spy FIFO Word Count										

Here:

- SFEC [10:0] = 0…1024 – FE Spy FIFO Word Count;
- SFEFF – FE Spy FIFO Full Flag or SFEC = 1024;
- SFEEF – FE Spy FIFO Empty Flag.

CSR_LNK – Link Control/Status

This register provides static link control and status directly to and from both Finisar and TLK2501 transceivers' pins. Read-only upper byte shows receiver status, while lower byte provides access to control pins. Under the normal operational conditions register value equals to 0x0511 for a receiving link and equals to 0x0014 for a transmitting link. When TSEN is asserted High, results of pseudorandom bit stream tests can be monitored on the RXER output. A High on this terminal indicates that valid PRBS is being received. The PRBS test counter counts (RXER goes Low) events, when TSEN is High. It stops, when reaches its maximum value of 31. Counter reset is provided through addressing to the ACT_LER register.

When the TLK2501 device is disabled (DVEN is set to "0") the corresponding ready/busy link status is masked off and does not contribute to the overall FRONT_FPGA fast monitoring status.

Table 56: CSR_LNK Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Acc
TEC4	TEC3	TEC2	TEC1	TEC0	RXDV	RXER	RXSD	0	TSEN	LPEN	DVEN	0	TXEN	TXER	TXDI	R
X	X	X	X	X	X	X	X	X	TSEN	LPEN	DVEN	X	TXEN	TXER	TXDI	W

Here:

- X – Don't care bit for writes;
- TXDI = 1/0 – Disable / Enable (default) the FINISAR optical Transmitter;
- {TXEN, TXER} = {Transmit Enable, Error Coding} – Transmit Data Control:
  - {TXEN,TXER} = {0,0} – Transmit Idle Character (0xC5BC or 0x50BC);
  - {TXEN,TXER} = {0,1} – Transmit Carrier Extend (0xF7F7);
  - {TXEN,TXER} = {1,0} – Transmit Normal Data Character -> default
  - {TXEN,TXER} = {1,1} – Transmit Error Propagation (0xFEFE);
- DVEN = 1/0 – Enable (default) / Disable the TLK2501 Device;
- LPEN = 1/0 – Enable / Disable (default) the TLK2501 Loop mode;

- TSEN = 1/0 – Enable / Disable (default) the TLK2501 Pseudorandom Bit Stream (PRBS) Test ;
- RXSD = 1/0 – Signal Detect/No Signal from FINISAR optical receiver;
- { RXDV, RXER} = { Receive Data Valid, Receive Error} – Receive Status Signals
  - {RXDV, RXER} = {0,0} – Receive Idle Character (0xC5BC or 0x50BC);
  - {RXDV, RXER} = {0,1} – Receive Carrier Extend (0xF7F7);
  - {RXDV, RXER} = {1,0} – Receive Normal Data Character;
  - {RXDV, RXER} = {1,1} – Receive Error Propagation (0xFEFE);

TEC [4:0] – PRBS Test Error Counter;

CSR_AFD - Alignment FIFO Read Delay

This read/write register controls delaying of the AF read enable signal after an L1 Reset occurs. In fact, the total delay calculates as (64 + CSR_AFD Value) bx after an L1 Reset. The register is used to optimize muon alignment budget. The register resides in the FRONT_FPGA.

Table 57: CSR_AFD Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	AFD6	AFD5	AFD4	AFD3	AFD2	AFD1	AFD0
									Alignment FIFO Read Delay						

Here:

- X – don't care bit for writes and zero for reads
- AFD[6:0] = 0…127 – AF resumes reads on the (64+1... 64+127) bx after an L1 Reset has been received. The register default value on power-up is 112, which gives the default delay of 176 bx.

CSR_TFC – Test FIFO Configuration

This read/write register defines where the Test FIFO (TF) injects test patterns, whether injected patterns get written back to the TF, and whether the entire content of the TF or just the specified number is injected.

The default register settings are used to run a link test with data patterns, similar to the MPC-SP one. The difference is that the SP can drive 15 optical outputs to test its 15 optical inputs at once, while one MPC is capable to drive only 3 optical cables. As for the rest, the procedure is quite similar, i.e. the user:

- connects 15 SP outputs to the 15 inputs of the same or another SP;
- configures the CSR_LNK register, if needed;
- sets the CSR_FCC into a local fast control mode, in order not to interfere with other modules in the same crate, if only one SP is under tests;
- addresses ACT_FCC to issue L1 Reset and perform link alignment procedure;
- loads the DAT_TF register with the test patterns in the same format, as he would do it for the MPC;
- compensates for the data path latency (the optical cable length, the AF word count, and the PF word count, if the SF is hooked up to its output) by configuring the CSR_SFC registers accordingly;

- runs the CCB_TPSP command;
- reads back the DAT_SF content and compares it with the original test patterns.

For the TFT = 1, when the TLK2501 transmitter is the test pattern destination, BC0 and BX0 timing bits are picked dynamically from the ccb bunch counter, running at the CCB backplane timing. It is done to prevent the Out-of-Synch condition to occur, once the link bunch counter has been tuned during the alignment procedure.

For the TFA = 1, when test patterns are injected in the incoming link data stream at the AF output, BC0 and BX0 bits are picked dynamically from the link data. Again, it is done to prevent the Out-of-Synch condition to occur, once the link bunch counter has been tuned during the alignment procedure.

Table 58: CSR_TFC Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFL	X	TFA	TFT	X	X	X	TFW8	TFW7	TFW6	TFW5	TFW4	TFW3	TFW2	TFW1	TFW0
Loop		Destination					Test FIFO Window								

Table 59: CSR_TFC Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFT	TFA	TFL	TFM	X	X	X	TFC8	TFC7	TFC6	TFC5	TFC4	TFC3	TFC2	TFC1	TFC0
Destination		Loop	Mode				Test FIFO Window								

Here:

- X – don't care bit for writes and zero for reads;
- TFW [8:0] = 0…511 – if TFM bit is set, then inject test patterns for 1…512 bunch crossings on the next CCB_TPSP / FC_TFRUN command, default value is 0;
- TFL = 1/0 – TF Loopback option: inject and write back data into the TF / just inject data into the destination circuit (default);
- TFA = 1/0 – enable / disable (default) injecting test data at the AF output;
- TFT = 1/0 – enable / disable (default) injecting test data into the TLK2501 transmitter.

Table 60: CSR_TFC Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFL	TFB	TFE	TFT	X	X	X	TFW8	TFW7	TFW6	TFW5	TFW4	TFW3	TFW2	TFW1	TFW0
Loop	Destination						Test FIFO Window								

Table 61: CSR_TFC Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFI	TFO	TFL	TFM	X	X	X	TFC8	TFC7	TFC6	TFC5	TFC4	TFC3	TFC2	TFC1	TFC0
Destination		Loop	Mode				Test FIFO Bunch Crossing Count								

Here:

- X – don't care bit for writes and zero for reads;
- TFW [8:0] = 0…511 – if TFM bit is set, then inject test patterns for 1…512 bunch crossings on the next CCB_TPSP / FC_TFRUN command, default value is 0;
- TFL = 1/0 – TF Loopback option: inject and write back data into the TF / just inject data into the destination circuit (default);

- TFE = 1/0 – enable / disable (default) injecting EMU muon test data (simulates EMU track stubs) from the EMU Test FIFOs: DAT_TF1/ DAT_TF2/ DAT_TF3/ DAT_TF4/ DAT_TF5/ DAT_TFE;
- TFB = 1/0 – enable / disable (default) injecting Barrel muon test data (simulates Barrel track stubs) from the Barrel Test FIFOs: DAT_TFB;
- TFT = 1/0 – enable / disable (default) injecting Track test data (simulates SP core output) from the Test FIFOs: DAT_TF.

CSR_SFC – Spy FIFO Configuration

In the VME_FPGA this register defines the delay inserted between the CCB test commands and the FC_SFRUN command on the internal FC bus, see Table 2. The delay is intended to compensate for the time required for the corresponding test data to reach the Spy FIFO input. The delay is not applicable to the CCB_L1ACC command. The register also determines if request for data is one-time or persistent. Power-up default state for this register is 0x0000.

Table 62: CSR_SFC Data Format for VME_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFM	SFRL	SFRS	SFRM	SFRT	X	SFD9	SFD8	SFD7	SFD6	SFD5	SFD4	SFD3	SFD2	SFD1	SFD0
Mode	Requests					Spy FIFO Delay Setting									

Here:

- X – don't care bit for writes and zero for reads;
- SFD [9:0] = 0 (default)…1023 - Spy FIFO starts writing data, when 1…1024 bunch crossings have passed after the requested event;
- SFRT = 1/0 (default) – store/don't store data on the next CCB_TPTMB command;
- SFRM = 1/0 (default) – store/don't store data on the next CCB_TPMPC command;
- SFRS = 1/0 (default) – store/don't store data on the next CCB_TPSP command;
- SFRL = 1/0 (default) – store/don't store data on the next CCB_L1ACC command;
- SFM = 1/0 (default) – persistent/one-time request. Persistent request stores data on all events that followed. One-time request stores data on the next event only and self-resets after that.

In the FRONT_FPGA this register defines the data source for the Spy FIFO input and the number of beam crossings to be stored upon receiving the FC_SFRUN command. Note that the actual number of 16-bit words, saved in the Spy FIFO is twice as big, since each beam crossing data consists of two frames.

Table 63: CSR_SFC Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFS	X	X	X	X	X	X	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
Source							Spy FIFO Bunch Crossing Count								

Here:

- X – Don't care bit for writes and zero for reads;
- SF [8:0] = 0 (default)…511 – Spy FIFO grabs data from 1…512 bunch crossings;

– SFS = 1 / 0 (default) – connects the Spy FIFO input to the Pipeline FIFO output / input (default) to grab data.

Table 64: CSR_SFC Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFS	X	SFM1	SFM0	X	X	X	SF8	SF7	SF6	SF5	SF4	SF3	SF2	SF1	SF0
Source		Data Source					Spy FIFO Bunch Crossing Count								

Here:

– X – Don't care bit for writes and zero for reads;
– SF [8:0] = 0 (default)…511 – Spy FIFO grabs data from 1…512 bunch crossings;
– SFM [1:0] = 0 (default) …3 – MS Spy FIFO (DAT_SFM) spies on PT[SFM] output data;
– SFS = 1 / 0 (default) – connects the Spy FIFO (DAT_SF) input to the Pipeline FIFO output / input (default) to grab data.

CSR_PFD – Pipeline FIFO Data Delay

This read/write register controls data delay in the Pipeline FIFO to compensate for L1 Accept latency. Default value on power-up is 128.

Table 65: CSR_PFD Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	PFD7	PFD6	PFD5	PFD4	PFD3	PFD2	PFD1	PFD0
								Pipeline FIFO Data Delay							

Here:

– X – Don't care bit for writes and zero bit for reads;
– PFD = 0…255 – PF delays data for 1... 256 bunch crossings or up to 6.4 μsec.

CSR_DFC – DAQ FIFO Configuration

This read/write register controls event size or the number of bunch crossing to be saved into the DAQ FIFO upon receiving an L1 Accept. When a zero DFB value is loaded, no muon data is saved on L1 Accept, and each event consists only of a Header block, see Table 105 for details. Default event size on power-up is 2.

Table 66: CSR_DFC Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	DFB4	DFB3	DFB2	DFB1	DFB0
											DAQ FIFO Bunch Crossings Count				

Here:

– X – Don't care bit for writes and zero for reads;
– DFB [4:0] = 0…31 – DAQ FIFO stores data from 0…31 bunch crossings.

CSR_SCC – SP Core Configuration

This read/write register keeps the SP core configuration options.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine

should be in the L1_STOP state. The above implies executing the following two VME commands:

- VW/MA/CSR_FCC/W/0x0100 -> put the SP02 under the VME control
- VM/MA/ACT_FCC/W/0x00C8 -> issue the bx reset command

before addressing the data register.

Table 67: CSR_DFC Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	BXE

Here:

- X – Don't care bit for writes and zero for reads;
- BXE = 1(default) / 0 – Bunch crossing analyzer enable (default) / disable.

CSR_SFM – Muon Sorter Spy FIFO Status

This read-only register, one per SP output track, returns the MS Spy FIFO (SFM) Flags and the SFM Word Count. The maximum available SFM capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA.

Table 68: CSR_SFM Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SFMFF	SFMEF	0	0	0	SFMC10	SFMC9	SFMC8	SFMC7	SFMC6	SFMC5	SFMC4	SFMC3	SFMC2	SFMC1	SFMC0
Flags					FE Spy FIFO Word Count										

Here:

- SFMC [10:0] = 0…1024 – MS Spy FIFO Word Count;
- SFMFF – MS Spy FIFO Full Flag or SFMC = 1024;
- SFMEF – MS Spy FIFO Empty Flag.

CSR_TF1 – F1 Test FIFO Status

This read-only registers, one register per F1 EMU muon, return the F1 Test FIFO (TF1) Flags and the TF1 Word Count. The maximum available TF1 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 69: CSR_TF1 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF1FF	TF1EF	0	0	0	TF1C10	TF1C9	TF1C8	TF1C7	TF1C6	TF1C5	TF1C4	TF1C3	TF1C2	TF1C1	TF1C0
Flags					F1 Test FIFO Word Count										

Here:

- TF1C [10:0] = 0…1024 – F1 Test FIFO Word Count;
- TF1FF – F1 Test FIFO Full Flag or TF1C = 1024;
- TF1EF – F1 Test FIFO Empty Flag.

CSR_TF2 – F2 Test FIFO Status

This read-only registers, one register per F2 EMU muon, return the F2 Test FIFO (TF2) Flags and the TF2 Word Count. The maximum available TF2 capacity is 1024 16-bit words, or

data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 70: CSR_TF2 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF2FF	TF2EF	0	0	0	TF2C10	TF2C9	TF2C8	TF2C7	TF2C6	TF2C5	TF2C4	TF2C3	TF2C2	TF2C1	TF2C0
Flags					F2 Test FIFO Word Count										

Here:

- TF2C [10:0] = 0…1024 – F2 Test FIFO Word Count;
- TF2FF – F2 Test FIFO Full Flag or TF2C = 1024;
- TF2EF – F2 Test FIFO Empty Flag.

CSR_TF3 – F3 Test FIFO Status

This read-only registers, one register per F3 EMU muon, return the F3 Test FIFO (TF3) Flags and the TF3 Word Count. The maximum available TF3 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 71: CSR_TF3 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF3FF	TF3EF	0	0	0	TF3C10	TF3C9	TF3C8	TF3C7	TF3C6	TF3C5	TF3C4	TF3C3	TF3C2	TF3C1	TF3C0
Flags					F3 Test FIFO Word Count										

Here:

- TF3C [10:0] = 0…1024 – F3 Test FIFO Word Count;
- TF3FF – F3 Test FIFO Full Flag or TF3C = 1024;
- TF3EF – F3 Test FIFO Empty Flag.

CSR_TF4 – F4 Test FIFO Status

This read-only registers, one register per F4 EMU muon, return the F4 Test FIFO (TF4) Flags and the TF4 Word Count. The maximum available TF4 capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 72: CSR_TF4 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF4FF	TF4EF	0	0	0	TF4C10	TF4C9	TF4C8	TF4C7	TF4C6	TF4C5	TF4C4	TF4C3	TF4C2	TF4C1	TF4C0
Flags					F4 Test FIFO Word Count										

Here:

- TF4C [10:0] = 0…1024 – F4 Test FIFO Word Count;
- TF4FF – F4 Test FIFO Full Flag or TF4C = 1024;
- TF4EF – F4 Test FIFO Empty Flag.

CSR_TF5 – F5 Test FIFO Status

This read-only registers, one register per F5 EMU muon, return the F5 Test FIFO (TF5) Flags and the TF5 Word Count. The maximum available TF5 capacity is 1024 16-bit words, or

data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 73: CSR_TF5 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TF5FF	TF5EF	0	0	0	TF5C10	TF5C9	TF5C8	TF5C7	TF5C6	TF5C5	TF5C4	TF5C3	TF5C2	TF5C1	TF5C0
Flags					F5 Test FIFO Word Count										

Here:

- TF5C [10:0] = 0…1024 – F5 Test FIFO Word Count;
- TF5FF – F5 Test FIFO Full Flag or TF5C = 1024;
- TF5EF – F5 Test FIFO Empty Flag.

CSR_TFE – EMU Test FIFO Status

This read-only register, common for all EMU muons, returns the FE Test FIFO (TFE) Flags and the TFE Word Count. The maximum available TFE capacity is 1024 16-bit words, or data for 512 bunch crossings, 2 frames per bx. The register address is applicable to the SP_FPGA only.

Table 74: CSR_TFE Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
TFEFF	TFEEF	0	0	0	TFEC10	TFEC9	TFEC8	TFEC7	TFEC6	TFEC5	TFEC4	TFEC3	TFEC2	TFEC1	TFEC0
Flags					FE Test FIFO Word Count										

Here:

- TFEC [10:0] = 0…1024 – FE Test FIFO Word Count;
- TFEFF – FE Test FIFO Full Flag or TFEC = 1024;
- TFEEF – FE Test FIFO Empty Flag.

Address Counter Register Group

CNT_LPL – Local Phi LUT Address Counter Low

This read/write register carries current value of the local phi LUT address counter 16 Least Significant Bits (LSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all local LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_LP register in a chip. The counter can be reset with the ACT_ACR command.

Table 75: CNT_LPL Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LA15	LA14	LA13	LA12	LA11	LA10	LA9	LA8	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0
Local Phi LUT Address Counter LSB															

Here:

- X – Don’t care bit;
- LA [15:0] – Local Phi LUT Address Counter, 16 LSB.

CNT_LPH – Local Phi LUT Address Counter High

This read/write register carries current value of the local phi LUT address counter 3 Most Significant Bits (MSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all local LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_LP register in a chip. The counter can be reset with the ACT_ACR command.

Table 76: CNT_LPH Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	LA18	LA17	LA16
													LP LUT AC MSB		

Here:

- X – Don't care bit;
- LA [18:16] – Local Phi LUT Address Counter, 3 MSB.

CNT_GLL – Global LUTs Address Counter Low

This read/write register carries current value of the global LUTs address counter 16 Least Significant Bits (LSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all global LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_GP/DAT_DT/DAT_GE register in a chip. The counter can be reset with the ACT_ACR command.

Table 77: CNT_GLL Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GA15	GA14	GA13	GA12	GA11	GA10	GA9	GA8	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0
Global LUTs Address Counter LSB															

Here:

- X – Don't care bit for writes and zero for reads;
- GA [15:0] – Global LUTs Address Counter, 16 LSB.

CNT_GLH – Global LUTs Address Counter High

This read/write register carries current value of the global LUTs address counter 3 Most Significant Bits (MSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all global LUTs serviced by the FRONT_FPGA and auto-increments on every access to any DAT_GP/DAT_DT/DAT_GE register in a chip. The counter can be reset with the ACT_ACR command.

Table 78: CNT_GLH Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	X	X	GA18	GA17	GA16
													GL LUTs AC MSB		

Here:

- X – Don't care bit for writes and zero for reads;
- GA [18:16] – Global LUTs Address Counter, 3 MSB.

CNT_PTL – PT LUTs Address Counter Low

This read/write register carries current value of the PT LUTs address counter 16 Least Significant Bits (LSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all PT LUTs serviced by the SP_FPGA and auto-increments on every access to any DAT_PT register in a chip. The counter can be reset with the ACT_ACR command.

Table 79: CNT_PTL Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PTA15	PTA14	PTA13	PTA12	PTA11	PTA10	PTA9	PTA8	PTA7	PTA6	PTA5	PTA4	PTA3	PTA2	PTA1	PTA0
PT LUTs Address Counter LSB															

Here:

- X – Don't care bit for writes and zero for reads;
- PTA [15:0] – PT LUTs Address Counter, 16 LSB.

CNT_PTH – PT LUTs Address Counter High

This read/write register carries current value of the global LUTs address counter 3 Most Significant Bits (MSB), as shown in the table below. The default register value on power-up is zero. The counter is common for all PT LUTs serviced by the SP_FPGA and auto-increments on every access to any DAT_PT register in a chip. The counter can be reset with the ACT_ACR command.

Table 80: CNT_PTH Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	PTA20	PTA19	PTA18	PTA17	PTA16
											PT LUTs AC MSB				

Here:

- X – Don't care bit for writes and zero for reads;
- PTA [20:16] – Global LUTs Address Counter, 5 MSB.

CNT_ETA – Eta Address Counter

This read/write register carries current value of the Eta Min/Max/Window Address Counter, as shown in the table below. The default register value on power-up is zero. The counter auto-increments on every access to the DAT_ETA register. The counter can be reset with the ACT_ACR command.

Table 81: CNT_ETA Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	X	X	X	ETA4	ETA3	ETA2	ETA1	ETA0
											ETA Address Counter				

Here:

- X – Don't care bit for writes and zero for reads;
- ETA [4:0] = 0…21 – Eta Min/Max/Window Address Counter.

Data Register Group

DAT_TF1 – F1 Test FIFO Data

This write-only register in the SP_FPGA, one register per F1 EMU muon, keeps the F1 Test FIFO (TF1) data. The TF1 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 82: DAT_TF1 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15;
- CSC ID [3:0] = 1…9.

DAT_TF2 – F2 Test FIFO Data

This write-only register in the SP_FPGA, one register per F2 EMU muon, keeps the F2 Test FIFO (TF2) data. The TF2 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 83: DAT_TF2 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15;
- CSC ID [3:0] = 1…9.

DAT_TF3 – F3 Test FIFO Data

This write-only register in the SP_FPGA, one register per F3 EMU muon, keeps the F3 Test FIFO (TF3) data. The TF3 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 84: DAT_TF3 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
X	X	X	X	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- X – don't care bit;
- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_TF4 – F4 Test FIFO Data

This write-only register in the SP_FPGA, one register per F4 EMU muon, keeps the F4 Test FIFO (TF4) data. The TF4 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 85: DAT_TF4 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
X	X	X	X	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- X – don't care bit;
- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_TF5 – F5 Test FIFO Data

This write-only register in the SP_FPGA, one register per F5 EMU muon, keeps the F5 Test FIFO (TF5) data. The TF5 data can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. Information on valid pattern (VP) and synchronization error (SE) bits is combined in a separate FE Test FIFO. On how to configure the testing process refer to the CSR_TFC register description.

Table 86: DAT_TF5 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
X	X	X	X	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- X – don't care bit;
- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;

– Quality [3:0] = 0…15.

DAT_TFE – EMU Test FIFO Data

This write-only register in the SP_FPGA keeps the FE Test FIFO data, which carries VP and SE bits for all fifteen EMU muons. The content of the TFE can be injected into the data path on the fast control FC_TFRUN command to test the SP core functionality. On how to configure the testing process refer to the CSR_TFC register description.

Table 87: DAT_TFE Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
F5 VP Flags			F4 VP Flags			F3 VP Flags			F2 VP Flags			F1 VP flags			X	FR1
F5 SE Flags			F4 SE Flags			F3 SE Flags			F2 SE Flags			F1 SE flags			X	FR2

Here:

– X – don't care bit;
– Valid Pattern flags, one per EMU muon;
– Synch Error flags, one per EMU muon.

DAT_LP – Local Phi LUT Data

This read/write registers provides access to the Local Phi LUT content. The LP LUT data format is shown in Table 88. Read/write transfers are performed on the LP LUT current address defined by the CNT_LPL and CNT_LPH values; after that the counter auto-increments. Note, that the local phi LUT address counter is common to all three muons, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

– VW/MA/CSR_FCC/W/0x0100 -> under VME control
– VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 88: DAT_LP Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LPB5	LPB4	LPB3	LPB2	LPB1	LPB0	LP9	LP8	LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0
Local Phi Bend						Local Phi									

Here:

– LP [9:0] = 0…1023 – Local Phi.
– LPB [5:0] = 0…31 – Local Phi Bend.

DAT_GP – Global Phi LUT Data

This read/write registers provides access to the Global Phi LUT content. The GP LUT data format is shown in the table below. Read/write transfers are performed on the GP LUT current address defined by the CNT_GLL and CNT_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

- VW/MA/CSR_FCC/W/0x0100 -> under VME control
- VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 89: DAT_GP Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
				Global Phi											

Here:

- X – don't care bit, returns zero on reads;
- GP [11:0] = 0…4095 – Global Phi.

DAT_DT – Drift Tube Global Phi LUT Data

This read/write registers provides access to the Drift Tube Global Phi LUT content. The DT LUT data format is shown in the table below. Read/write transfers are performed on the DT LUT current address defined by the CNT_GLL and CNT_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

- VW/MA/CSR_FCC/W/0x0100 -> under VME control
- VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 90: DAT_DT Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	DT11	DT10	DT9	DT8	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
				Drift Tube Global Phi											

Here:

- X – don't care bit, returns zero on reads;
- DT [11:0] = 0…4095 – Drift Tube Global Phi.

DAT_GE – Global Eta LUT Data

This read/write registers provides access to the Global Eta LUT content. The GE LUT data format is shown in the table below. Read/write transfers are performed on the GE LUT current address defined by the CNT_GLL and CNT_GLH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three muons and to the DT/GP/GE LUTs, serviced by the FRONT_FPGA. Register address is applicable to the FRONT_FPGA only.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

- VW/MA/CSR_FCC/W/0x0100 -> under VME control
- VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 91: DAT_GE Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	GE11	GE10	GE9	GE8	GE7	GE6	GE5	GE4	GE3	GE2	GE1	GE0
				Global Phi Bend					Global Eta						

Here:

- X – don't care bit, returns zero on reads;
- GE [6:0] = 0…127 – Global Eta;
- GE[11:7] = 0…31 – Global Phi Bend;

DAT_PT – PT LUT Data

This read/write registers provides access to the PT LUT content. The PT LUT data format is shown in the table below. Read/write transfers are performed on the PT LUT current address defined by the CNT_PTL and CNT_PTH values; after that the counter auto-increments. Note, that the global LUTs address counter is common to all three PT LUTs serviced by the SP_FPGA.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two commands:

- VW/MA/CSR_FCC/W/0x0100 -> under VME control
- VM/MA/ACT_FCC/W/0x00C8 -> bx reset command

before addressing the data register.

Table 92: DAT_PT Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RVC	RQ1	RQ0	RR4	RR3	RR2	RR1	RR0	FVC	FQ1	FQ0	FR4	FR3	FR2	FR1	FR0
Rear Muon Data								Front Muon Data							

Here:

- RVC – Rear muon Valig Charge;
- RQ[1:0] – Rear muon Quality;
- RR[4:0] – Rear muon Rank;
- FVC – Front muon Valig Charge;
- FQ[1:0] – Front muon Quality;
- FR[4:0] – Front muon Rank.

DAT_ETA – Eta Min/Max/Win Data

This read/write register provides access to the Eta register file content. The register file keeps data for Eta Minimum – 8 words, Eta Maximum – 8 words, and Eta Window – 6 words

setting, which totals to 22 data words. The CNT_ETA counter provides indexed access to the register content; see the CNT_ETA register description for details.

This register is protected against accidental accesses: in order to get VME access to this register the SP02 should be set to the VME fast control mode and the L1Access state machine should be in the L1_STOP state. The above implies executing the following two VME commands:

- VW/MA/CSR_FCC/W/0x0100 -> put the SP02 under the VME control
- VM/MA/ACT_FCC/W/0x00C8 -> issue the bx reset command

before addressing the data register.

Table 93: DAT_ETA Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	ETAP7	ETAP6	ETAP5	ETAP4	ETAP3	ETAP2	ETAP1	ETAP0
								Eta Parameters							

Here:

- X – don't care bit, reads back as zero;
- ETAP [7:0] = 0…127 for Eta Minimum;
- ETAP [7:0] = 0…127 for Eta Maximum;
- ETAP [7:0] = 0…255 for Eta Window;

DAT_VPC – Valid Pattern Counter Data

This read-only register is intended to monitor incoming muon stub rate for each link by counting the number of Valid Pattern bits at the Alignment FIFO output in the FRONT_FPGAs and outgoing track rate for each SP core output by counting the number of Mode>0 decisions in the SP_FPGA. The counter control follows that of the event counter: it is reset on the CCB_L1RES, CCB_BXRES and CCB_ECRES commands and enabled, when data taking state machine is in an L1A_RUN state, see Figure 1 for details on L1Accept control. The DAT_VPC address is applicable to FRONT_FPGAs.

Table 94: DAT_VP Data Format for FRONT_FPGA, SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
VP15	VP14	VP13	VP12	VP11	VP10	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
Valid Pattern Counter															

DAT_SF1 – F1 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F1 EMU muon, returns data from the F1 Spy FIFO (SF1). The SF1 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 95: DAT_SF1 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15;
- CSC ID [3:0] = 1…9.

DAT_SF2 – F2 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F2 EMU muon, returns data from the F2 Spy FIFO (SF2). The SF2 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 96: DAT_SF2 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
CSC ID [3:0]				Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15;
- CSC ID [3:0] = 1…9.

DAT_SF3 – F3 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F3 EMU muon, returns data from the F3 Spy FIFO (SF3). The SF3 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 97: DAT_SF3 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
0	0	0	0	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_SF4 – F4 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F4 EMU muon, returns data from the F4 Spy FIFO (SF4). The SF4 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and

BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 98: DAT_SF4 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
0	0	0	0	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_SF5 – F5 Spy FIFO Data

This read-only register in the SP_FPGA, one register per F5 EMU muon, returns data from the F5 Spy FIFO (SF5). The SF5 spies on the data after it has passed the local and global LUTs. Information on valid pattern (VP) and synchronization error (SE) bits, as well as BX0 and BC0 timing marks is combined in a separate FE Spy FIFO. On how to configure the spying process refer to the CSR_SFC register description.

Table 99: DAT_SF5 Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
Quality [3:0]				Global Phi [11:0]												FR1
0	0	0	0	Global Phi Bend[4:0]					Global Eta[6:0]							FR2

Here:

- Global Phi [11:0] = 0…4095;
- Global Eta [6:0] = 0…127;
- Global Phi Bend [11:7] = 0…31;
- Quality [3:0] = 0…15.

DAT_SFE – EMU Spy FIFO Data

This read-only register in the SP_FPGA returns data from the FE Spy FIFO, which carries VP, SE and timing marks for all fifteen EMU muons. Each FRONT_FPGA sends a pair of timing marks to the SP_FPGA, but all active muon links should be timed on L1 Reset, so that the timing is the same for all FRONT_FPGAs. What the Spy FIFO captures is a logical OR of five BC0 and five BX0 timing signals. On how to configure the spying process refer to the CSR_SFC register description.

Table 100: DAT_SFE Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
F5 VP Flags			F4 VP Flags			F3 VP Flags			F2 VP Flags			F1 VP flags			BX0	FR1
F5 SE Flags			F4 SE Flags			F3 SE Flags			F2 SE Flags			F1 SE flags			BC0	FR2

Here:

- Valid Pattern flags, one per EMU muon;
- Synch Error flags, one per EMU muon;
- BX0 – Bunch Counter LSB;

– BC0 – Bunch Crossing Zero mark.

DAT_TF – Test FIFO Data

VME cycles addressed to this write-only register load data in the Test FIFO (TF). Preferred method for loading TF with data is setting up a BLT write cycle. Address is valid for FRONT_FPGA (3 each), DDU_FPGA (1 each), and SP_FPGA (3 each).

The output of the FRONT_FPGA TF is normally connected to the TLK2501 transmitter to provide a source of data patterns for link tests. Alternatively, during data taking phase TF data may be injected in the data steam, substituting the Alignment FIFO output for one or more bunch crossings. TF destination is defined by the CSR_TFC register. CCB fast control signals (TBD) are responsible for test pattern injection. Table 101 shows the TF data format, which exactly follows the MPC – SP two-frame data format.

Data loaded into the TF cannot be verified by reading it back, since FIFO reads are destructive. Addressing to the CSR_TF register provides an indirect verification method of the current TF word count.

Table 101: DAT_TF Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							FR1
CSC ID [3:0]				X	X	SE	L/R	CLCT Pattern ID [7:0]								FR2

Here:

– X – Don’t care bit;
– VP – Valid Pattern flag;
– Quality - the more hits the higher track Quality;
– CLCT Pattern # - the 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit;
– Wire Group ID - the 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111;
– CSC ID - the 4-bit CSC ID indicates the chamber # and runs from 1 to 9;
– SE - Synchronization Error bit;
– L/R - the Left/Right bend bit indicates whether the track is heading towards lower or higher strip number;
– CLCT Pattern ID - For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber.

Table 102: DAT_TF Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
RSV	SE	HL	CHRG	FR	SIGN	Eta [4:0]					Phi [4:0]					FR1
Mode [3:0]				Delta23 Phi [3:0]				Delta12 Phi [7:0]								FR2

Here:

– Phi [4:0] is the Azimuth Coordinate;
– Eta [4:0] is the Pseudorapidity, the Eta [4:1] is a part of the PT LUT address;

- SIGN – the Delta Phi Sign bit is a part of the PT LUT address;
- FR – the Front/Rear bit;
- CHRG – the Muon Charge or Sign bit;
- HL – the Halo bit;
- SE – the Synchronization Error bit;
- RSV – the Reserved bit;
- Delta12 Phi [7:0] is a part of the PT LUT address;
- Delta23 Phi [3:0] is a part of the PT LUT address;
- Mode [3:0] is a part of the PT LUT address.

DAT_SF – Spy FIFO Data

VME cycles addressed to this read-only register return data from the Spy FIFO (SF). Preferred method of reading the SF content is setting up the BLT read. Before reading the SF content it is useful to check the SF status, by addressing to the CSR_SF register, which would return the current SF word count. Address is valid for FRONT_FPGA (3 each) and SP_FPGA (3 each).

The FRONT_FPGA SF input could be connected to either Pipeline FIFO Input or Pipeline FIFO output, as defined by the CSR_SFC register. Data format for both sources is shown in table below. The process of collecting data into the SF is regulated by fast control commands.

Table 103: DAT_SF Data Format for FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							FR1
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								FR2

Here:

- VP – Valid Pattern flag;
- Quality - the more hits the higher track Quality;
- CLCT Pattern # - the 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit;
- Wire Group ID - the 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111;
- CSC ID - the 4-bit CSC ID indicates the chamber # and runs from 1 to 9;
- BC0 - the Bunch Crossing Zero flag marks bunch zero data**;**
- BX0 - the least significant bit of Bunch Crossing Number (BXN ranges from 0 to 3563);
- SE - Synchronization Error bit;
- L/R - the Left/Right bend bit indicates whether the track is heading towards lower or higher strip number;
- CLCT Pattern ID - For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number

corresponds to the position of the pattern selected at the third or “key” layer of the chamber.

The SP_FPGA SF input could be connected to either Pipeline FIFO Input or Pipeline FIFO output, as defined by the CSR_SFC register. Data format for both sources is shown in table below. The process of collecting data into the SF is regulated by fast control commands.

Table 104: DAT_SF Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
RSV	SE	HL	CHRG	FR	SIGN	Eta [4:0]					Phi [4:0]					FR1
Mode [3:0]				Delta23 Phi [3:0]				Delta12 Phi [7:0]								FR2

Here:

- Phi [4:0] is the Azimuth Coordinate;
- Eta [4:0] is the Pseudorapidity, the Eta [4:1] is a part of the PT LUT address;
- SIGN – the Delta Phi Sign bit is a part of the PT LUT address;
- FR – the Front/Rear bit;
- CHRG – the Muon Charge or Sign bit;
- HL – the Halo bit;
- SE – the Synchronization Error bit;
- RSV – the Reserved bit;
- Delta12 Phi [7:0] is a part of the PT LUT address;
- Delta23 Phi [3:0] is a part of the PT LUT address;
- Mode [3:0] is a part of the PT LUT address.

DAT_DF – DAQ FIFO Data

VME cycles addressed to this read-only register retrieve event data from the DAQ FIFO (DF). The data format has a header followed by a specified number of data blocks. Each block is composed of 3 muons, 2 frames per muon, see Table 105 for details. The SP header structure follows the DMB header structure and starts with the number of data blocks or, in other words, the number of bunch crossings for which the muon data is presented. Two next words carry the L1 Accept or event number, and, finally, the fourth word is the bunch crossing counter reading for the first data block in the event. The header carries a specific signature of hexadecimal 0xF values to facilitate the separation of events. The data block format exactly follows the MPC-SP link format.

Table 105: DAT_DF Data Format for the FRONT_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word	Block
0xF				0xF				BC# – # of Bunch Crossings in Event								HD1	Header
0xF				EC [11:0] – Event Counter 12 Less Significant Bits												HD2	
0xF				EC [23:12] – Event Counter 12 Most Significant Bits												HD3	
0xF				BC [11:0] – Bunch Crossing Counter value for data block 1												HD4	
VP	Quality [3:0]			CLCT Pattern # [3:0]				Wire Group ID [6:0]								M1FR1	Data Block 1
CSC ID [3:0]			BC0	BX0	SE	L/R		CLCT Pattern ID [7:0]								M1FR2	
VP	Quality [3:0]			CLCT Pattern # [3:0]				Wire Group ID [6:0]								M2FR1	
CSC ID [3:0]			BC0	BX0	SE	L/R		CLCT Pattern ID [7:0]								M2FR2	
VP	Quality [3:0]			CLCT Pattern # [3:0]				Wire Group ID [6:0]								M3FR1	
CSC ID [3:0]			BC0	BX0	SE	L/R		CLCT Pattern ID [7:0]								M3FR2	

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Word	Block
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							M1FR1	Data Block BC#
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								M1FR2	
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							M2FR1	
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								M2FR2	
VP	Quality [3:0]				CLCT Pattern # [3:0]				Wire Group ID [6:0]							M3FR1	
CSC ID [3:0]				BC0	BX0	SE	L/R	CLCT Pattern ID [7:0]								M3FR2	

Here:

- VP – Valid Pattern flag
- Quality - the more hits the higher track Quality
- CLCT Pattern # - the 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit.
- Wire Group ID - the 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111.
- CSC ID - the 4-bit CSC ID indicates the chamber # and runs from 1 to 9.
- BC0 - the Bunch Crossing Zero flag marks bunch zero data
- BX0 - the least significant bit of Bunch Crossing Number (BXN ranges from 0 to 3563 in LHC mode and from 0 to 923 in SPS mode).
- SE - Synchronization Error bit
- L/R - the Left/Right bend bit indicates whether the track is heading towards lower or higher strip number
- CLCT Pattern ID - For high pT patterns, the 8-bit half-strip ID is between 0 and 159. For low pT patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber.

DAT_SFM – MS Spy FIFO Data

This read-only register in the SP_FPGA, one per output track, returns data from the MS Spy FIFO, which carries track ID, MS winner bits, and the PT LUT output. If the ID is non-zero, it shows the input stub number used by the SP core logic to build the output track. Although there is a DAT_SFM register for each output track, only one register at a time can be selected for spying on the PT LUT output data, refer to the CSR_SFC register descriptions for details.

Table 106: DAT_SFM Data Format for SP_FPGA

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Frame
0	MSW [2:0]			IDB1 [2:0]			ID4 [1:0]		ID3 [1:0]		ID2 [1:0]		ID1 [2:0]			FR1
Rear Muon PT LUT Data									Front Muon PT LUT Data							FR2

Here:

- MSW [2:0] = 0…3 – Muon Sorter Winner bits;
- For PT LUT Data format refer to the DAT_PT register description;
- For the ID to firmware muon correspondence see the table below.

Table 107: Spy FIFO to Muon ID Correspondence

Look for track stub into the Spy FIFO	Muon ID
SP/DAT_SF1/M1	ID1 = 1

SP/DAT_SF1/M2	ID1 = 2
SP/DAT_SF1/M3	ID1 = 3
SP/DAT_SF2/M1	ID1 = 4
SP/DAT_SF2/M2	ID1 = 5
SP/DAT_SF2/M3	ID1 = 6
SP/DAT_SF3/M1	ID2 = 1
SP/DAT_SF3/M2	ID2 = 2
SP/DAT_SF3/M3	ID2 = 3
SP/DAT_SF4/M1	ID3 = 1
SP/DAT_SF4/M2	ID3 = 2
SP/DAT_SF4/M3	ID3 = 3
SP/DAT_SF5/M1	ID4 = 1
SP/DAT_SF5/M2	ID4 = 2
SP/DAT_SF5/M3	ID4 = 3
SP/DAT_SFB/M1	IDB1 = 1
SP/DAT_SFB/M1 – next bx	IDB1 = 2
SP/DAT_SFB/M2	IDB1 = 3
SP/DAT_SFB/M2 – next bx	IDB1 = 4

DAT_RW – Data Transfer Bus Read/Write Register

This register is used for backplane and internal data bus validation. It allows write/read cycles to be performed to/from each FPGA chip without affecting SP02 functionality in any way.

Table 108: DAT_RW Data Format

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Validation Data Word															

History

Version 5.0 – Sep 01, 2003

1. Clock routing changed due to patches:
   - Eliminated the osc_clk input in the VME_FPGA;
   - Eliminated the clk_sel input in the VME_FPGA;
   - Returned two DCMs: internal and external to the VME_FPGA;
   - Eliminated the CSR_CLK register in the VME_FPGA;
   - Changed default value of the CSR_CLK register in the FRONT_FPGA from DCM to VCXO clock;
2. Changed the CCB_BC0 to DATA_BC0 adjustment scheme:
   - Eliminated the CSR_CCB register in the VME_FPGA;
   - Added the CSR_BCO register in the FRONT_FPGA (with the same access address);
   - Changed format of the CSR_OSY registers in the FRONT_FPGA, now it displays the latched bunch counter value without calculating positive/negative offsets;
3. Added data taking state diagrams in the interface description;
4. Added the STS_VPC (Valid Pattern Counter) register for each link in the FRONT_FPGA;

5. Renamed ACT_LER – Link Error Counters Resets to ACT_LCR – Link Counter Resets, added the VPR bit to reset the STS_VPC counter;
6. Fake L1Accept generated by CCB_TPxxx commands is ORed with the CCB_L1A line BEFORE the L1Accept delay, not AFTER;
7. Added intercept of the CCB_TPTMB(0x24) command;
8. Changed the CSR_SFC format in the VME_FPGA;

Version 5.1 – Nov 25, 2003

1. Changed the usage of the 39 and 3A access codes, Table 4. Previously identical data and program access is now split according to its function.
2. Changed the IDTB protocol from synchronous with a handshake to synchronous with a predetermined timing.
3. Added the CSR_BF(0x36) and DAT_BF(0x76) registers for the Barrel FIFO, Table 9;
4. Added the BF reset bit in the ACT_XFR, Table 20;
5. Added the ACT_ACR register description;
6. Changed the CSR_LF address from 0x36 to 0x37, Table 9;
7. Changed the CSR_RBW address from 0x37 to 0x38, Table 9;
8. Changed the CSR_RBR address from 0x38 to 0x39, Table 9;
9. Eliminated the CNT_GEL/CNT_GEH/CNT_GPL/CNT_GPH registers description;
10. Added the CNT_GLL/CNT_GLH registers description.

Version 5.2 – Dec 10, 2003

1. Added the DAT_GP register description;
2. Added the DAT_DT register description;
3. Added the DAT_GE register description.

Version 5.3 – Dec 25, 2003

1. Added the CNT_PTL/CNT_PTH registers description;
2. Added the DAT_PT register description;
3. Modified the ACT_ACR register description;
4. Modified the CSR_AFD register description;
5. Added the CSR_TFC register description;
6. Completely redefined CSR_OSY for FRONT_FPGA.

Version 5.6 – Mar 8, 2004

1. Added the CSR_F1/CSR_F2/CSR_F3/CSR_F4/CSR_F5 registers description;
2. Added the DAT_F1/DAT_F2/DAT_F3/DAT_F4/DAT_F5 registers description;
3. Eliminated the STS_CCB register description;

4. Changed the STS_ANA register description;
5. Added the ACT_FCC register description;
6. Eliminated the ACT_TST register description, the ACT_FCC took over this register;
7. Added the CSR_FCM register description;
8. Changed the CSR_TFC register description;
9. Eliminated the CSR_L1D register description since this the CCB function;
10. Restricted access to DAT_LP, DAT_GP, DAT_DT, DAT_GE, DAT_PT, DAT_ETA, and CSR_SCC registers

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[i] CSC Track Finder Crate Specification, created by Mike Matveev and updated by Alex Madorsky, December 12, 2002; http://www.phys.ufl.edu/~madorsky/TrackFinder/TF_backplane_v4.doc
[ii] ANSI/VITA 1.1-1997, American National Standard for VME64 Extensions.