

Sector Processor Front FPGA Choice

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Summary

Current Sector Processor (SP2002) PCB layout assumes [1] that each Front FPGA services 3 input optical links. Below we will compare two options of having 2 and 3 input links per Front FPGA in terms of number of BlockRAMs and user I/Os required, as well as available packaging for Virex-E and Virtex-II families.

Front FPGA Functionality

The Front FPGA serves as an intermediate buffer between optical links and the main Sector Processor FPGA. It plays a role of the former Sector Receiver. There are several Front FPGAs in the SP2002, the exact number depends more on the available packages, rather than FPGA capacity. Each FPGA services a number of data streams, coming from the optical links. Every bunch crossing each link delivers from the MPC a muon stub formatted as two 16-bit words. Front FPGA:

- Resynchronizes incoming data to the SP2002 global clock;
- Aligns all links to the latest one;
- Demultiplexes data from 16-bit @ 80 MHz to the 32-bit @ 40 MHz format;
- Sends it to the external lookup memories for further processing;
- Stores incoming data in the pipeline FIFO, which is deep enough to compensate for L1Accept latency;
- Upon receiving L1A reloads pipeline FIFO output to the L1A DAQ FIFO;
- Reads out and sends the L1A DAQ FIFO output data to the Detector Dependent Unit (DDU) and, optionally, to the L1A Spy FIFO;
- Under VME control generates downloadable test patterns for simulating the MPC data streams and checking the main SP2002 FPGA algorithms;
- Gives the user full control over Finisar FTRJ-8519-1-2.5 and Texas Instruments TLK2501 transceivers;
- Allows error analysis for each link;
- Provides fast monitoring information;
- Provides access for loading external lookup memories.

Front FPGA uses Block RAMs to implement FIFOs. Table 1 summarizes the Block RAM usage by each Front FPGA. This number imposes a first constraint on the FPGA choice. The applicable candidates are XCV50E/XCV100E and bigger from the Virtex-E family (see Table 2) and XC2V250 and bigger from the Virtex-II family (see Table 3).

Table 1 Block RAM count

Item	Width	Depth	# of Block RAMs per Link	# of Block RAMs per 2 Links	# of Block RAMs per 3 Links
Alignment FIFO	16	63	1	2	3
Pipeline FIFO	16	512	2	4	6
L1 DAQ FIFO	16	256	1	2	3
Stub Spy FIFO, optional	16	256	1	2	3
Test Pattern FIFO	16	256	1	2	3
Total			6	12	18

Table 2 Virtex-E Devices Summary – 1.8V

	System Gates	Row x Col	Slices	Distrib RAM Kbits		SRAM 4-Kbit Blocks	DLLs	Max I/O Pads
XCV50E	70K	16 x 24	1,536	24		16	8	176
XCV100E	120K	20 x 30	2,400	38		20	8	196
XCV200E	300K	28 x 42	4,704	74		28	8	284
XCV300E	400K	32 x 48	6,144	96		32	8	316
XCV400E	500K	40 x 60	9,600	150		40	8	404
XCV600E	1M	48 x 72	13,824	216		72	8	512
XCV1000E	1.5M	64 x 96	24,576	384		96	8	660
XCV1600E	2M	72 x 108	31,104	486		144	8	724
XCV2000E	2.5M	80 x 120	38,400	600		160	8	804
XCV2600E	3M	92 x 138	50,784	794		183	8	804
XCV3200E	4M	104 x 156	64,896	1014		208	8	804

Table 3 Virtex-II Devices Summary – 1.5V

	System Gates	Row x Col	Slices	Distrib RAM Kbits	Multiplier Blocks	SRAM 18-Kbit Blocks	DCMs	Max I/O Pads
XC2V40	40K	8 x 8	256	8	4	4	4	88
XC2V80	80K	16 x 8	512	16	8	8	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	12	1,108

Another constrain emerges from the number of I/O pins required to route all necessary FPGA ins and outs. Figure 1 shows a muon processing logic of the receiver part of the module. All data paths are marked in blue, addresses in green, controls in red and statuses in pink. Dashed area applies to A-layer muons only. Table 4 brings up details, when each Front FPGA services 3 links (3 muons), or 2 links (2 muons) per Front FPGA.

Signals in the tables are grouped per function, group names highlighted in bold. For example, first group is composed of the VME interface signals and includes the VME

data, VME Address, and VME control (Chip Select and Write Enable) signals. Only one control signal and one status-monitoring signal are required for the Finisar Optical Transmitter. More signals are needed to control and monitor the TI TLK2501 behavior. In fact, only transmit and receive data paths for one muon consume as many as 32 I/O pins. Note that Finisar and TI use different supply voltages that assume using of different output FPGA banks when connecting to these devices.

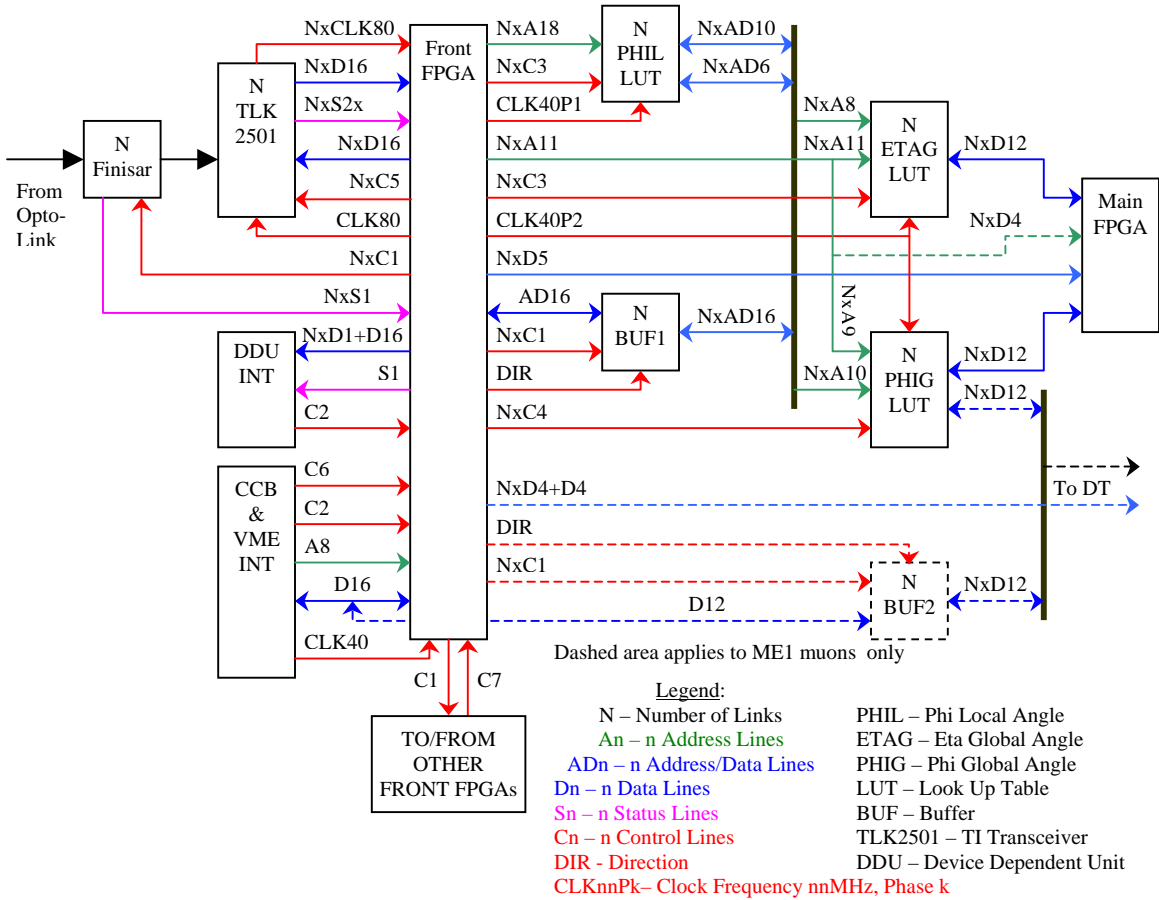


Figure 1 Sector Receiver, Muon processing logic

Table 4 Front FPGA I/O Count

Signal Name	Power or Dir	Bits	2 Links		3 Links		Comment
			Grps	Sum	Grps	Sum	
VME Interface							
VM_D	I/O	16	1	16	1	16	VME Data
VM_A	I	7	1	7	1	7	VME Subaddress Space [A7:A1]
/VM_WR	I	1	1	1	1	1	Write Enable (AL-Active Low)
/VM_CE	I	1	1	1	1	1	Chip Select (AL)
Subtotal		25		25		25	

Signal Name	Power or Dir	Bits	2 Links		3 Links		Comment
			Grps	Sum	Grps	Sum	
FINISAR	3.3V						
FI_SD	I	1	2	2	3	3	Signal Detect
FI_TD	O	1	2	2	3	3	Transmitter Disable
Subtotal		2		4		6	
TI TLK2501	2.5V						
TI_GTX_CLK80	O	1	1	1	1	1	Reference Clock
TI_ENABLE	O	1	2	2	3	3	Normal /Power Down Mode
TI_LOOPEN	O	1	2	2	3	3	Loop Enable
TI_PRBSEN	O	1	2	2	3	3	Pseudorandom Bit Stream
TI_TX_EN	O	1	2	2	3	3	Transmit Enable
TI_TX_ER	O	1	2	2	3	3	Transmit Error Coding
TI_TXD	O	16	2	32	3	48	Transmit Data
TI_RX_DV_ /LOS	I	1	2	2	3	3	Receive Data Valid /Loss of Synch
TI_RX_ER_ /PRBS_PASS	I	1	2	2	3	3	Receive Error /PRBS Test Pass
TI_RX_CLK80	I	1	2	2	3	3	Receive Clock
TI_RXD	I	16	2	32	3	48	Receive Data
Subtotal		41		81		121	
Local Phi LUT 256K x 18 GS841Z18A	2.5V or 3.3V						
LP_A	O	18	2	36	3	54	LUT Address
/LP_CE	O	1	2	2	3	3	Chip Enable (AL)
/LP_OE	O	1	2	2	3	3	Output Enable (AL)
/LP_WE	O	1	2	2	3	3	Write Enable (AL)
LP_CLK40	O	1	1	1	1	1	Clock40, Phase 0
Subtotal		22		43		64	
Global Phi LUT 512K x 36 GS8161Z36A	2.5V or 3.3V						
/GP_CE	O	1	2	2	3	3	Chip Enable (AL)
/GP_OE	O	1	2	2	3	3	Output Enable (AL)
/GPH_WE	O	1	2	2	3	3	High Bytes Write Enable (AL)
/GPL_WE	O	1	2	2	3	3	Low Bytes Write Enable (AL)
GP_CLK40	O	1	1	1	1	1	Clock40, Phase 180
Subtotal		5		9		13	
Global Eta LUT 512K x 18 GS881Z18A	1.8V or 2.5V						
GE_A	O	11	2	22	3	33	LUT Address
/GE_CE	O	1	2	2	3	3	Chip Enable (AL)

Signal Name	Power or Dir	Bits	2 Links		3 Links		Comment
			Grps	Sum	Grps	Sum	
/GE_OE	O	1	2	2	3	3	Output Enable (AL)
/GE_WE	O	1	2	2	3	3	Write Enable (AL)
Subtotal		14		28		42	
Buffer_1							
BUF_D	O	16	1	16	1	16	LUT Address
/BUF_OE	O	1	2	2	3	3	Chip Enable (AL)
/BUF_DIR	O	1	1	1	1	1	Output Enable (AL)
Subtotal		18		19		20	
Buffer_2							
/BUF_OE	O	1	2	2	3	3	Chip Enable (AL)
/BUF_DIR	O	1	1	1	1	1	Output Enable (AL)
Subtotal		2		3		4	
Main FPGA Data							
SP_D	O	5	2	10	3	15	Valid Pattern, Quality[3:0]
Subtotal		5		10		15	
Alignment FIFO							
/AF_WR	I	1	7	7	4	4	Alignment FIFO Write (AL)
/AF_RD	O	1	1	1	1	1	Alignment FIFO Read (AL)
Subtotal		2		8		5	
DDU Readout							
DDU_D	O	16	1	16	1	16	Readout Data
DDU_VP	O	1	2	2	3	3	Valid Pattern
DDU_RR	I	1	1	1	1	1	Readout Request
DDU_RA	O	1	1	1	1	1	Request Acknowledge
DDU_ST	O	1	1	1	1	1	Readout Start
Subtotal		20		21		22	
Fast Control							
CCB_CLK40	I	1	1	1	1	1	Main Clock
CCB_BC0	I	1	1	1	1	1	Bunch Counter Zero
CCB_BCR	I	1	1	1	1	1	Bunch Counter Reset
CCB_TEST	I	1	1	1	1	1	Test Request
CCB_L1A	I	1	1	1	1	1	L1 Accept
CCB_SPARE	I	2	1	2	1	2	Reserved
Subtotal		7		7		7	
DT Interface							
DT_ETA	O	1	2	2	3	3	Region Flag -? Compute?
DT_Q	O	3	2	6	3	9	Quality -? Compute?
DT_BXN	O	2	1	2	1	2	2 LSB of BXN
DT_BC0	O	1	1	1	1	1	To Facilitate Alignment
DT_CLK40	O	1	1	1	1	1	Clock
Subtotal		8		12		16	
Fast Monitoring							
FM_OSY	O	1	1	1	1	1	Out of Synch

Signal Name	Power or Dir	Bits	2 Links		3 Links		Comment
			Grps	Sum	Grps	Sum	
FM_SPARE	O	1	1	1	1	1	Reserved
Subtotal		2		2		2	
Configuration							
CFG_DIN	I	1	1	1	1	1	Serial Input
CFG_DOUT	O	1	1	1	1	1	Serial Output
CFG_INIT	I/O	1	1	1	1	1	Delay Configuration
Subtotal		3		3		3	
TOTAL				275		365	

Link Interface

CSC Trigger Primitives are coming from the Muon Port Cards (MPC) to the SP2002 via optical links. It has been agreed with Rice University that both ends of the link are instrumented with the Finisar FTRJ-8519-1-2.5 Transceivers [2], running at 1.6 Gbit/Sec, which in turn are coupled with the TI TLK2501 Transceivers [3] to perform data serialization / deserialization. Refer to Figure 2 and Table 5 for details regarding the Finisar device.

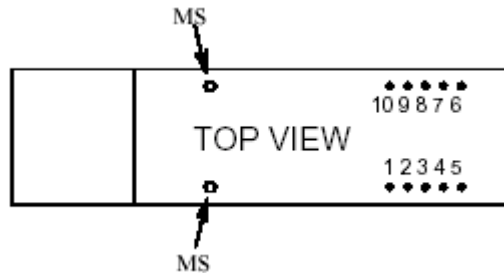


Figure 2 Finisar Transceiver Pin Layouts

Table 5 Finisar Transceiver Pin Assignments

Pin	Symbol	Name/Description	Logic Family
MS	MS	Mounting Studs for mechanical attachment. Internally connected to transceiver grounds. Connection to user's ground plane is recommended.	
1	VEER	Receiver Ground (Common with Transmitter Ground)	GND
2	VCCR	Receiver Power Supply	3.3V
3	SD	Signal Detect. Logic 1 indicates normal operation.	LVTTTL
4	RD-	Receiver Inverted DATA out. AC Coupled	PECL Swing
5	RD+	Receiver Non-inverted DATA out. AC Coupled	PECL Swing
6	VCCT	Transmitter Power Supply	3.3V
7	VEET	Transmitter Ground (Common with Receiver Ground)	GND
8	TDIS	Transmitter Disable	LVTTTL
9	TD+	Transmitter Non-Inverted DATA in; 100-ohm termination between TD+ and TD-, AC Coupled thereafter.	PECL Swing
10	TD-	Transmitter Inverted DATA in. See TD+	PECL Swing

It is supposed that Front FPGA takes control over the Finisar TDIS pin and is capable of reading back the transmitter status, or the SD pin. Note that both signals are in LVTTTL_33 logic levels.

Front FPGA has a full control over the TLK2501 device as well. Detailed description of the TLK2501 signals can be found in [3], or in Table 6 below.

Table 6 Texas Instruments TLK2501 Control and Status

TLK2501 Control / Status	Description	Comment
ENB=ENABLE	Normal / Power Down Mode	W/R
LEN=LOOPEN	Loop Enable (test)	W/R
PEN=PRBSEN	PseudoRandom Bit Stream	W/R
TEN=TX_EN	Transmit Enable	W/R
TER=TX_ER	Transmit Error Coding	W/R
RDV=RX_DV/LOS	Receive Data Valid / Loss of Synch	R only
RER=RX_ER/PRBS_PASS	Receive Error / PRBS Test Pass	R only

DDU Interface

Each Front FPGA delivers data to the 16-bit data bus on request of the readout logic. Readout Start prepares internal FPGA data, sitting in the L1A DAQ FIFO for readout. All Front FPGAs output pattern of “Valid Pattern” bits to the DDU interface, so it could put it as a first word of the Input Block [4]. Then readout proceeds by exchanging the Readout Request – Request Acknowledge handshake with each Front FPGA in turn.

Alignment FIFO

The Alignment FIFO Control group ensures carrying out the alignment procedure over all 15 CSC input links. One of the input FPGAs plays role of a master during the alignment procedure [5]. It collects write enable (/AF_WR) statuses from all of the Front FPGA chips, synchronizes it to the FIFO read clock and distributes a read enable (/AF_RD) signal back to FPGAs. All Front FPGAs begin simultaneously delivering first bunch-crossing data to their outputs.

CCB & VME Interface

The CCB interface provides a means of the TTC and VME control over the Front FPGA. All TTC timing signals including the master CLK40, BC0, BCR, and L1A are delivered from the CCB/VME FPGA. A few spare lines are foreseen for future developments. The VME control over Front FPGA assumes that each Front FPGA occupies space no more than 256 (0x100) byte (D8) addresses or 128 short word (D16) addresses. Table 7 shows an example of the Front FPGA address assignments in case of 2 input links per chip.

Basically, there are three groups of VME addresses in the Front FPGA:

- Addresses, servicing individual input data streams, like Link Control/Status, Link Error Counter, Alignment FIFO Status, Test Pattern FIFO Status/Data, etc.
- Addresses, servicing all data stream in the same FPGA, like L1 Pipeline FIFO Depth, and L1A DAQ FIFO Status.

- Address common to all links, like Alignment FIFO offset, which is located only in one of the Front FPGAs. Front FPGA, which owns this address acts as a master with respect to all other Front FPGAs during alignment procedure.

Table 7 Front FPGA VME Access

Offset	Description	Bits	Wrds	Blks	Comment
0x00	1 st Link Control/Status	16	1	-	See Table 9 for details
0x02	1 st Link Error Counter	16	1	-	See Table 10 for details
0x04	1 st Alignment FIFO Status	8+2	1	-	See Table 11 for details
0x06	1 st Test Pattern FIFO Status	8+2	1	-	See Table 12 for details
0x08	1 st Test Pattern FIFO	16	256	2	
0x10	1 st Local Phi LUT Address High	2	1	-	See Table 13 for details
0x12	1 st Local Phi LUT Address Low	16	1	-	
0x16	1 st Local Phi LUT Data	16	256K	2K	Local Phi LUT Data
0x20	1 st Global Phi LUT Address High	4	1	-	See Table 14 for details
0x22	1 st Global Phi LUT Address Low	16	1	-	
0x24	1 st Global Phi LUT Data High	16	1M	8K	
0x26	1 st Global Phi LUT Data Low	16	1M	8K	
0x30	1 st Global Eta LUT Address High	4	1	-	See Table 15 for details
0x32	1 st Global Eta LUT Address Low	16	1	-	
0x36	1 st Global Eta LUT Data	16	1M	8K	
0x40	2 nd Link Control/Status	16	1	-	See Table 9 for details
0x42	2 nd Link Error Counter	16	1	-	See Table 10 for details
0x44	2 nd Alignment FIFO Status	8+2	1	-	See Table 11 for details
0x46	2 nd Test Pattern FIFO Status	8+2	1	-	See Table 12 for details
0x48	2 nd Test Pattern FIFO	16	256	2	
0x50	2 nd Local Phi LUT Address High	1	1	-	See Table 13 for details
0x52	2 nd Local Phi LUT Address Low	16	1	-	
0x56	2 nd Local Phi LUT Data	16	256K	2K	Local Phi LUT Data
0x60	2 nd Global Phi LUT Address High	3	1	-	See Table 14 for details
0x62	2 nd Global Phi LUT Address Low	16	1	-	
0x64	2 nd Global Phi LUT Data High	16	1M	8K	
0x66	2 nd Global Phi LUT Data Low	16	1M	8K	
0x70	2 nd Global Eta LUT Address High	3	1	-	See Table 15 for details
0x72	2 nd Global Eta LUT Address Low	16	1	-	
0x76	2 nd Global Eta LUT Data	16	1M	8K	
0x80	3rd Link Control/Status	16	1	-	See Table 9 for details
0x82	3rd Link Error Counter	16	1	-	See Table 10 for details
0x84	3rd Alignment FIFO Status	8+2	1	-	See Table 11 for details
0x86	3rd Test Pattern FIFO Status	8+2	1	-	See Table 12 for details
0x88	3rd Test Pattern FIFO	16	256	2	
0x90	3rd Local Phi LUT Address High	1	1	-	See Table 13 for details
0x92	3rd Local Phi LUT Address Low	16	1	-	
0x96	3rd Local Phi LUT Data	16	256K	2K	Local Phi LUT Data
0xA0	3rd Global Phi LUT Address High	3	1	-	See Table 14 for details
0xA2	3rd Global Phi LUT Address Low	16	1	-	
0xA4	3rd Global Phi LUT Data High	16	1M	8K	
0xA6	3rd Global Phi LUT Data Low	16	1M	8K	
0xB0	3rd Global Eta LUT Address High	3	1	-	See Table 15 for details
0xB2	3rd Global Eta LUT Address Low	16	1	-	
0xB6	3rd Global Eta LUT Data	16	1M	8K	

Offset	Description	Bits	Wrds	Blks	Comment
0xC0	1-2 Pipeline FIFO Depth/Status	9+2	1	-	See Table 16 for details
0xC8	1-2 L1A DAQ FIFO Status	8+2	1		See Table 17 for details
0xE0	Alignment FIFO Offset	5	1	-	See Table 18 for details Applicable for middle FPGA only

All transceiver’s control signals are writable / readable and all status signals are readable only over the VME interface by addressing the Front FPGA internal registers, see Table 8 and Table 9 below.

The TLK2501 synchronization procedure [5], when both RX_DV and RX_ER have been dropped LOW for at least three RX_CLK periods – IDLE state, always precedes the normal operation. Normal operation assumes SD and RX_DV to be HIGH and RX_ER to be LOW. To facilitate monitoring of error conditions, any combination of SD, RX_DV and RX_ER other than normal is detected and latched, Table 9. Latched statuses are accumulated over time, starting from the previous synchronization procedure. There is a 10-bit error counter for a detailed analysis of link errors, Table 10, which can be tuned to count either number of error words received, or carrier extend characters, or both.

Table 8 Finisar and TI Transceivers Latched Statuses and Error Counter Controls

Latched Status/ Error Counter Control	SD	RX_DV	RX_ER	Description
LLS=Latched Loss of SD	LOW	Any	Any	Latched Loss of Signal Detect
LID=Latched IDLE	HIGH	LOW	LOW	Latched IDLE
LCE=Latched CE	HIGH	LOW	HIGH	Latched Carrier Extend
LER=Latched Error	HIGH	HIGH	HIGH	Latched Error Propagation
CCE=Count CE	HIGH	LOW	HIGH	Count Carrier Extend words
CER=Count Errors	HIGH	HIGH	HIGH	Count Error Words

Table 9 Link Control/Status Register Bit Assignments

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LID	LER	LCE	LSD		RER	RDV	SD			PEN	LEN	ENB	TER	TEN	TD
Link Statuses, R only								Link Controls, W/R							

There is a copy of Link Control/Status Register for each input link (2 or 3 per Front FPGA).

Table 10 Link Error Counter

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		CER	CCE			EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
Spare		W/R		Spare		Error Counter, R only									

There is a copy of Link Error Counter for each input link (2 or 3 per Front FPGA).

Table 11 Alignment FIFO Status Bit Assignments

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		AFF	AEF					Spare		AC5	AC4	AC3	AC2	AC1	AC0
Spare		Flags, R		Spare				Alignment FIFO Word Count, R only							

There is a copy of an Alignment FIFO Status for each input link (2 or 3 per Front FPGA).

Table 12 Test FIFO Status Bit Assignments

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		TFF	TEF					TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0
Spare		Flags, R		Spare				Test FIFO Word Count, R only							

There is a copy of a Test FIFO Status for each input link (2 or 3 per Front FPGA).

Table 13 Local Phi LUT Address

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hi															LP17	LP16
Lo	LP15	LP14	LP13	LP12	LP11	LP10	LP9	LP8	LP7	LP6	LP5	LP4	LP3	LP2	LP1	LP0
Local Phi Address, W/R																

Muon processing logic provides both downloading and reading back capabilities for all LUTs, including DT LUTs for A-layer muons. Extra buffers BUF1 and BUF2 are needed to provide an address/data path to nets running between two LUTs, and going nowhere else.

There is a copy of a Local Phi Address Register for each input link (2 or 3 per Front FPGA). To fill out the LUT – 256K x 16 SRAM, user has to load the Hi Address Register first, followed by loading the Lo Address Register and LUT data. Loading one 16-bit data word increases the Local Phi Address Register by 1.

Table 14 Global Phi LUT Address (VME FPGA)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hi														GP18	GP17	GP16
Lo	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0
Global Phi Address, W/R																

There is a copy of a Global Phi Address (GPA) Register for each input link, 15 in total. To fill out the LUT – 512K x 32 SRAM, user has to load the Hi Address Register first, followed by loading the Lo Address Register and LUT data. Loading one 16-bit data word increases the Global Phi Address Register by 1. Loading Hi and/or Lo 16-bit words are independent processes. Basically for the user, the 512K x 32 SRAM behaves like two 512K x 16 SRAMs with a common address counter. While the Front FPGA provides for all LUT control signals, either main FPGA or BUF2 provides for data.

Table 15 Global Eta LUT Address (VME FPGA)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hi														GE18	GE17	GE16
Lo	GE15	GE14	GE13	GE12	GE11	GE10	GE9	GE8	GE7	GE6	GE5	GE4	GE3	GE2	GE1	GE0
Global Phi Address, W/R																

There is a copy of a Global Eta Address (GEA) Register for each input link, 15 in total. To fill out the LUT, user has to load the Hi Address Register first, followed by loading the Lo Address Register and LUT data. Loading one 16-bit data word increases the Global Eta Address Register by 1. While the Front FPGA provides for all LUT control signals, the main FPGA provides for data.

Table 16 Pipeline FIFO Control/Status Bit Assignments

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		PEF	PEF				PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Spare		Flags, R		Spare			L1 Pipeline FIFO Depth, W/R								

Pipeline FIFO is (16*3 = 48)-bit wide and services simultaneously three links. There is just one copy of the Pipeline FIFO Control/Status for each Front FPGA. The user has to download the same FIFO Depth parameter for all 8 Front FPGAs.

Table 17 L1A DAQ FIFO Status Bit Assignments

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		DFE	DFE					DC7	DC6	DC5	DC4	DC3	DC2	DC1	DC0
Spare		Flags, R		Spare			L1A DAQ FIFO Word Count, R only								

L1A DAQ FIFO is (16*3 = 48)-bit wide and services simultaneously two links. There is just one copy of L1A DAQ FIFO Status for each Front FPGA.

Table 18 CSC Offset Register Bit Assignments

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											CO4	CO3	CO2	CO1	CO0
												CSC Offset, W/R			

There is just one copy of CSC Offset Register, located in the middle Front FPGA. This offset allows aligning CSC muon data with barrel data, if necessary.

Finally, Table 19 presents a Base address, assigned to each Front FPGA in the SP2002.

Table 19 Front FPGA Base Addresses

Front FPGA #	Base Address	Comment
1	0x0100	2 or 3 links per FPGA
2	0x0200	2 or 3 links per FPGA
3	0x0300	2 or 3 links per FPGA
4	0x0400	2 or 3 links per FPGA
5	0x0500	2 or 3 links per FPGA
6	0x0600	3 links per FPGA
7	0x0700	3 links per FPGA
8	0x0800	3 links per FPGA

FPGA Choice

In summary, the number of required I/Os comes to **365** in case of 3 links per chip, and to **275** in case of 2 links per Front FPGA. Note, that this number tends to increase as the design progresses, and never to decrease. For example, we may want to use a parallel or SelectMAP configuration option instead of Serial, which immediately would increase

the number of required user I/O pins by 11. We probably would also like to keep the user I/O utilization level below 90 percent to maintain some flexibility in design development. So, the best Virtex-E candidate is an XCV300E device in FG456 package for 2 muons per FPGA and an XCV400E device in FG676 package for 3 muons per FPGA. Choice amongst Virtex-II candidates leads to an XC2V1000 device in FG456 package, and the same device in FF896 package accordingly, see Table 20 thru Table 22. Figure 3, Figure 4, and Figure 5 show scaled images of the packages.

Table 20 Virtex-E, Virtex-II Packages Information

Package	Pitch	Size	Package	Pitch	Size	Package	Pitch	Size
CS144	0.80	12 x 12						
PQ240	0.50	32 x 32				FG256	1.00	17 x 17
BG256	1.27	27 x 27				FG456	1.00	23 x 23
BG352	1.27	35 x 35				FG676	1.00	27 x 27
BG432	1.27	40 x 40				FG680	1.00	40 x 40
BG560	1.27	42.5 x 42.5				FG860	1.00	42.5 x 42.5
BG575	1.27	31 x 31	FF896	1.00	31 x 31	FG900	1.00	31 x 31
BG728	1.27	35 x 35	FF1152	1.00	35 x 35	FG1156	1.00	35 x 35
BF957	1.27	40 x 40	FF1517	1.00	40 x 40			

Table 21 Virtex-E Device/Package Combinations and Maximum Number of Available I/Os

Package	Virtex-E Available I/Os										
	XCV 50E	XCV 100E	XCV 200E	XCV 300E	XCV 400E	XCV 600E	XCV 1000E	XCV 1600E	XCV 2000E	XCV 2600E	XCV 3200E
CS144	94	94	94								
PQ240	158	158	158	158	158						
HQ240						158	158				
BG352		196	260	260							
BG432				316	316	316					
BG560					404	404	404	404	404		
FG256	176	176	176	176							
FG456			284	312							
FG676					404	444					
FG680						512	512	512	512		
FG860							660	660	660		
FG900						512	660	700			
FG1156							660	724	804	804	804

Table 22 Virtex-II Device/Package Combinations and Maximum Number of Available I/Os

Package	Virtex-II Available I/Os											
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000	
CS144	88	92	92									
FG256	88	120	172	172	172							
FG456			200	264	324							
FG676						392	456	484				
FF896					432	528	624					
FF1152								720	824	824	824	
FF1517									912	1104	1108	
BG575					328	392	408					
BG728							456	516				
BF957							624	684	684	684	684	

All devices in a particular package are pin-out (footprint) compatible. In addition, the FG456 and FG676 packages are compatible, as are the FF896 and FF1152 packages.



Figure 3 Fine Pitch BGA (FG456) Package, 23 x 23 mm, Scale 1:1

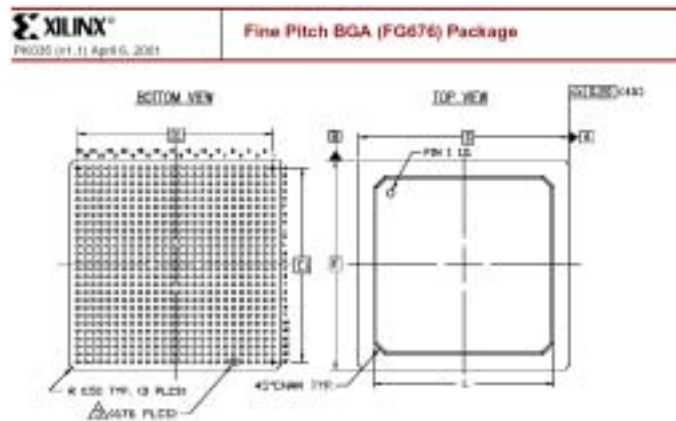


Figure 4 Flip-Chip BGA (FG676) Package, 27 x 27 mm, Scale 1:1

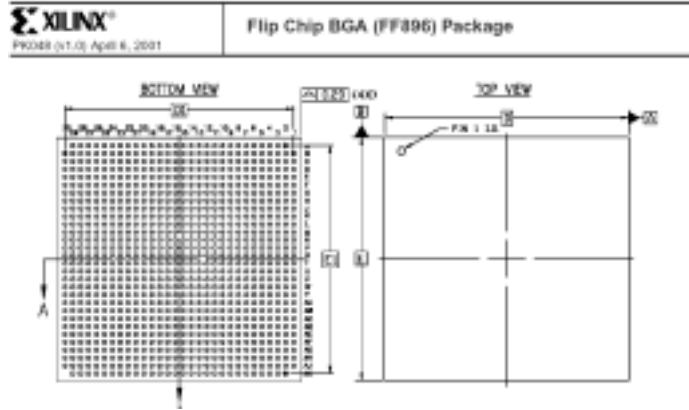


Figure 5 Flip-Chip BGA (FF896) Package, 31 x 31 mm, Scale 1:1

We suggest staying with the option of having 3 muons per Front FPGA and using XC2V1000 devices in FF896 packages. The PCB routing would require at least 4 signal and 3 plane layers. Overwhelming majority of user I/Os will be using LVTTTL_25 I/O standard with at least one I/O bank using LVTTTL_33 I/O standard. Table 23 gives reference prices for XC2V1000 devices.

Table 23 Reference Prices for XC2V1000 Devices

Device	Reference Price
XC2V1000-4FF896C	\$397.00
XC2V1000-5FF896C	\$556.00

A separate FPGA chip will service the DDU interface.

Table 24 Revision Histories

Date	Revision #	What's new
February 19, 2002	Initial Proposal	
March 14, 2002	Rev 1.0	Figure 1, Changed ETAG LUT output from NxD11 to NxD12 Figure 1, Changed text label from "A-Layer" to "ME1" Figure 1, Added NxD4 datapath to Main FPGA for ME1 muons

[1] CSC Track-Finder Update, D.Acosta's Presentation at UCLA, Dec. 2001;
at http://www.phys.ufl.edu/~acosta/cms/srsp_dec01.pdf

[2] Finisar FTRJ-8519-1-2.5 2x5 Pin SFF Product Specification, July 2000.

[3] Texas Instruments SLLS427A – TLK2501 1.6 to 2.5 GBPS Transceiver, Aug 2000, revised Oct 2000.

[4] Sector Processor - DDU Interface,
at http://red.pnpi.spb.ru/~uvarov/uf_crate/LU-SP_DDU_Interface.pdf

[5] MPC – SP Synchronization Procedure,
at http://red.pnpi.spb.ru/~uvarov/uf_crate/LU-MPC_SP_Synch_Procedure_Ver1d1.pdf