

Sector Processor Main FPGA Choice

Petersburg Nuclear Physics Institute / University of Florida

Rev 1.0

March 14, 2002

Summary

Main FPGA choice is discussed in detail. Table 1 summarizes the chip I/O usage. It also counts the required number of signal pins for mezzanine card connectors. The appropriate candidates appear to be Virtex II XC2V3000 or bigger devices into FF1152 packages. The total number of mezzanine card connector pins exceeds the current mezzanine card design by almost 150 and reaches almost 730. It is very unlikely that ALCT and SP could share the same mezzanine card.

Main FPGA Functionality

Main FPGA of the SP2002 prototype performs reconstruction of complete tracks from individual track segments delivered to it from both Endcup Muon (EMU) CSC chambers over front panel optical links and Front FPGAs and Barrel Drift Tubes (DT) over Transition board, see Figure 1. Whereas EMU track segments are already aligned in time into the Front FPGAs, DT track segments still need to be aligned into the Main FPGA.

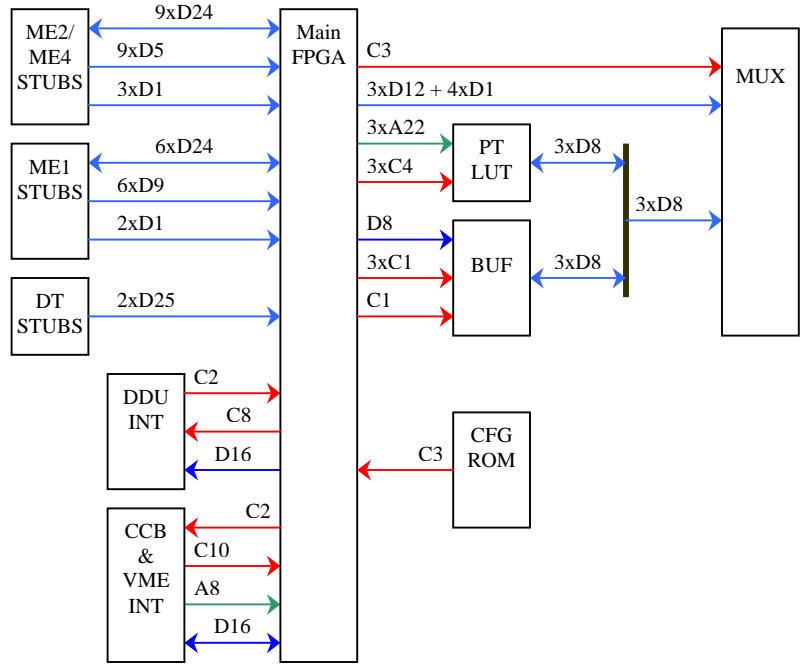
The CCB and VME interface provides VME access to the Main FPGA chip, as well as delivers timing control signals from the CCB. The DDU interface ensures collecting of DT track segments and reconstructed tracks into the event frame on the L1A request. The Main FPGA drives address and control lines of PT LUTs. It also allows loading PT LUTs with data using an additional buffer, which provides a data path to the LUT I/Os.

PT LUT is a 4Mx8 Static RAM (SRAM) implemented either as two Toshiba 4Mx4 TC55V4400FT devices, or as two Toshiba 2Mx8 TC55V8200FT devices with access time of 10-15 ns.

Each bunch crossing the SP2002 sends to the Muon Sorter (MS) 64 bits of data at a double rate of 80 MHz, organized in two 32-bit frames, Figure 2. LVTTTL/GTLP translators are Fairchild GTLP16617 devices and feature synchronous output enable, allowing clean wired multiplexing on their outputs. Other features include:

- Medium drive GTLP capability of 50 mA;
- Flow-through pinout;
- 6.7/8.7ns CLKAB to B-out maximum delay.

In each GTLP16617 transceiver internal triggers sample A-inputs at 80MHz, but only every other sample reaches the transceiver output. Which one succeeds is determined by the CLK40-90 and CLK40-270 signals applied to the /OEAB transceiver enable inputs.

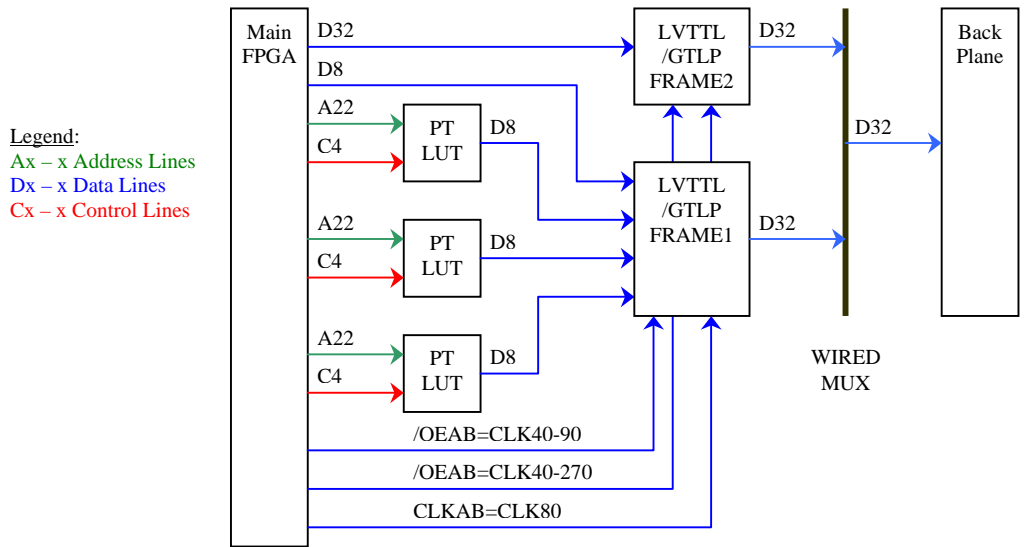


Legend:

- G – Number of Signal Groups
- GxA_n – G Groups of n Address Lines
- GxC_n – G Groups of n Control Lines
- GxD_n – G Groups of n Data Lines

- CCB & VME INT – Combined CCB and VME Interface
- BUF – Buffer
- PT LUT – PT Assignment Look Up Table
- CFG ROM – Configuration EEPROM
- DDU INT – Readout Interface
- ME1 STUBS – ME1 CSC Track Segments
- ME2/ME4 STUBS – ME2, ME3, and ME4 CSC Track Segments
- DT STUBS – Drift Tube Track Segments
- MUX - Multiplexer

Figure 1 Sector Processor Main FPGA Dataflow



Legend:

- A_x – x Address Lines
- D_x – x Data Lines
- C_x – x Control Lines

Figure 2 PT LUT and Multiplexer Details

Table 1 Main FPGA I/O Count

Signal Name	Virtex-II I/O Pin Count				Connectors Pin Count	Comment
	Dir	Bits	Groups	Sum		
VME Interface	3.3V					
VM_D	I/O	16	1	16	16	VME Data
VM_A	I	12	1	12	12	VME Subaddress Space [A8:A1]
/VM_WR	I	1	1	1	1	Write Enable (AL-Active Low)
/VM_CE	I	1	1	1	1	Chip Select (AL)
Subtotal		30		30	30	
ME2-ME4 Muons	3.3V or 2.5V					
CSC_VP	I	1	9	9	9	Valid Pattern
CSC_Q	I	4	9	36	36	Quality
CSC_PHI	I	12	9	108	108	Phi Azimuthal Angle
CSC_PHIB	I	5	9	45	45	Phi Bend Angle
CSC_ETA	I	7	9	63	63	Eta Global Angle
CSC_BC1	I	1	3	3	3	Bunch Crossing One, once per orbit
Subtotal		30		264	264	
ME1 Muons	3.3V or 2.5V					
CSC_VP	I	1	6	6	6	Valid Pattern
CSC_Q	I	4	6	24	24	Quality
CSC_PHI	I	12	6	72	72	Phi Azimuthal Angle
CSC_PHIB	I	5	6	30	30	Phi Bend Angle
CSC_ETA	I	7	6	42	42	Eta Global Angle
CSC_ID	I	4	6	24	24	CSC ID
CSC_BC1	I	1	2	2	2	Bunch Crossing One, once per orbit
Subtotal		34		200	200	
DT Muons	3.3V					
DT_Q	I	3	2	6	6	Quality
DT_PHI	I	12	2	24	24	Phi Azimuthal Angle
DT_PHIB	I	5	2	10	10	Phi Bend Angle
DT_BXN	I	2	2	4	4	Bunch Crossing
DT_Flag	I	1	2	2	2	Second Muon Flag
DT_Synch	I	1	2	2	2	Synchronization / Calibration
DT_CLK40	I	1	2	2	2	Clock40
Subtotal		25		50	50	
MS Mux	3.3V					
SP_PHI	O	5	3	15	15	Phi Azimuthal Angle
SP_ETA	O	5	3	15	15	Eta Angle
SP_HALO	O	1	3	3	3	Halo Muon Trigger

Signal Name	Virtex-II I/O Pin Count				Connectors Pin Count	Comment
	Dir	Bits	Groups	Sum		
SP_CHARGE	O	1	3	3	3	Muon Sign
SP_BXN	O	2	1	2	2	2 LSB of BXN
SP_ERROR	O	1	1	1	1	Error
SP_SPARE	O	1	1	1	1	Spare
MX_CLK	O	3	1	3	3	Mux Clocks
Subtotal		19		43	43	
SP to PT LUT 4M x 8 TC55V4400FT x 2	3.3V					
PT_DPFI	O	13	3	39	39	Delta Phi Azimuthal Angle
PT_SIGN	O	1	3	3	3	Sign
PT_ETA	O	4	3	12	12	Eta Angle
PT_MODE	O	4	3	12	12	Mode
/PT_CE	O	1	3	3	3	Chip Enable (AL)
/PT_WE	O	1	3	3	3	Write Enable (AL)
/PT_OE	O	2	3	6	6	Output Enable (AL)
Subtotal		26		78	78	
Buffer (for PT LUT loading)	3.3V					
BUF_D	O	8	1	8	8	Data
/BUF_OE	O	1	3	3	3	Chip Enable (AL)
/BUF_DIR	O	1	1	1	1	Output Enable (AL)
Subtotal				12	12	
DDU Readout	3.3V					
DDU_D	O	16	1	16	16	Readout Data
DDU_VP	O	1	4	4	4	Valid Pattern
DDU_RR	I	1	1	1	1	Readout Request
DDU_RA	O	1	1	1	1	Request Acknowledge
DDU_ST	I	1	1	1	1	Readout Start
DDU_RSVD	I/O	3	1	3	3	Readout Reserved
Subtotal		23		26	26	
Fast Control	3.3V					
CCB_CLK40	I	1	1	1	1	Main Clock
CCB_CLKEN	I	1	1	1	1	Clock Enable
CCB_BC0	I	1	1	1	1	Bunch Counter Zero
CCB_BCR	I	1	1	1	1	Bunch Counter Reset
CCB_TEST	I	1	1	1	1	Test Request
CCB_L1A	I	1	1	1	1	L1 Accept
CCB_SPARE	I	2	1	2	2	Reserved
Subtotal		8		8	8	
Fast Monitoring	3.3V					
FM_OSY	O	1	1	1	1	Out of Synch
FM_SPARE	O	1	1	1	1	Reserved
Subtotal		2		2	2	
Configuration	3.3V					

Signal Name	Virtex-II I/O Pin Count				Connectors Pin Count	Comment
	Dir	Bits	Groups	Sum		
CFG_M	I	3	1		3	Configuration Mode Bits
CFG_DIN	I	1	1	1	1	Serial Input
CFG_DOUT	O	1	1	1	1	Serial Output
CFG_INIT	I/O	1	1	1	1	Delay Configuration
CFG_CCLK	I	1	1		1	Configuration Clock
CFG_PROG_B	I	1	1		1	Hard Reset from CCB
CFG_DONE	I/O	1	1		1	Completion of Configuration
Subtotal		9		3	9	
JTAG Modes	3.3V					
CFG_TMS	I	1	1		1	Test Mode Select
CFG_TDO	O	1	1		1	Test Data Out
CFG_TDI	I	1	1		1	Test Data In
CFG_TCK	I	1	1		1	Test Clock
Subtotal				0	4	
TOTAL				716	726	XC2V3000-5FF1152C or bigger

The total number of required I/Os for Main SP2002 FPGA reaches 716. **Error! Not a valid bookmark self-reference.** gives us available number of user I/Os for each device/package combination of the Virtex-II FPGA series. The applicable candidates are devices in FF1152 package (highlighted in light green).

Table 2 Virtex-II Device/Package Combinations and Maximum Number of Available I/Os

Package	Virtex-II Available I/Os										
	XC2V 40	XC2V 80	XC2V 250	XC2V 500	XC2V 1000	XC2V 1500	XC2V 2000	XC2V 3000	XC2V 4000	XC2V 6000	XC2V 8000
CS144	88	92	92								
FG256	88	120	172	172	172						
FG456			200	264	324						
FG676						392	456	484			
FF896					432	528	624				
FF1152								720	824	824	824
FF1517									912	1104	1108
BG575					328	392	408				
BG728							456	516			
BF957							624	684	684	684	684

The smallest XC2V3000 device provides as many as 720 user I/Os, whereas XC2V4000 and bigger devices – 824 I/Os. The preliminary number of required user I/Os is very close to 720, and using the smallest device may become an obstacle for development as design progresses and request for more I/Os emerges.

Mezzanine Card Considerations

It is assumed that the Main FPGA chip is located on the mezzanine card, square in shape, which is stacked to the main board using 4 Samtec FOLC/MOLC connectors. The FOLC/MOLC interconnect system features 4-row of 2 mm pitch contacts, and up to 50 contacts per row. 200 contacts per connector, or 800 contacts in total give enough flexibility for SP2002 board routing.

Table 3 Revision Histories

Date	Revision #	What's new
February 26, 2002	Initial Proposal	
March 14, 2002	Rev 1.0	Figure 1 completely updated. EMU Muon box has been split into two boxes for ME2/ME4 and ME1 track segments respectively.