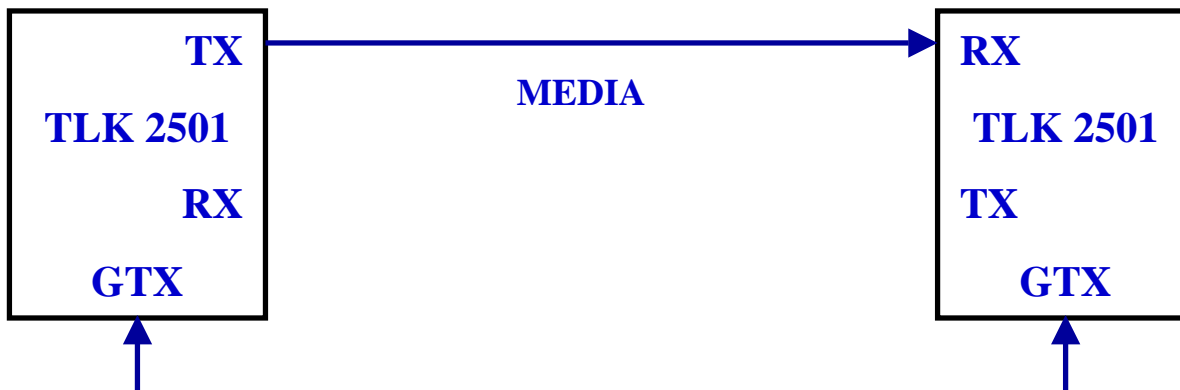




MPC-SP02 Jitter Budget

TI App note “Understanding Jitter and Bit Error for the TLK2500”



- We cannot allow more jitter in a system than the UI, which is 625 ps, or errors will result
- The transmitter is specified to consume **0.2 UI** of the budget under clean GTX (40 ps peak-to-peak) and power supply, and could be worse. GTX jitter above 5 MHz is filtered out, below – passes through.
- The receiver is specified to consume **0.50 UI** of the budget under clean GTX (40 ps peak-to-peak) and power supply.
- Media jitter comes from Finisar spec and is about **0.2 UI**.
- Remaining budget is about **0.1 UI** or 60 ps.

GTX allowed jitter should be very close to the required 40 ps peak-to-peak.

For reference: $PP = (6-14) * RMS$





Understanding Jitter and Bit Error

For example, a desired error rate of 1 bit error out of 10^{12} bits means that the random jitter components be measured as a peak-to-peak value out to 14 standard deviations.

Random jitter components throughout the system are added up by the sum-of-squares method, not linearly. This reflects the fact that if a random jitter event in the transmitter were to jitter a data bit out to the peak in one direction, it is unlikely that a random event in the fiber optic transceiver would also jitter the data bit out to the peak in the same direction at the same time.

If jitter events throughout a system are characterized as random and deterministic, then the total of the random jitter (added by sum of squares) is added to the total of the deterministic jitter (added linearly). This total jitter in the system must be less than the jitter budget. If the jitter budget is just met using peak-to-peak jitter measurements, assuming the peak-to-peak random jitter measurements contain all but 1 out of 10^{12} jitter events, then an error rate of 1 out of 10^{12} for the system can be expected.



TTCrx Jitter

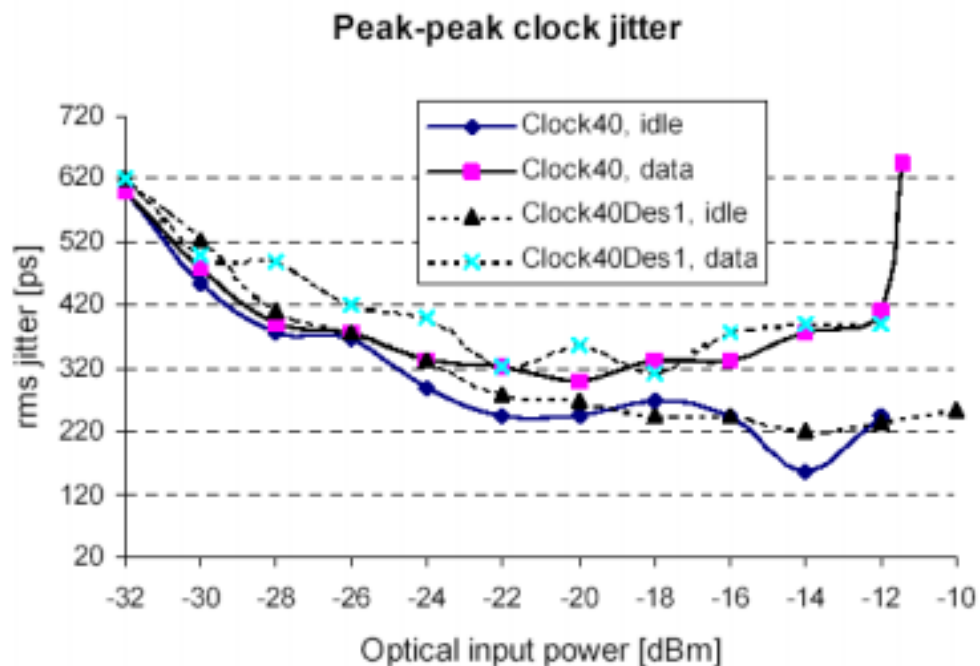


Figure 24 Peak to peak clock jitter versus input optical power.

TTCrx Reference Manual, ver 3.8:

Peak-to-peak jitter **PP \geq 350 ps**



TTCrx Jitter Continue

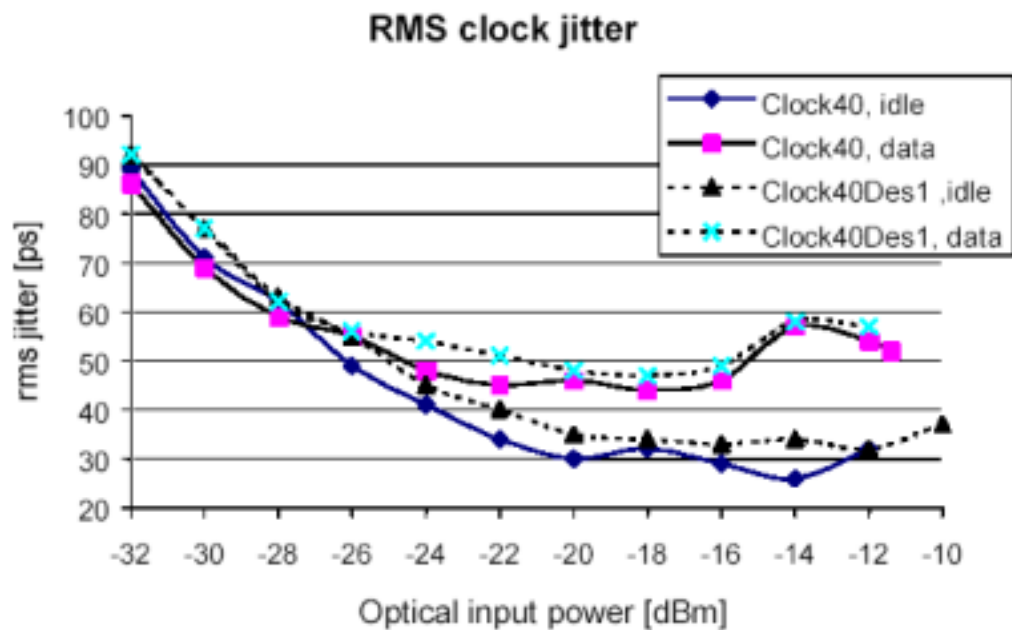


Figure 23 RMS Clock jitter versus input optical power.

TTCrx Reference Manual, ver 3.8:

RMS jitter \geq 50 ps





CCB Oscillator Jitter

Epson SG-8002 80.16 MHz PLL oscillator spec:

Peak-to-peak jitter **PP=250 ps**

Cycle-to-cycle jitter **CC=200 ps**

**Jitter of both clock sources is 6-9 times worse than
the TLK2501 GTX jitter requirement (40 ps)!**





MPC Jitter

ICS AV9170 Frequency Multiplier spec:

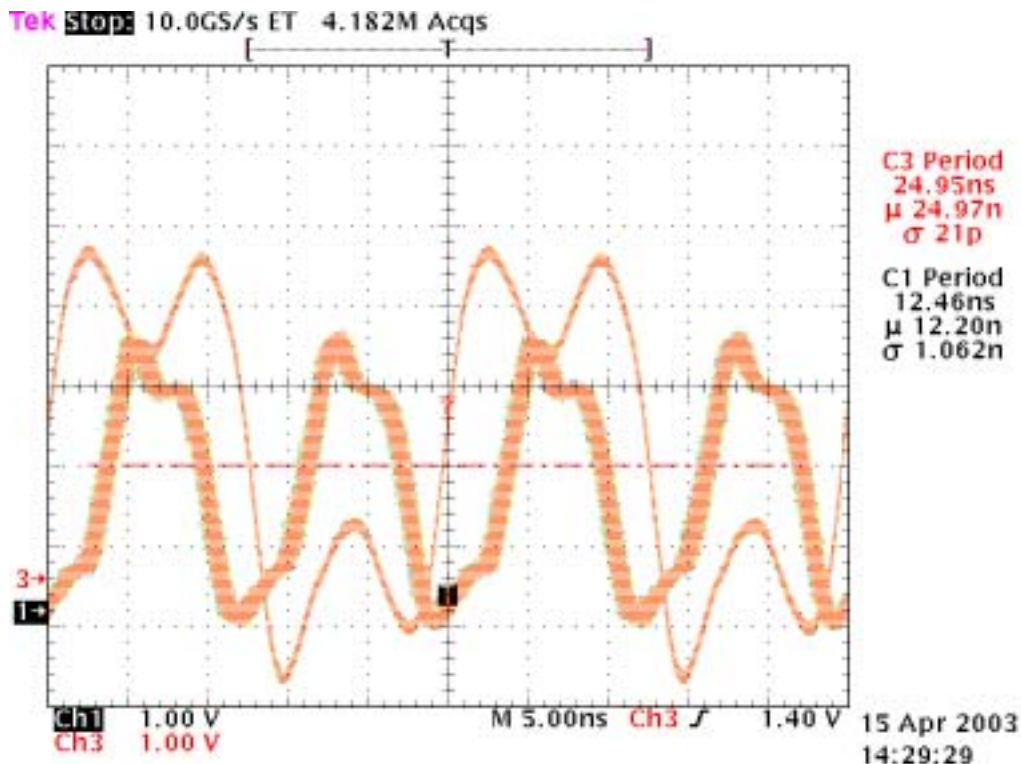
Jitter absolute PP = 1 000 ps ---?

Jitter sigma RMS = 300 ps

Multiplier may introduce A LOT of jitter to transmitter GTX clock!

C3 – 40MHz CCB Oscillator Clock (U38-5, TP27) - Trigger

C1 – 80 MHz MPC GTX Clock (U28-8)





SP02 Jitter

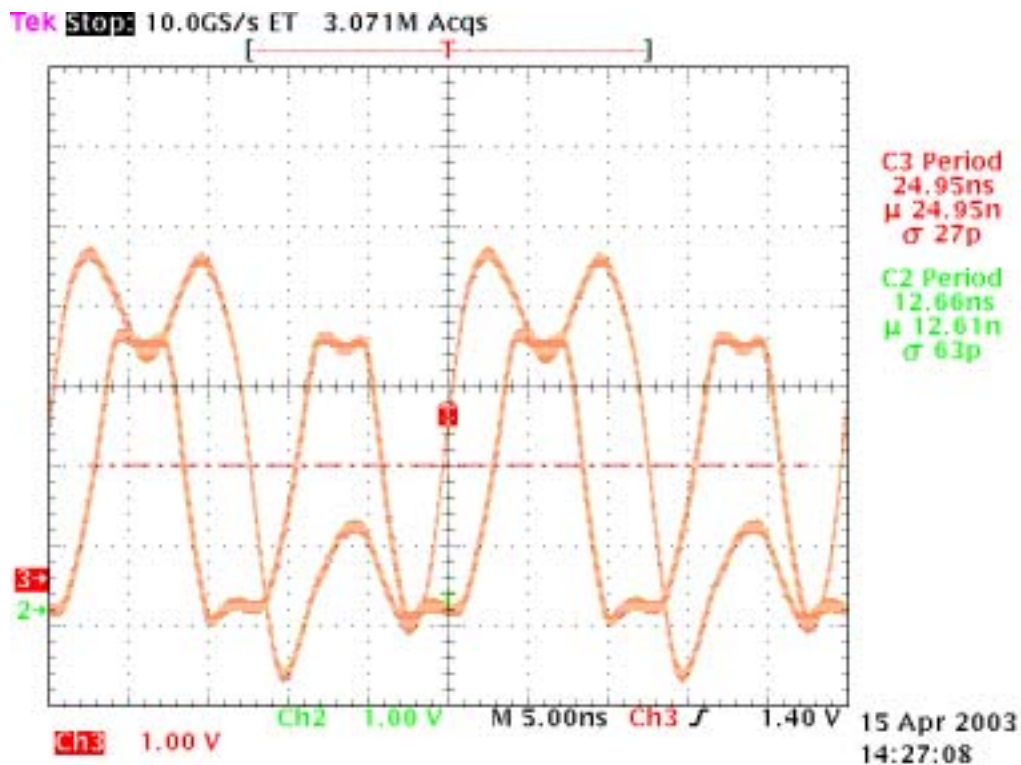
Virtex II DDL multiplier spec:

Peak-to-peak jitter = **400 ps**

DDL may introduce A LOT of jitter to receiver GTX clock!

C3 – 40MHz CCB Oscillator Clock (U38-5, TP27) – Trigger

C2 – 80 MHz SP02 GTX Clock (U165-8)





Link Tests

SP02 optical loopback PRBS test over 1 m cable

No errors

SP02 optical loopback PRBS test over 100 m cable

BER = 10^{-12}

Consistent with the jitter budget!

MPC-SP02 PRBS test over 100 m cable

BER = $3 * 10^{-13}$

Too good to be true

Expected much worse according to the jitter budget

No explanation yet





Conclusions

CCB Oscillator should be “Fibre Channel Compliant”

Example: CTS CB3LV SMD Clock Oscillator has RMS jitter ≤ 1 ps

MPC & SP Multiplier might be based on VCXO, running on fundamental frequency, which possibly could refine TTCrx clock

There are companies capable of producing such custom 80,157 MHz VCXO with very low jitter.

R&D on low jitter multiplier is needed





Post-VC Remarks

1. **According to Wesley Smith, the need in the low jitter PLL multiplier has already been understood at CERN and QPLL is being developed:**
 - An auxiliary **VCXO/PLL ASIC** is now being developed by the Microelectronics Group at CERN for use as an optional auxiliary jitter filter for those applications, such as clocking high-speed serializers, for which the jitter of the raw 40.079 MHz clock output of the TTCrx is too high, see <http://proj-qpll.web.cern.ch/proj-qpll/>
 - **03/03/2003 - A data transmission test lasting for sixty hours was completed. In this test, the QPLL was used as a jitter filter for the TTCrx clock which was serving as the clock reference for both the GOL transmitter and the TLK2501deserializer. The test was run at 1.6 Gbit/s and no transmission errors were observed. Both random data and triggers (approximately 400 KHz rate) were sent on the TTC A and B channels.**



Post-VC Remarks Continue

2. There are at least two options to choose from:

- Only the CCB carries TTCrq mezzanine card with the QPLL chip and then distributes both clean 80 MHz and 40MHz clocks over Peripheral backplane to MPCs or/and over Track Finder backplane to SPs.
 - Clock may deteriorate on a long path to the TLK2501 chips, which are located near the front, not the rear of the cards.
 - Backplane timing becomes at least 2 times tighter for the 40 MHz GTLP lines under the current design.
 - Presumably current card designs are able to accommodate required changes on a firmware level – need to investigate it.
- Each MPC and SP has its own QPLL on board, which basically replaces the existing multipliers (AV9170 for MPC and VitexII DLL for SP).
 - QPLL may be placed just near the TLK2501 chips, - the ultimate consumer of the clean 80 MHz clock. The rest of the board logic perfectly works with the jittered TTCrx clock.
 - Backplane design remains intact.
 - Both MPC and SP have to be redesigned to accommodate changes in the clock distribution.