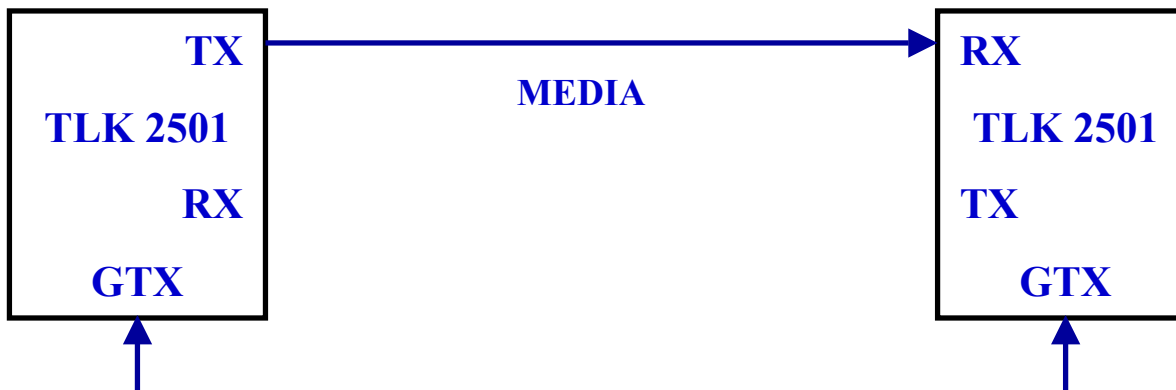




MPC-SP02 Jitter Budget

TI App note “Understanding Jitter and Bit Error for the TLK2500”



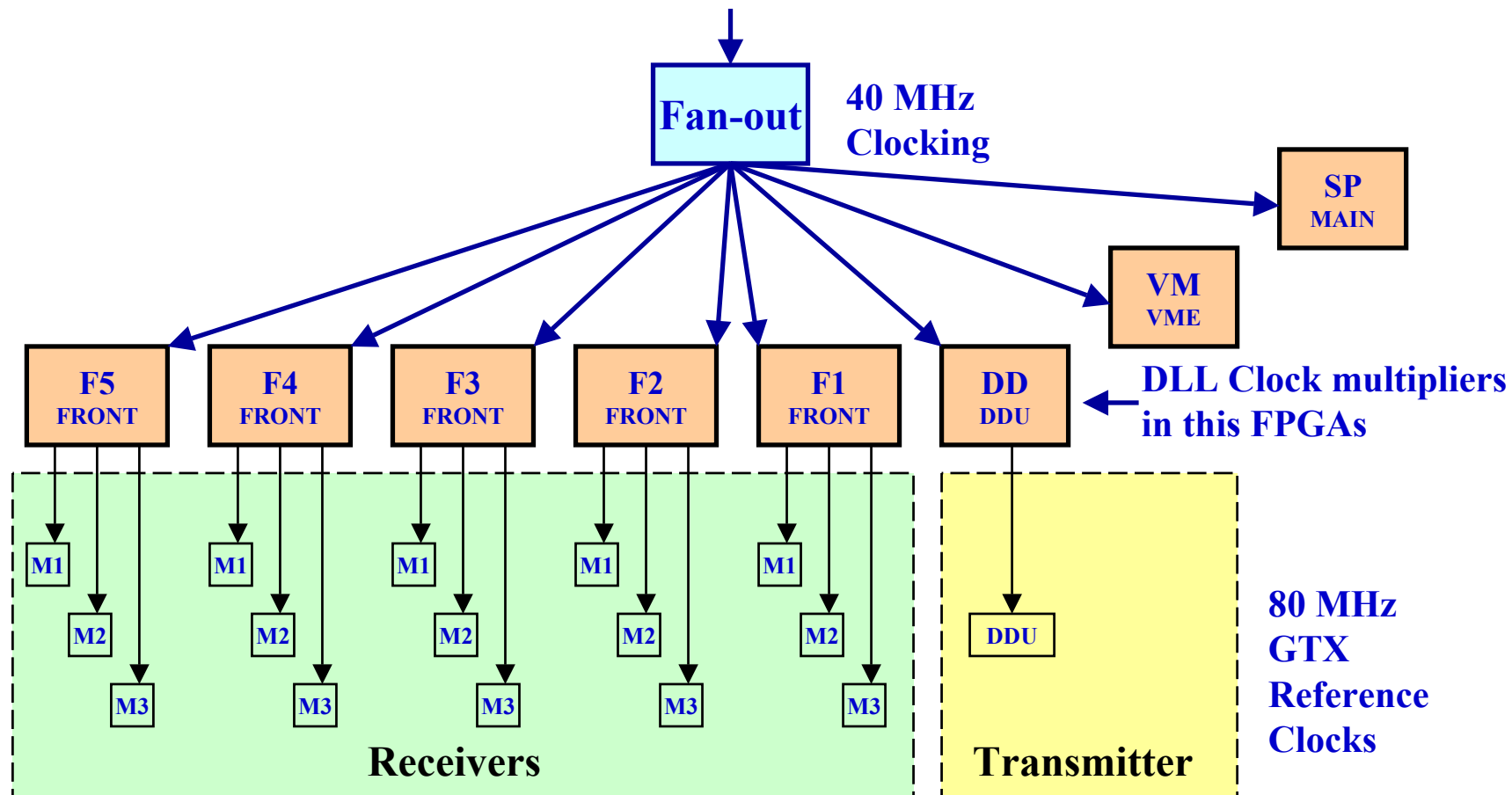
- We cannot allow more jitter in a system than the **UI**, which is **625 ps**, or errors will result
 - The transmitter is specified to consume **0.2 UI** of the budget under clean GTX (40 ps peak-to-peak) and power supply, and could be worse. GTX jitter above 5 MHz is filtered out, below – passes through.
 - The receiver is specified to consume **0.50 UI** of the budget under clean GTX (40 ps peak-to-peak) and power supply.
 - Media jitter comes from Finisar spec and is about **0.2 UI**.
 - Remaining budget is about **0.1 UI** or 60 ps.
 - GTX requires 40 ps peak-to-peak jitter max
- For reference: $PP = (6-14) * RMS$





Current SP02 Clocking Solution

SP02 utilizes Virtex-II DLLs to double the CCB 40 MHz clock for TLK2501 Transceivers





Beam Test Lessons

While CCB oscillator & TTC clock peak-to-peak jitter specs are very close:

- TTCrx chip Peak-to-peak jitter PP = 350 ps
- CCB oscillator Peak-to-peak jitter PP = 250 ps

link behavior is quite different:

- Reasonable BER when using CCB oscillator clock
- Error flood when using TTC clock

Question is, what affects the DLL (and consequently link) performance?

- Guess: different jitter spectrum of the clocks?

Tektronix TDS7000 series oscilloscope (models TDS7104 and higher) with TDSJIT3 Jitter and Timing Analysis Software might help in understanding the problem.

Availability?



Receiver Clock Requirements

Both TLK2501 Transmitter and Receiver contribute to the overall link performance/jitter

- ✓ Leave Transmitter performance enhancements to Rice (use of QPLLs, Frequency Translators, Clock Regenerator ICs, etc.)
- ✓ Improve Receiver performance by providing a jitter-free reference clock
- ✓ Reference clock may be **asynchronous** to the transmitter clock, but within 100 ppm of it → **use XO** (crystal oscillator) instead of clock multiplier
- ✓ Receiver recovered clock will still be **synchronous** to the transmitter clock

XO Requirements:

- ✓ Custom frequency of 80.1574 MHz, fundamental mode
- ✓ 3.3v power supply
- ✓ Surface mount
- ✓ ± 25 ppm or better stability (including 10 year aging)
- ✓ Jitter performance optimized for Fibre Channel applications
- ✓ Differential output (LVDS, LVPECL)

Available Devices:

- ✓ **Connor-Winfield** **P143–80.1574 MHz → LVPECL**
- ✓ **M-tron Industries** **M200116FL(P)N-80.1574 MHz → LVDS (LVPECL)**
- ✓ **SaRonix** **SEL3810A-80.1574 → LVPECL**



Updated SP02 Clocking Solution

Add 80 MHz oscillator and deliver clean clock to each TLK2501 chip

