

MPC – SP Data Format

Petersburg Nuclear Physics Institute / University of Florida

D R A F T

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Muon Trigger design enters the implementation stage. It is very important at this stage to agree upon data formats different modules exchange with each other.

Each bunch crossing the MPC sends data to the SP over optical in the format shown in Table 1. The format has been presented at a number of meetings [1], [2] and discussed over e-mail. This paper is a call for one more discussion (if anybody considers it necessary), before the draft turns into a document. Comments are appreciated.

Table 1. MPC to SP Data Format

		15	14	13	12	11	08	07	06	00
Frame	1	Quality			L/R	CLCT Pattern #		CLCT Pattern ID		
	2	BC1	BC0	SE	VP	CSC ID		AM	Wire Group ID	

Here:

CLCT Pattern IDFor high p_T patterns, the 8-bit half-strip ID is between 0 and 159.
For low p_T patterns, the 8-bit di-strip ID is between 0 and 39. This number corresponds to the position of the pattern selected at the third or “key” layer of the chamber.

CLCT Pattern #.....The 4-bit pattern number encodes the number of layers and whether the pattern consists of half-strips or di-strips. Higher pattern numbers are assigned to straighter high-momentum tracks with more layers hit.

L/R.....The Left/Right bend bit indicates whether the track is heading towards lower or higher strip number.

Quality.....The more hits the higher track Quality.

Wire Group IDThe 7-bit Wire Group ID indicates the position of the pattern within the chamber and runs from 0 to 111.

AM.....The Accelerator Muon bit indicates a pattern parallel to the beam axis.

VPThe Valid Pattern flag indicates a valid LCT pattern has been found and information is being sent on the current clock cycle.

SE.....Synchronization Error bit.

BC0, BC1Two less significant bits of the Bunch Counter.

[1] Conceptual Design for SR/SP - Internal Review, May 2001, available at:
http://www.phys.ufl.edu/~acosta/cms/srsp_may01.pdf

[2] Conceptual Design for SR/SP - Update, Rice, August 2001, available at:
http://www.phys.ufl.edu/~acosta/cms/srsp_aug01.pdf