



CERN / Rice Link Test Lessons

Requirement:

- ✓ TLK2501 Transmitter/Reference Clock Jitter – 40 ps PP max

Multiplier Specs:

- ✓ Transmitter: MPC (ICS AV9170) Clock Jitter – 1000 ps PP
- ✓ Receiver: SP02 (Virtex II DLL) Clock Jitter – 400 ps PP
- ✓ Specs for both multipliers are 10 times worse than the requirement
- ✓ DLL-based multiplier ADDS input clock jitter (CCB or TTCrx clock) to its output making it even more worse as shown by the SP-to-SP loopback tests over 100 m cable:

Clock Source	PP Jitter	BER
SP Xtal Osc	30 ps	1E-10
CCB PLL Osc	200 ps	1E-08
TTCrx	350 ps	1E-05

- ✓ PLL-based multiplier TRANSFERS some input clock jitter (CCB or TTCrx clock) to its output, but not that much.



QPLL Option

Options to improve link performance:

1. Use **QPLL** as a clock multiplier / smoother for each SP02 card to get clean reference clock for TLK2501 chips



It is **unlikely** that **QPLLs** will be available for the September test beam.



VCXO-based SP02 Patches

2. Use **QPLL substitute** as a clock multiplier / smoother.

For this, several PLL patches based on Connor-Winfield VSML31151-80.1574MHz custom VCXO have been designed.

We are going to evaluate three types of Phase Frequency Detectors:

- based on a Vectron International FX-700 Low Jitter Translator
- based on a TI TLC2934 chip
- based on a simple XOR gate

For last two PFD types, active and passive loop filter options are available for evaluation.

Complication:

TTC system uses a **40.000 MHz (not 40.078MHz)** oscillator as an internal clock source.

For **QPLL** or **QPLL Substitute** options, in order to perform link tests with the TTC system without machine clock, its internal 40.000 MHz oscillator **should be replaces** with a 40.079 MHz one.



XO SP02 Patches

3. Use Xtal Oscillator to drive TLK2501 reference clocks.



Reference clock may be **asynchronous** to the transmitter clock, but should be within 100 ppm of it .

Receiver recovered clock will still be **synchronous** to the transmitter clock.

Three patches have been made for three different types of Xtal oscillators:

Connor-Winfield VSML31151-80.1574MHz

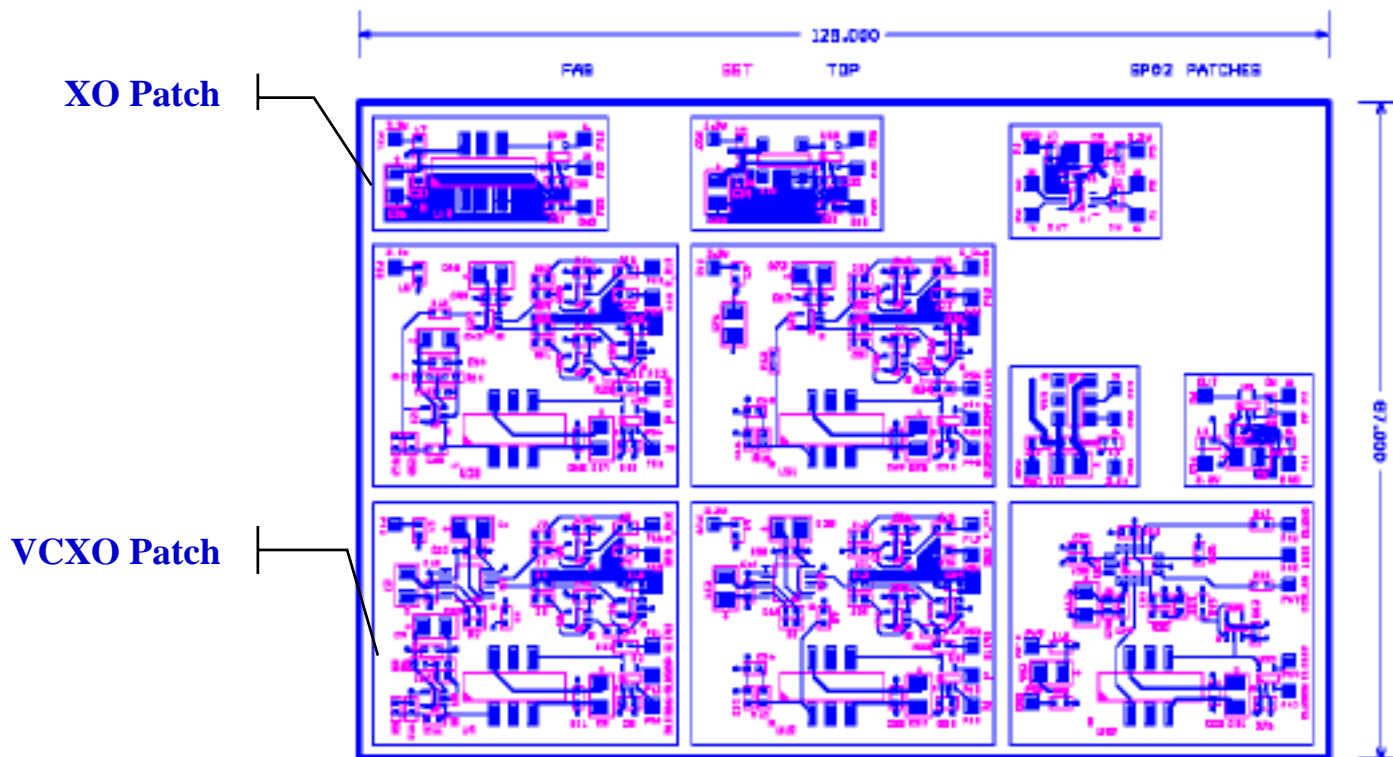
COMLOCK_CS22AZ-80.1574MHz

MF-ELECTRONICS_T3492-80.157MHz

Complication: Sp-to-SP loopback tests will be **asynchronous** to the CCB clock that drives the rest of the SP02 logic.



SP02 Patches



All patches provide differential LVDS outputs for 80.157 MHz clock and in that are **compatible** with the QPLL solution.

LVDS clock repeaters and LVDS -> LVTTTL translators are also available



Tentative Plan

July 21, 2003 – bare boards received

July 22, 2003 – patches assembled

We are going to try different clocking solutions for the SP02 card:

1. **Asynchronous** reference clock solution:
Apply clean XO clock directly to the TLK2501 GTX_CLK pin or pins or fan out it via FRONT FPGAs (preferred) to the same pins.
2. **Synchronous** reference clock solution:
 - **Apply** VCXO-based PLL patch to the CCB clock and get clean 80.1574 MHz clock near the backplane,
 - **Deliver** differential 80.1574 MHz clock to the LVDS repeater sitting near the front panel,
 - **Fan out** clean clock to the GTX_CLK pins either directly or via FRONT_FPGAs (preferred)