Towards A Unified Track-Finder Processor

Darin Acosta

University of Florida
Vienna Approach to Track Finding

Generalize scheme to include $\eta$ dependence in endcap and overlap regions for matching and Pt-assignment
### Number of Extrapolation Units Per Sector Processor

<table>
<thead>
<tr>
<th></th>
<th>DT</th>
<th>CSC</th>
<th>Overlap</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Sector size</strong></td>
<td>30° 60° 60°(30°)</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Number of stations</strong></td>
<td>4</td>
<td>3 (4)</td>
<td>3 / 4</td>
</tr>
<tr>
<td><strong>Number of extrapolation pairs</strong></td>
<td>6 3 (6)</td>
<td>3 / 6</td>
<td></td>
</tr>
<tr>
<td>(1↔2, 1↔3, 2↔3, …)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Source track segments / station</strong></td>
<td>2</td>
<td>3</td>
<td>2 / 3</td>
</tr>
<tr>
<td><strong>Target track segments / station</strong></td>
<td>12 (18)</td>
<td>3</td>
<td>3 ?</td>
</tr>
</tbody>
</table>

**Number of extrapolation units:**

- **DT:** 6 (or 9) neighbors in $\varphi$ and $\eta$ 144 (216)
  - No $\varphi$ sharing 48 (72)
- **CSC:** 3 (4) stations, no $\varphi$ sharing 27(54)
- **Overlap:** no $\varphi$ sharing 18-54+

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Darin Acosta

CMS Week, June 1998
### Inputs to a Single Pairwise Extrapolation Unit

<table>
<thead>
<tr>
<th></th>
<th>DT</th>
<th>CSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\varphi$</td>
<td>11 bits / 30°</td>
<td>12 bits / 60°</td>
</tr>
<tr>
<td>$d\varphi$</td>
<td>8 bits</td>
<td>6 bits</td>
</tr>
<tr>
<td>$\eta$</td>
<td>2 bits</td>
<td>11 bits</td>
</tr>
<tr>
<td>Quality</td>
<td>2 bits</td>
<td>3 bits</td>
</tr>
</tbody>
</table>

*n.b.* No $\eta$ information from DT in overlap region
**Effect of 12-bit $\phi$ Resolution in Endcap**

<table>
<thead>
<tr>
<th></th>
<th>ME 1 / 1</th>
<th>ME 2,3,4 / 2</th>
<th>ME 2,3,4 / 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Strip Count</td>
<td>59 / 10°</td>
<td>75 / 10°</td>
<td>75 / 20°</td>
</tr>
<tr>
<td>12-bits / 60° segmentation</td>
<td>0.09 strip</td>
<td>0.11 strip</td>
<td>0.06 strip</td>
</tr>
<tr>
<td>Resolution Contribution</td>
<td>0.03 strip</td>
<td>0.03 strip</td>
<td>0.02 strip</td>
</tr>
</tbody>
</table>

⇒ LCT $\phi$ resolution expected to be ~0.1 strip

⇒ 12-bit precision contributes < 5% to overall resolution
Block Diagram of Extrapolation Unit

- Δϕ calculation
- η correlation
- Quality correlation & assignment
- dϕ₁, Δϕ correlation
- η₁, Δϕ correlation
- Q₁, Q₂ correlation & assignment

Symbols:
- η₁, η₂
- Δϕ₁, Δϕ₁₂
- dϕ₁, dϕ₂
- Q₁, Q₁₂
Δφ Calculation Unit

⇒ Δφ result used in further correlations

⇒ Compresses φ₁ and φ₂ information into physically meaningful quantity

⇒ Only need 6 - 8 bits for φ extrapolation

⇒ Subtraction can be implemented in FPGA in 1 b.x.
12-bit Adder Ripple Delay (FFFF+1) in Xilinx XC4000 testboard
**Φ Extrapolation (dφ, Δφ Correlation)**

⇒ Checks consistency between Δφ and dφ
\( \eta \) \textit{Extrapolation}

\[ \eta_1 \xrightarrow{<11} \eta \]

\[ \eta_2 \xrightarrow{<11} \eta \]

\[ \eta \rightarrow \eta \text{ correlation unit sends } \eta_1 \text{ for further correlations if } \eta_1 \text{ and } \eta_2 \text{ are in agreement} \]

\[ \Rightarrow \text{ Necessary precision still to be determined} \]

\[ \Rightarrow \text{ LUT implementation in FPGA if the bit count is low} \]

\[ \Rightarrow \Delta \eta \text{ calculation followed by LUT if bit count is larger, or external LUTs} \]
$\eta, \Delta \phi$ Correlation Unit

$\eta \quad \Delta \phi_{12} \quad \sim 8 \quad \LUT \quad \Delta \phi_{\text{max}} \quad \sim 8 \quad <$

$\Rightarrow$ Limits $\Delta \phi$ as function of $\eta$

$\Rightarrow$ Not needed for barrel region, where $B$ is independent of $\eta$

$\Rightarrow$ Need to determine necessary $\eta$ precision
Need to define criterion
Track Assembly

- The Vienna approach in assembling tracks from station pairs is independent of extrapolation details, so the logic would be applicable for all regions.

- Further complications (and latency) arise if we try to account for track segments out of time or in neighboring $\phi$ sectors at this point.
\( P_T \) Assignment

⇒ Size of single LUT may be prohibitive

\[
\begin{align*}
\varphi_1 & \quad 12 \\
\varphi_2 & \quad 12 \\
\eta & \quad N \\
\end{align*}
\]

\[
\Rightarrow 2^{12+12+N} = 17 \times 10^6 \times 2^N \quad (\times 5 \text{ bits})
\]

⇒ Cascade logic:

\[
\begin{align*}
\varphi_1 & \quad 12 \\
\varphi_2 & \quad 12 \\
\Delta \varphi & \quad 12 \\
\Delta \varphi_{12} & \quad 12 \\
\eta & \quad N \\
\end{align*}
\]

⇒ Arithmetic unit adds 1 b.x. latency, but could use fast cascaded SDRAM instead
Features

• Trigger logic is tunable
  – Content of memory LUT is programmable
  – Any correlation unit can be set to accept all inputs
  – For example, turn off $\eta$ correlation for barrel region

• FPGA technology allows flexibility in logic design

• No extra latency in the extrapolation units to include $\eta$ dependencies (just additional correlations in parallel)

• Design hopefully evolves into the same hardware for barrel, overlap, and endcap regions
Limitations

- Neighboring $\phi$ sectors are not explicitly handled unless one copes with the *large* number of additional extrapolation units and signal inputs.

- Track segments assigned to the wrong bunch crossing are also ignored.

- Increasing the number of extrapolation units is probably the wrong approach (too many signals).

- Try to account for these minor effects in the track assembly stage to promote tracks to higher quality:
  - Require at least 2 in-time stations in one sector, then consider a limited number of late or neighboring segments.

- Multiple hits in a single CSC chamber are not tested for ghosts (2 track segments $\rightarrow$ 4). Requires more extrapolation units. Try to keep solution at motherboard level.
Further Study

• Minimize $\eta$ precision for $\Delta \phi$, $\eta$ correlation
  – Reduces LUT sizes
  – Simplifies $\eta$ determination for ME1/1 (tilted wires)

• Study extrapolation from CSC to DT in overlap region where DT has no $\eta$ information

• Useful to have backward $\phi$ extrapolation ($2 \rightarrow 1$) ?

• What is criterion for track quality assignment ?

• Improve track assembly to account for neighboring $\phi$ sectors and bunch crossings

• Any problem from ghost hits in single chamber ?

• Simulate efficiency and $P_T$ resolution (trigger rate) of track-finding algorithms