CSC Trigger Electronics in the Counting Room

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Outline

Overview
Sector Receiver functionality
Sector Processor functionality
Muon Sorter functionality
Crate design
Progress
Plans
CSC Muon Trigger Scheme

- Strip FE cards
- Wire FE cards
- Strip LCT card
- Wire LCT card

CSC Track-Finder
- Sector Receiver
- Sector Processor

In counting house
- CSC Muon Sorter
- Global μ Trigger
- Global L1

On chamber
- Motherboard
- Port Card
- 2μ / chamber
- 3μ / port card
- 3μ / sector

On periphery
- Optical
- TMB
- LCT

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Muon Track-Finding

Perform 3D track-finding from trigger primitives

Measure $P_T$, $\phi$, and $\eta$

Transmit highest $P_T$ candidates to Global L1
CSC Track-Finder Requirements

High efficiency

Trigger Rate:
- Single muon rate < few kHz at $L = 10^{34} \text{cm}^{-2} \text{s}^{-1}$

Resolution:
- $\sigma_{P_t} / P_t \leq 30\%$ (Requires $\eta$ information)

Multi-muon capability:
- $\leq 3$ muons per 60° sector
- Best 4 muons sent to Global L1

Redundancy
- Require only 2 stations out of 3 (or 4)

Minimal latency, programmable
CSC Muon Trigger Rates

- Single $\mu$ rate from Pythia, convoluted with efficiency curve
- Thresholds set for 90% efficiency
- Require rates < 1 kHz per unit rapidity
- Not satisfied for $P_T$ resolution worse than 30%

![Graph showing Muon Rate $dN/d\eta dt$ vs Effective $P_T$ Threshold (GeV/c)]

$L = 10^{34} \text{ cm}^{-2} \text{s}^{-1}$

PYTHIA6

CSC resolution from CMSIM
Trigger Regions in $\eta$

Separate trigger regions

Overlap $1.2 > \eta > 0.9$

CSC

DT

ME3 ME2 ME1

MB4 MB3 MB2 MB1
Track-Finding performed in independent 60° sectors

Illustration of overlap region
• CSC and DT segments are required for efficient coverage of \(0.9 < |\eta| < 1.2\)

• Agreement with Vienna and Bologna on Barrel/Endcap boundary (CMS IN 1999/015)
  \(\Rightarrow\) Barrel and Endcap Track-Finders are fundamentally different (2D vs. 3D)
  \(\Rightarrow\) Information sent both ways
    • \(\text{MB2/1+MB2/2} \Rightarrow \text{CSC T-F} \quad \text{ME1/3+ME2/2} \Rightarrow \text{DT T-F}\)
  \(\Rightarrow\) Programmable sharp \(\eta\) boundary
    • Avoids duplication of single muon in overlap region
  \(\Rightarrow\) Separate sorting of CSC and DT muons
Sector Partitioning

30° or 20° subsectors in ME1

2 or 3 MPC

6 μ / SR

60° sectors in ME2 — ME4
Sector Receiver Functionality

- Receives 6 $\mu$ segments via 12 optical links from 2 Muon Port Cards
- Synchronizes the data
- Reformats the data
  \[ \Rightarrow \text{LCT bit pattern} \rightarrow \eta, \phi, \Psi, \ldots \]
- Applies alignment corrections
- Communicates to Sector Processors via custom backplane (Channel Link)
- Fans out signals to DT Track-Finder

- Functional block diagram developed and board layout started

\[ \Rightarrow \] via LUT
Required Precision of Data

Azimuthal angle $\phi$:
- 12 bits / 60° $\Rightarrow$ 1 bit / 0.26 mrad (0.1 strip)

Bend angle $\Psi$:
- 6 bits / ±45° $\Rightarrow$ 1 bit / 60 mrad

Polar angle $\eta$:
- 6 bits / 1.5 units $\Rightarrow$ 1 bit / 0.025

Quality:
- 3 bits

Chamber i.d.:
- 6 bits

Accelerator $\mu$ flag: 1 bit

34 bits per CSC segment to Sector Processor
Sector Receiver Board Layout

Optical Receivers
SRAM LUTs

muon 1
muon 2
muon 3
muon 4
muon 5
muon 6

Channel Link transmitters & connectors

VME

optical fiber

7 Synchronous SRAMS (CYPRESS) / muon

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Sector Processor Functionality

- Identify and measure muons from ~ 600 bits every 25ns (3 GB/s)
- Perform all possible station-to-station extrapolations in parallel
  ⇒ Simultaneously search roads in $\phi$ and $\eta$
- Assemble 3- and 4-station tracks from 2-station extrapolations
- Cancel redundant short tracks if track is 3 or 4 stations in length
- Select the three best candidates
- Calculate $P_T$, $\phi$, $\eta$ and send to CSC muon sorter:
  $22 \text{ bits} \times 3 = 66 \text{ bits}$
- Functional block diagram developed
• Perform all combinations of extrapolations in parallel:
  \[ 1_i \leftrightarrow 2_k, \; 1_i \leftrightarrow 3_k, \; 2_i \leftrightarrow 3_k \]
  \[ 2_i \leftrightarrow 4_k, \; 3_i \leftrightarrow 4_k \]
  But not \[ 1_i \leftrightarrow 4_k \]

• Track Assembler takes best 2 or 3 extrapolations per reference segment
Data Stream Paths

**Stream 1**

- **Extrapolation Units**
  - 1 – 3, 2 – 3, 3 – 4 Extrapolations

**Stream 2**

- **Track Assembler Unit (TAU1)**
  - Track types:
    - 1 – 2
    - 2 – 3
    - 3 – 4
    - 1 – 2 – 3 – 4

- **Track Assembler Unit (TAU2)**
  - Track types:
    - 1 – 3
    - 2 – 3
    - 3 – 4
    - 1 – 3 – 4
    - 2 – 3 – 4

1 – 2, 2 – 3, 2 – 4 Extrapolations
Track Assembler Unit (TAU1)

- **3 best extrapolations**
- **4 (2+2) best extrapolations**

Multiplexer

- **Sel1**
- **Sel2**
- **Sel3**

Selection Unit

- **Link 2₁**
- **Link 2₂**
- **Link 2₃**

Extrapolations Quality

LUT 32Kx16

- **2₁ - 1**
- **2₁ - 3**
- **2₁ - 4**

- **32Kx16**

Link

- **A₁**
- **A₂**
- **A₃**

- **B₁**
- **B₂**
- **B₃**

- **C₁**
- **C₂**
- **C₃**

Track Absolute Quality

2bits + 2bits:
2 bits select 2₁, 2₂ or 2₃ stream
2 bits select h., m. or l. priority track

Track Local Quality

7 bits:
- Hit number (1st chamber) – 3
- Hit number (2nd chamber) – 2
- Hit number (3rd chamber) – 2
- Hit number (4th chamber) – 2

- **To Final Selection Unit**
  - Hit Number Part
  - Extrapolation Quality Part

- **4→5**

- **4 bits + 3 bits + 3 bits according to the order of priority (PCB Layout)**

- **2 bits + 2 bits according to the order of priority (PCB Layout)**

- **3 bits + 3 bits + 3 bits**

- **8 ([2 bits Quality + 2 bits Number] x 2)**

- **15 ([2 bits Quality + 3 bits Number] x 3)**

- **4 (2+2) best extrapolations**

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Each track consists of 4 track segments as maximum. 6 Tracks has 24 track segments. We need 10 (5+5) bits to describe all possible combinations.

Extrapolations Quality Comparators (9 Units)

Hit Number Comparators (9 Units)

Final Selection Unit

MUX

Sel1 Sel2 Sel3

Final Decision Unit

LUT 256Kx32

From Track Assembling Unit (Hit Number Part)

Stream 1

Stream 2

Track 6 9

Track 5 9

Track 4 9

Track 3 9

Track 2 9

Track 1 9

8 bits:
1st track segment number – 4 bits:
2nd track segment number – 4 bits:
(if we need only 2 track segments
for Pt calculation)

To Data Extraction Multiplexer

8 bits:

Each track consists of 4 track
segments as maximum

6 Tracks has 24 track
segments

We need 10 (5+5) bits to
describe all possible
combinations.

We should compare:
Track1-Track4; Track1-Track5;
Track1-Track6; Track2-Track4;
Track2-Track5; Track2-Track6;
Track3-Track4; Track3-Track5;
Track3-Track6 (9 bits as total)

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Muon Sorter Functionality

• The 3 highest rank muons from each Sector Processor are sent to the CSC muon sorter, which selects the 4 highest rank
• Total muon count:
  ⇒ 3 muons × 6 sectors × 2 endcaps × 2 regions = 72 muons for CSC and OVL regions
• Sort is based on 7 bits (5 bits for $P_T$ and 2 bits for quality)
  ⇒ Basic sorting unit design (4 best out of 8) is complete
• Input: 72 × 22 bits = 1584 bits
• Output: 4 × 22 bits = 88 bits
  ⇒ Sent to Global L1 Muon Trigger for association with RPC and DT triggers
CSC Track-Finder Crate Organization

CSC and overlap regions handled in same crate

Two 60° sectors per crate

CSC Counting House electronics:

- Racks: 3 or 4
- Crates: 6
- Sector Receivers: 24
- Sector Processors: 24
- Muon Sorter: 1
Layout for Track-Finder Crate

Two 60° sectors housed in one 9U VME crate with custom backplane
Backplane Connections

- Channel Link custom backplane
- AMP Z-Pack 2mm connectors

Not shown: 204 bits (8 µ) from DT trigger to SP-OVR
Design Progress

• Full conceptual design from trigger primitives to Global L1 Trigger
  ⇒ Bit counts fully documented
  ⇒ Crate design underway
  ⇒ Sector Receiver functionality defined
  ⇒ Sector Processor algorithms defined
  ⇒ Sort algorithms defined

• Simulation of Track-Finder performance underway
  ⇒ resolution, efficiency, rate, chamber misalignment

• Prototyping started
Milestones / Schedule

√ D387 – 1999 Mar, Sector Receiver  Initial System Design (UCLA)
√ D331 – 1999 Mar, Sector Processor Initial System Design (Florida)

D390 – 1999 Sep, Sector Receiver  Prototype Design (UCLA)
D332 – 1999 Sep, Sector Processor Prototype Design (Florida)
on schedule

D391 – 2000 Jan, Sector Receiver  Prototype (UCLA)
D334 – 2000 Jan, Sector Processor Prototype (Florida)
D335 – 2000 Apr, Sector Receiver / Processor Crate Test
• Sector Processor design and simulation:
  • http://www.phys.ufl.edu/~acosta/cms/trigger.html

• Sector Receiver design and overall CSC trigger bit document:
  • http://www-collider.physics.ucla.edu/cms/trigger/