The CSC Track-Finding Processor

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CSC Muon Trigger Scheme

Strip FE cards

Strip LCT card

LCT

Motherboard

Port Card

TMB

PC

2μ / chamber

3μ / port card

CSC Track-Finder

Sector Receiver

Sector Processor

OPTICAL

SR

SP

3μ / sector

In counting house

On chamber

In chamber crate

Wire FE cards

Wire LCT card

LCT

On chamber

In chamber crate

CSC Muon Sorter

Global μ Trigger

Global L1

RPC

DT

4μ

4μ

4μ

4μ
Muon Track-Finding

- Link trigger primitives into tracks
- Assign $P_T$, $\varphi$, and $\eta$
- Send highest $P_T$ candidates to Global L1 trigger
CSC Track-Finder Requirements

- Trigger Rate: Single muon rate < few kHz at \( L = 10^{34} \text{cm}^{-2} \text{s}^{-1} \)
- Resolution: \( \sigma_{P_t} / P_t \leq 30\% \) \((\text{Requires } \eta \text{ information})\)
- Threshold: \( P_t > 3 \text{ GeV} \)
- Selection: \( \leq 3 \text{ muons per 60}^\circ \text{ sector} \)
- Redundancy: Require 2 stations out of 3 or 4
- Latency: \( \leq 16 \text{ b.x. for Sector Processor} \)
- Pipelined
- High Efficiency
- Programmable
- Test features
Trigger Regions in $\eta$
Trigger Regions in $\phi$
### Track Segments per Sector

<table>
<thead>
<tr>
<th>Region</th>
<th>Station</th>
<th>Chamber</th>
<th>Segments per sector</th>
<th>No. of φ sectors</th>
<th>No. of segments</th>
<th>Extrapolations</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSC</td>
<td>1</td>
<td>ME1</td>
<td>3</td>
<td>2</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>ME2</td>
<td>3</td>
<td>1</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>ME3</td>
<td>3</td>
<td>1</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>ME4</td>
<td>3</td>
<td>1</td>
<td>3</td>
<td>81</td>
</tr>
<tr>
<td>OVL</td>
<td>1</td>
<td>MB1</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>MB2</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>ME1</td>
<td>3</td>
<td>2</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>ME2</td>
<td>3</td>
<td>1</td>
<td>3</td>
<td>106</td>
</tr>
</tbody>
</table>

- Neighbors in $\phi$ are not considered:
  - CSC chambers project in $\phi$
  - $\Delta\phi_{12} < 3^\circ$ for $P_T > 10$ GeV
- Neighbors in $\eta$ do not exist
Differences between CSC and DT Track-Finders

• No neighbor input for CSC T-F implies
  – Fewer extrapolations
  – Less data input
  – Fewer signals to fan out
  – Less opportunity for two tracks to arise from one muon

• Inclusion of $\eta$ in CSC T-F allows
  – Precise $P_T$ assignment in endcap
  – Track-Finding in 3 dimensions
  – Rate reduction

• Therefore, CSC T-F is fundamentally different than DT T-F

• Coverage of overlap region in CSC T-F complements approach taken by DT T-F
Required Precision of Data

- Azimuthal angle $\phi$:
  - 12 bits / 60° $\Rightarrow$ 1 bit / 0.26 mrad (0.1 strip)

- Bend angle $\Psi$:
  - 6 bits / ±45° $\Rightarrow$ 1 bit / 60 mrad

- Polar angle $\eta$:
  - B-field variation $< \pm 3\%$ for 0.05 unit bins
  - 5 bits / 1.5 units $\Rightarrow$ 1 bit / 0.05

- Quality:
  - 3 bits

- Full precision needed for $P_T$ assignment only, not extrapolation
  - e.g. $\phi$ : 7 bits    $\Delta \phi$ : 6 bits
**Inputs to CSC Sector Processor**

- 1 CSC stub = 12 $\varphi$ bits + 6 $\Psi$ bits + 5 $\eta$ bits + 3 Q bits = 26 bits
- 1 Port Card sends 3 stubs
- 1 Sector Receiver accepts 2 Port Cards = 6 stubs
- 1 Sector Processor accepts $6 + 3 + 3 + 3 = 15$ stubs (divided between 2.5 Sector Receivers)
- $15 \text{ stubs} \times 26 \text{ bits} = 390 \text{ bits}$

CSC crate: 9U VME with custom point-to-point backplane for last 3U
Inputs to OVL Sector Processor

- 1 CSC stub = 26 bits
- 1 DT stub = 11 \( \phi \) bits + 8 \( \Psi \) bits + 3 Q bits = 22 bits
- 1 Sector Processor accepts 4+4 DT stubs and 6+3 CSC stubs
- (8 DT stubs \( \times \) 22 bits) + (9 CSC stubs \( \times \) 26 bits) = 410 bits
- DT stubs sent from DT trigger fan-out unit

OVL crate: 9U VME with custom point-to-point backplane for last 3U
CSC Track-Finder Crate Organization

CSC Counting House electronics:

Racks: 4
Crates: 8 (including power supply, controller, CCC)
Sector Processors: 24
Sector Receivers: 48
Muon Sorter: 1
Sector Receiver Functionality

- Receives 6 stubs via optical links from 2 Port Cards
- Synchronizes the data
- Reformats the data
  - LCT bit pattern $\rightarrow \eta, \varphi, \Psi$
- Communicates to Sector Processor via custom point-to-point backplane
- Fans out signals to CSC overlap processors and sends ME1/3 signals to DT Sector Processor
Sector Processor Functionality

- Sector Processor must identify muons from ~400 bits every 25ns (2 GB/s)
  1. Perform all possible station-to-station extrapolations in parallel
     *Simultaneously search for roads in $\phi$ and $\eta$*
  2. Assemble 3- and 4-station tracks from 2-station extrapolations
  3. Cancel redundant short tracks if track is 3 or 4 stations in length
  4. Select the three best candidates
  5. Calculate $P_T$, $\phi$, $\eta$ and send to CSC muon sorter:

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Precision</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\eta$</td>
<td>6 bits</td>
</tr>
<tr>
<td>$\phi$</td>
<td>8 bits</td>
</tr>
<tr>
<td>Muon sign</td>
<td>1 bit</td>
</tr>
<tr>
<td>$P_T$</td>
<td>5 bits (nonlinear)</td>
</tr>
<tr>
<td>Quality</td>
<td>2 bits</td>
</tr>
</tbody>
</table>
**Sector Processor Block Diagram**

![Block Diagram Image]

**FIG. 1. TRACK FINDING PROCESSOR. BLOCK DIAGRAM.**

**EU** - Extrapolation Unit  
**QSU** - Quality Selection Unit  
**TAU** - Track Assembling Unit  
**FSU** - Final Selection Unit  
**CLOCKED FIFO**  
**MUX**  
**STA**  
**PI LOOK-UP**  
**FIFO**  

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**STA**  
**PI LOOK-UP**  
**FIFO**
Extrapolation Unit Detail

\( \eta \) road finder

Result quality

Coarse \( P_T \) assign

\( \phi \) road finder
Implementation Technology

• Sector Processor logic to be implemented in FPGAs and RAM

• Attempt to run some logic at 80 MHz

• Study of Xilinx FPGA implementation of Extrapolation Unit only:
  – Small number of chips needed for extrapolation (3)
  – Number of I/O pins needed per chip under control (~250)
  – Logic size under control (~60K gates)
  – No external RAM needed
  – Routing resources inside chip limits minimum chip size

• Complication of $\eta$ dependence for $P_T$ assignment under control
Assignment Unit

Clock RAMs at 80 MHz
⇒ 1 b.x. delay only
CSC Muon Sorter

- The three highest rank muons from each Sector Processor are sent to the CSC muon sorter, which then selects the four highest rank overall.

- Total muon count:
  - $3 \text{ muons} \times 6 \text{ sectors} \times 2 \text{ endcaps} = 36 \text{ muons}$ for CSC only
  - $\times 2 = 72 \text{ muons}$ for CSC and OVL regions

- For comparison, the DT muon sorter accepts 24 muons

- Sort is based on 7 bits (5 bits for $P_T$ and 2 bits for quality)

- One sorter card is necessary for entire CSC+OVL
Milestones / Schedule

- D387 – 1999 Mar, Sector Receiver Initial System Design
- D331 – 1999 Mar, Sector Processor Initial System Design
- D390 – 1999 Sep, Sector Receiver Prototype Design
- D332 – 1999 Sep, Sector Processor Prototype Design
- D391 – 2000 Jan, Sector Receiver Prototype
- D334 – 2000 Jan, Sector Processor Prototype
- D335 – 2000 Apr, Sector Receiver / Processor Crate Test
- Dnnn – 2001 Sep, Sector Receiver Final Design
- Dnnn – 2002 Apr, Sector Processor Final Design
- Dnnn – 2003 May, Sector Receiver Produced
- Dnnn – 2003 Aug, Sector Processor Produced
- Dnnn – 2003 Oct, Sector Receiver Installed
- Dnnn – 2004 Jan, Sector Processor Installed
- Dnnn – 2004 Sep, Trigger System Tested
Documentation

• Can be found at:
  – http://www.phys.ufl.edu/~acosta/cms/trigger.html

• Includes more detailed design descriptions and some simulation results