Sector Processor 2002
Development and Test Plans

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Some History on SP Work

Discussion took place by telephone Nov.4 regarding PNPI past activities and future plans

→ Detailed written report by Lev sent as well on work since May

History:

→ Schematics for 85% of board completed by June
→ Trial routing for main board started in June, incremental approach to working on layout and back-annotating to schematics since then
→ Mezzanine card schematics and routing successfully completed in parallel

The disaster (early September):

→ Although careful attention paid to transceiver and LUT routing, bottleneck revealed in VME, DDU and fast control busses to Front FPGAs
→ Had to reassign pins to avoid exceeding max number of layers of OrCAD Layout
→ Program failure occurred when trying to back-annotate to schematics
→ Older backups were for pin assignment and routing that could not be accomplished in 16 layers
Conclusions of PNPI Layout Work

ORCAD Layout software was not up to the task (or at least not optimal)

- Pushing maximum number of layers (16)
- Pushing maximum number of components, nets, connections, etc.
- Very sluggish Windows response preceded fatal crash
- Labor intensive (manual routing of 4 merged boards!)

Long absence from Florida because of visa delays led to communication break-down

- Status reports were not always timely or detailed enough to take immediate action. I did not immediately recognize this because we were expecting a visit to UF “soon” starting in August. (We had arranged in-person reports before then, such as at June CMS week.)
- Immediate solution is to implement weekly telephone meetings with everyone (engineers and supervisors) in attendance
- Design files will be sent periodically to Florida so that everyone is informed of status and what is being worked on.
We are still waiting for approval on Lev and Victor’s J visa application for their visit to Florida

Called U.S. consulate in St. Petersburg

- Processing time is unpredictable, depends case by case
- Once we start this procedure, we cannot re-apply for a shorter visit with a B visa. They will wait until they hear back from Washington in any case on the first application
- In general, issuance of B visas may go faster (anecdotal information from Victor and impression I got from consulate). They are scrutinizing the nature of the visit, and a short visit means one is not staying to do much work.
- B visa is for short visits, but you can have multiple entries in a 2 year period. May be best for future visits.

We continue collaboration with engineers working at PNPI, with more detailed reporting, and with Lev and Victor coming to Florida as soon as visa is granted
Engineering Priorities

1. Top priority is for Alex and Lev to review progress of layout and to answer any questions from vendor
   - Lev recently sent an updated list of layout concerns to the vendor based on his previous experience
   - Component placement received
   - Estimate of completion for layout, fab, and assembly is mid-Jan.

2. Develop firmware for VME/CCB interface and Front FPGAs
   - PNPI. Necessary for optical link tests.

3. Routing of the Track-Finder backplane (in parallel with #2)
   - Alex. Also necessary for multi-board tests.

4. Develop firmware for SP chip
   - Alex. Trigger logic done, but supporting logic still to do

5. Develop DDU firmware
   - PNPI

6. Schematics and layout of DT transition card
   - PNPI
Assignment of Resources

PNPI:

- Front FPGA firmware: Lev, full-time, 2–3 months. Work starts at PNPI, but shifts to UF whenever visa issued.
- VME/CCB FPGA firmware: Misha Kan, 50% time, 2–3 months, supervised by Lev. (Training of Evgeny Nikolaev on Verilog during development.)
  - Feb. 1 is deadline for these two items, but hope to have it ready earlier if SP board is ready. Critical path.
- DT Transition card schematics and layout: Evgeny Nikolaev, full-time, 2 months, Feb. 1 – Apr. 1 2003
- DDU FPGA firmware: Victor, 50% time, 3.5 months starting Dec. 1.

Florida:

- Backplane routing. Alex, full-time, 3 weeks, already started.
- SP firmware. Alex, full-time, 3 weeks following backplane
Production Costs

Orders for most parts placed

- Total component cost for SP prototypes exceeds WBS 3.1.1.17.2.2 (SR/SP) by $25K! ($46K vs. $21K)
  - FPGAs: $24K; memories: $6K; optical: $9K; misc: $7K
- 5–6 week delay on most Xilinx FPGAs (mid Dec.)

SP main board fabrication and assembly

- Fab: $7K for 5 boards; Ass: $9K for 3 fully stuffed boards

Backplane:

- Expect similar to EMU: $4K for 4 boards + component cost

Mezzanine card:

- No quote yet for fabrication or assembly.

Fabrication and Assembly costs so far appear to be within budget. Component cost exceeded by $25K.
Development of Test Software

Standalone ORCA simulation for latest SR/SP prototype is completed
- Finished by Bobby, earlier work by Slava and D.A.
- Interface class reads ASCII files with LCT info (or generates random numbers), makes available to simulation classes and hardware interface classes
- Still require update from Rice on MPC sorter logic

Configuration software
- Previous tools for JTAG download of FPGA firmware through VME, and VME read/write of LUTs, have been ported to Linux by Holger
- Needs updating to SP2002 registers, conversion to HAL, and integration with software below:

Test routines
- Need XDAQ/HAL compliant classes to download data into input registers as well as to read out output buffers
- Need integration with Rice TMB/CCB/MPC test software
- Critical path.
Resources for Software Development

Bobby Scurlock
- Student, full-time, VME test software and simulation studies

Holger Stoeck
- Post-doc, 50% time, VME test software, XDAQ

Song Ming Wang
- Post-doc, 50% time, XDAQ, Run ctrl.
  2 week visit to UF now, continue contributions beyond then

Alex Madorsky
- HW and SW engineer, author of some original SP code and our “technical consultant” for new development
- 100% time during testing period

 Longer term:
- Barashko, Drozdetski, Madorsky available to help with interface to EMU FAST-DAQ software
Software and Test Plans

Initial goal is to have a HAL-compliant C++ class written and tested in the next 2 weeks to read & write data into SP2000 registers

- Should be straightforward to adapt to SP2002 when needed

Next goal is to incorporate Rice TMB/MPC/CCB test software into a common environment

- Needs to be modified to accept events from the ORCA Interface Manager
- Would be useful to arrange a meeting with Rice to discuss how best to do this (which version of code to start from)
- Try out this merged code for the same tests already conducted to make sure software is working properly
  - Ship an MPC to UF? (or a UF person to Rice?)

After getting the framework established, continue on with writing SP test software

- Code to coordinate tests among all boards
- Inclusion of XDAQ communication across multiple PCs (or at least multiple VME controllers)
  - But will arrange to have test slots in TF backplane for several MPCs (otherwise we need several peripheral crates!)
CVS Repository and Web Page

http://www.phys.ufl.edu/~tfcvs

Instructions for access ➔

Documentation on packages (to come) ➔

Tagged releases ➔