Level-1 CSC Track-Finder Simulation Status

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Outline

1. Improvements to ORCA Simulation Model LUTs.
2. Switch to ORCA-fied Verilog Model.
3. Modifications for ME1/1a Ganged Strip Study
4. Future Improvements to Track-Finder.
Improvements to Simulation Since May 2001

• cf D. Acosta, CMS Note 2001/033 – Status of CSC TF as of May 2001

• Simulation: Trigger Primitive improvement: J. Mumford, CMS Note [soon to be released].

• ORCA CSC TF Model will include new cuts on $\Delta\phi$ and $\Delta\eta$ to reduce background rates.

• In ORCA: $P_T$ definition using 90% of efficiency curve maximum has been retuned.

• Change from Xilinx schematic based SP design to Verilog program complete.

• Verilog code translated to C++ is now integrated into ORCA environment.

• Studies to be conducted on improving $P_T$ resolution using bend angle.
Track-Finder is implemented as 12 Sector Processors (SP)

**BXA:** Allows SP to analyze track segments received out of time.

**EU:** Test consistency of 2 track segments to share track.

**TAU:** Links successfully extrapolated segments.

**FSU:** Selects best 3 tracks, cancels redundant tracks.

**AU:** Assigns $P_t$ value and uncertainty.
Extrapolation Unit

η Road Finder:
- Check if track segment is in allowed trigger region in η.
- Check if Δη and η bend angle are consistent with a track originating at the collision vertex.

Quality Assignment Unit:
- Assigns final quality of extrapolation by looking at output from η and φ road finders and the track segment quality.

φ Road Finder:
- Check if Δφ is consistent with φ bend angle φ_b measured at each station.
- Check if Δφ in allowed range for each η window.
We use 6 bits for $\eta$ in range 0.9-2.5.

$\therefore$ we have 0.025 $\eta$-unit binning.

$\Delta \eta$ plots show best window to be one $\eta$-bin (0.025 $\eta$-units).

Plots generated using single muon events for $P_t=5\text{GeV/c}$.

This takes advantage of $\eta$ corrections in SR for ME1/1
We can further restrict $\Delta \phi$ range by looking in each of the 64 $\eta$ bins in end-caps, and finding the maximum allowable $\Delta \phi[\eta]$ value. We do this for:

- Low Pt: 3 and 5 GeV/c (Depends on EU)
- Med Pt: 15 GeV/c
- High Pt: 25 GeV/c
CSC Trigger Efficiency vs. $P_T$

- Efficiency as of May
  - Trigger threshold defined at 90% efficiency
  - Efficiency unaffected by new cuts and improved since May (with Improved Trigger Primitives)

Current Efficiency

- Efficiency unaffected by new cuts and improved since May (with Improved Trigger Primitives)
**CSC Single Muon Rate**

- Weighted minimum bias sample used to estimate rate for $L = 10^{34}$

- Rate reduced by half

- Plots converge at $\text{Pt}_{\text{cut}} = 8 \ \text{GeV/c}$.

So, new cuts only helpful in low Pt range.
We will use correlation between $\Delta \phi$ and $\phi_{\text{bend}}$ to find allowed range for $\Delta \phi$ in a given $\eta$ and $\phi_{\text{bend}}$ bin. This will also allow us to further untangle low Pt from high Pt tracks.

Extrapolation Type: MB1-ME2

$\phi_{\text{bend}}$ given by DT

$0 < \text{Pt} < 10$
$10 < \text{Pt} < 25$
$25 < \text{Pt} < 50$
$50 < \text{Pt} < 100$

$0.8 < \eta < 1.2$
First Implementation of $f_b$ for CSCs

Currently, we just use the CLCT Pattern Numbers.

These patterns are defined for both half and di-strip track segments corresponding to high and low momentum tracks.

Patterns 1 and 2 are very similar. They do not give enough bend information.
**NEW: Tuning** $\Delta \phi[\eta, \phi_b]$ **LUTs**

Extrapolation Type:
- **ME1-ME2**

$\phi_b$ bend given by CSC $\frac{1}{2}$ Strips

[Same Applies for Di-Strips]

### Cutting on $\phi_b = \pm 2$:
- Brings trigger efficiency down to 95%
- Rate only reduces by 50% for $Pt<7$

We need more half strip $\phi_b$ bend patterns from CSCs. With the current Trigger design, we do not have enough information to establish cuts or to discriminate low from high Pt tracks.

**Increase number of $\frac{1}{2}$ Strip Patterns?**

[Remove Di-Strips?]
Current Status of Verilog SP Model

Sector Processor SW Modification Scheme

ORCA SP C++ Model

Verilog HW Program

“Verilog” C++ Translation

Model Change

ORCA SP C++ Model

Verilog HW Program

“Verilog” C++ Translation

ORCA SP C++ Model

Verilog HW Program

“Verilog” C++ Translation

ORCA SP C++ Model

Verilog HW Program

“Verilog” C++ Translation

Verilog SW Model checked against ORCA SP Model: in perfect agreement

ORCA-fication Complete!

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New Development Scheme

Post ORCA-fication:

"Verilog" C++ Translation

Model Change

"Verilog" C++ Translation

"Verilog" C++ Translation

"Verilog" C++ Translation

Verification

Verilog HW Program

Verilog HW Program

Verilog HW Program

Verilog HW Program

$t_0$ $t$
Verilog SP Model

Sample of Verilog SP SW Model Translated to C++

```c
//
c[11:0] = {b[7:4], a[8:1]};
c = ((b & 0xf0) << 4) | ((a & 0x1fe) >> 1);
//
c[12] = ((phiB >= phiA) || (phiB >= phiC)) & ((phiA >= phiB) || (phiC >= phiB));
c |= (((phiB >= phiA) || (phiB >= phiC)) & ((phiA >= phiB) || (phiC >= phiB))) ? 0x1000 : 0;
mode = Mode(rank);
modeout =
    ((etaPT < 3) && ((mode == 2) || (mode == 3))) ? 6 :
    ((etaPT < 3) && (mode == 4)) ? 7 :
    ((etaPT < 3) && (mode == 5)) ? 8 :
    mode;
modenew = ((modeout == 2) && (modeout <= 5)) ? 1 :
    (modenew == 0) ? d : c;
//
//

sign = (phiA >= phiB) && (si == 0);
```

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Verilog SP Model

Currently, Implementation of Verilog SP Model is controlled with a switch in the .orcarc file.

- Available in ORCA 6
- The current switch is: “CSCTrackFinder:verilog = 1”
- Default is currently old model, but not for long…

Another Switch in the .orcarc file is:

Enable Ganging of ME1/1a:

- CSCTrackFinder:ORedME1A = 1
- Muon:Endcap:ORedME1A = 1
Enabling Ganging of ME1/1a

Generated 98 single muons with
50 < Pt < 100 and 2.0 < \( \eta \) < 2.4

Full ME1/1a:
CSC TF reconstructs 56 tracks with Pt>10GeV

ME1/1a Ganged 3-Strips, No ghosts created
CSC TF reconstructs 27 tracks with Pt>10GeV
Lose \( \mu \)'s to low Pt tracks

ME1/1a Ganged 3-Strips, created ghosts in CSC TF
CSC TF reconstructs 51 tracks with Pt>10GeV
Recovered \( \mu \)'s

“Efficiency” is about 90% to recover tracks
Conclusions

What’s been done in ORCA 6?

- $\Delta \eta$ windows installed
- New $\Delta \phi[\eta]$ cuts installed for ME1 and MB1 Extrapolations
- Default Verilog Based SP SW Model controlled by switch

Soon to come:

- Verilog will become default.
- Use 7 bits for $\eta$ to allow finer tuning in $\eta$ windows.
- Install $\Delta \phi[\eta]$ cuts for other Extrapolation types.
- Install $\Delta \phi[\eta, \phi_b]$ cuts using improved CLCT pattern numbers.
- Improve Pt resolution using parameterized fits in both $\eta$ and $\phi_b$ windows [long term].

Include SP Bunch crossing analyzer in ORCA. This is needed to Correctly handle out-of-time track segments for detailed neutron background study.